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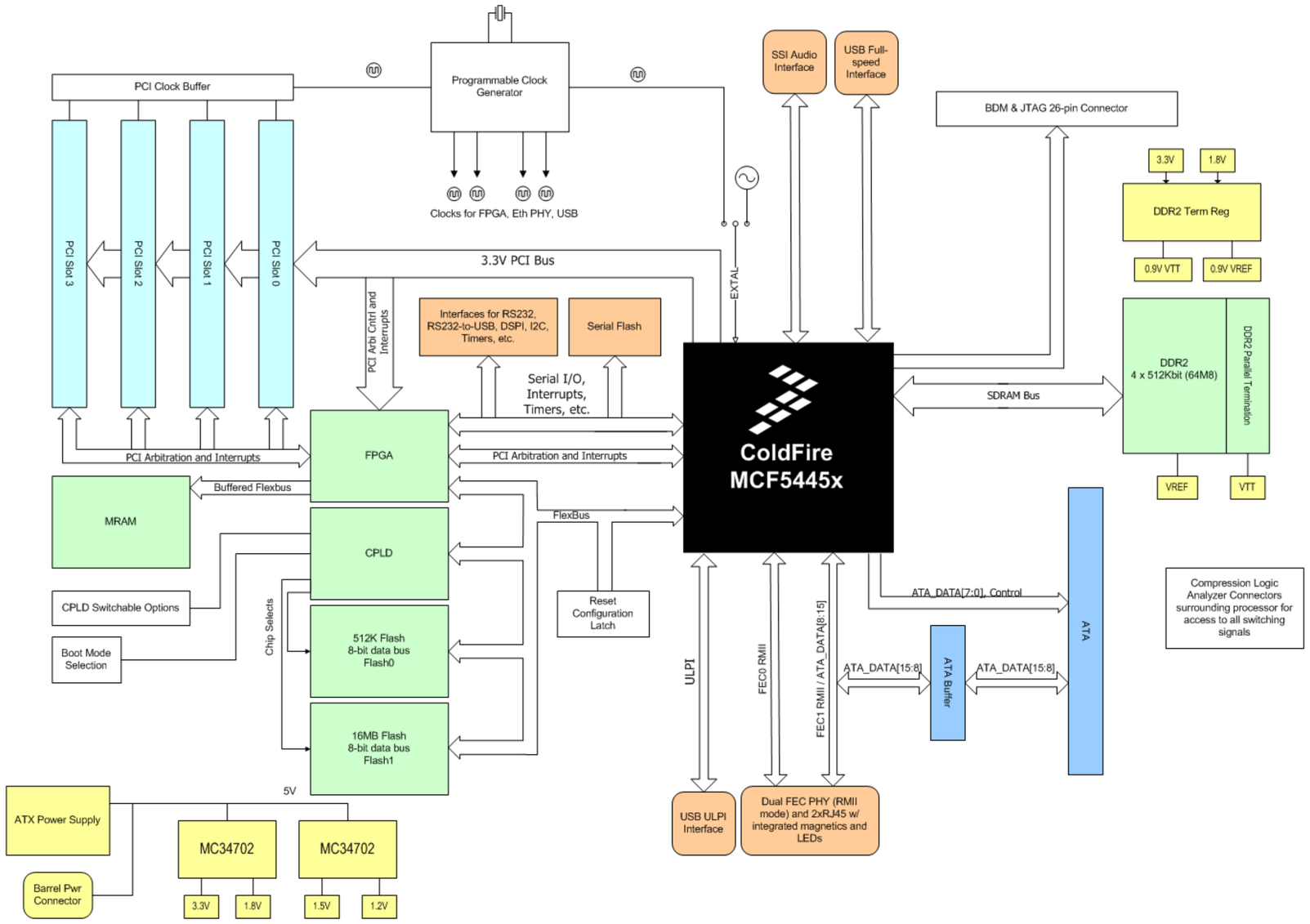
Revisions

Rev	Description	Date	Approved
X1	Original Draft	11/08/06	J.W.
X2	Fixed Flash1, serial port interfaces, etc.	07/03/07	M.N.



freescale semiconductor

Transportation & Standard Products Group
6501 William Cannon Drive West
Austin, TX 78735-8598

Designer: M.Norman & J.Smith	Drawing Title: **M54455EVB**		
Drawn by: DEVTECH CAD - RO	Page Title: **TITLE PAGE**		
Approved: JOHN WEIL	Size C	Document Number PDF: SPF-22131 SOURCE: SCH-22131	Rev B
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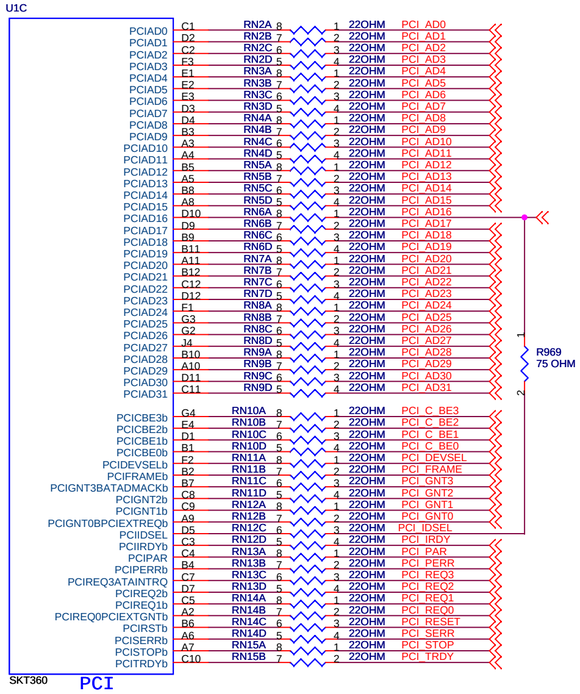
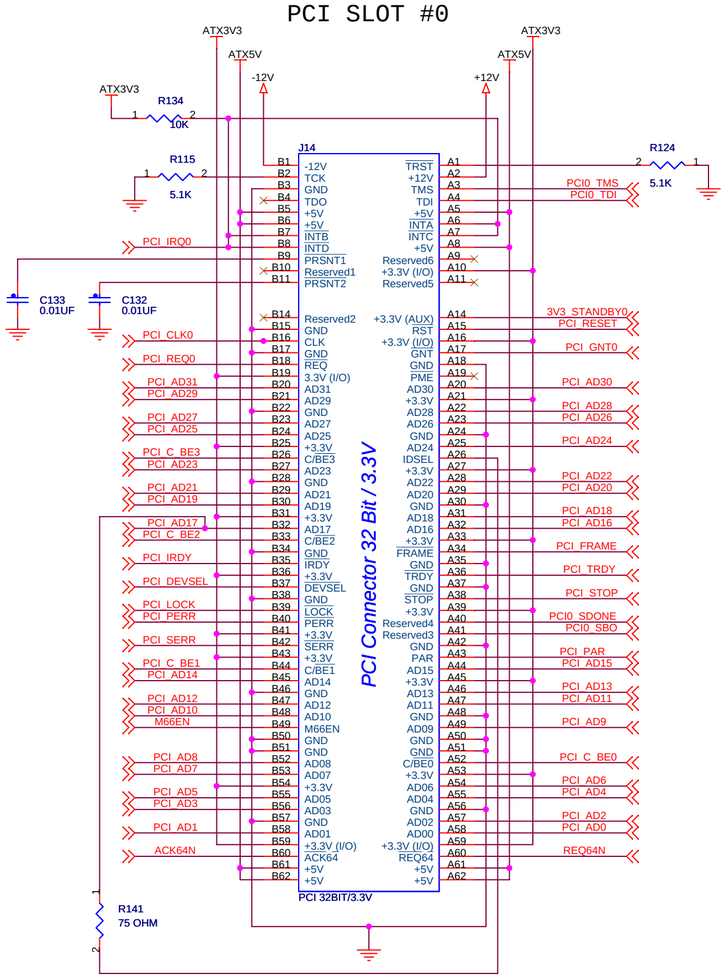
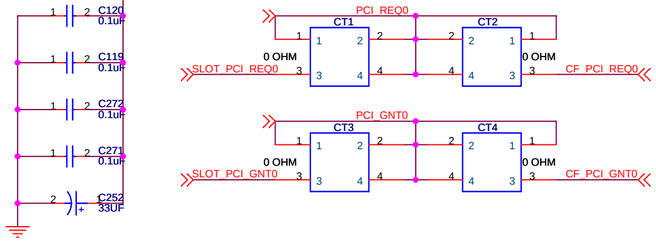
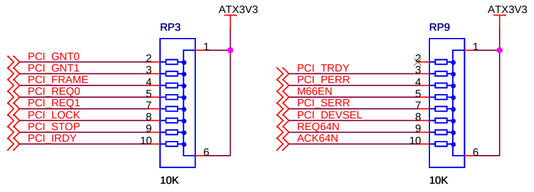
PCI SLOT #0

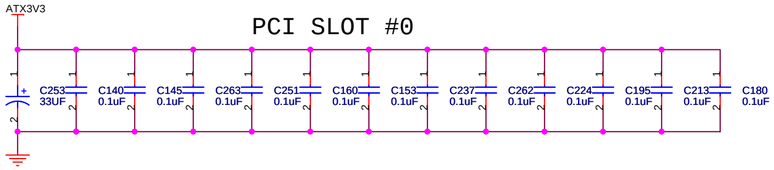


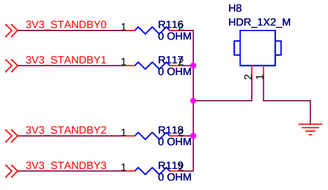


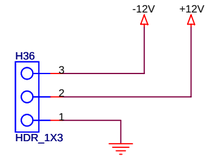
Cut-Trace Options - Slot 0
By default, PCI_REQ0 and PCI_GNT0 routed
directly to PCI Slot 0.
To route through FPGA, cut trace between
1 and 2 on CT1 and solder 1 to 3. Then, cut
trace between 1 and 2 on CT2 and solder
1 to 3. Repeat this process for CT3 and CT4.











The ATX power supply provides
+/- 12V power to the connectors.
This header can be used to monitor
the supply.

PCI Notes:

1. CF_PCI_GNTn and CF_PCI_REQn signals connect to the FPGA. PCI_GNTn and PCI_REQn signals are connected from the FPGA to the PCI slots.

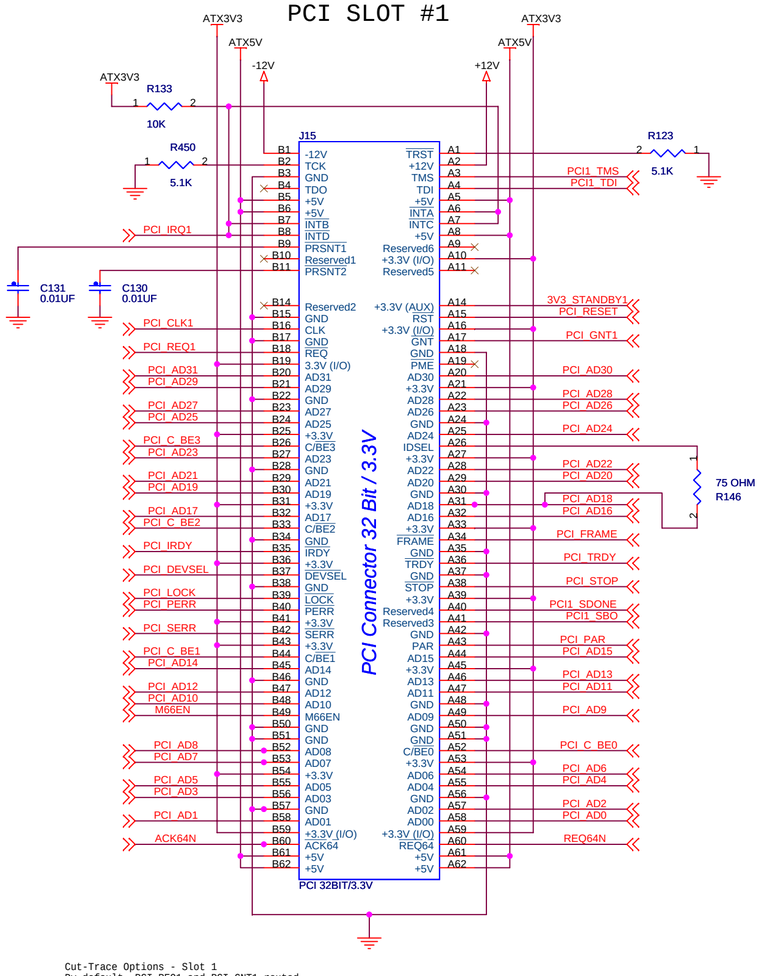
2. PCI Slot #0 uses PCI_REQ0 and PCI_GNT0
   PCI Slot #1 uses PCI_REQ1 and PCI_GNT1
   PCI Slot #2 uses PCI_REQ2 and PCI_GNT2
   PCI Slot #3 uses PCI_REQ3 and PCI_GNT3

3. MCF5445x IDSEL connected to PCI_AD16
   PCI Slot #0 IDSEL connected to PCI_AD17
   PCI Slot #1 IDSEL connected to PCI_AD18
   PCI Slot #2 IDSEL connected to PCI_AD19
   PCI Slot #3 IDSEL connected to PCI_AD20

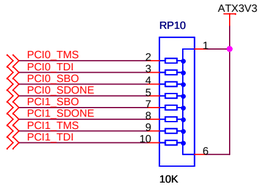
4. The FPGA gathers interrupts from the PCI slots.

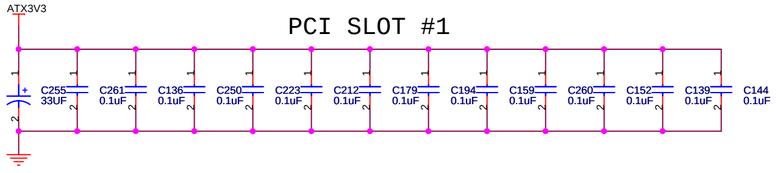
5. JTAG is unusable on PCI connectors

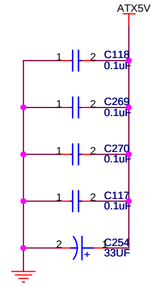
PCI SLOT #1



Cut-Trace Options - Slot 1
By default, PCI_REQ1 and PCI_GNT1 routed
directly to PCI Slot 1 from U1.
To route through FPGA, cut trace between
1 and 2 on CT5 and solder 1 to 3. Then, cut
trace between 1 and 2 on CT6 and solder
1 to 3.







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Page Title: **PCI SLOT #0 AND #1**

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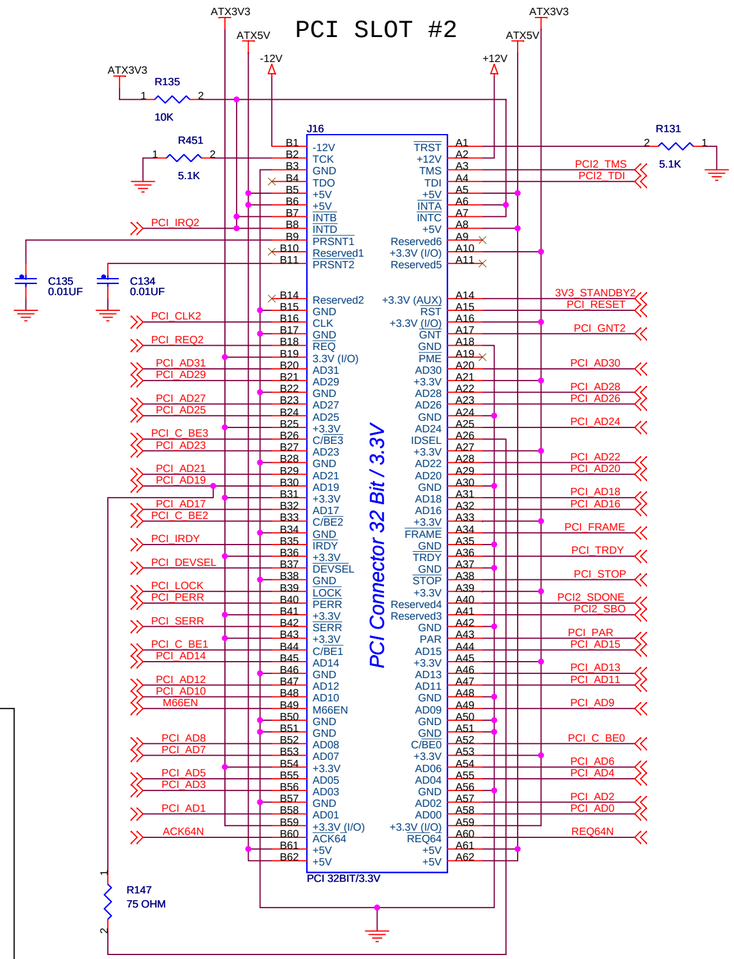
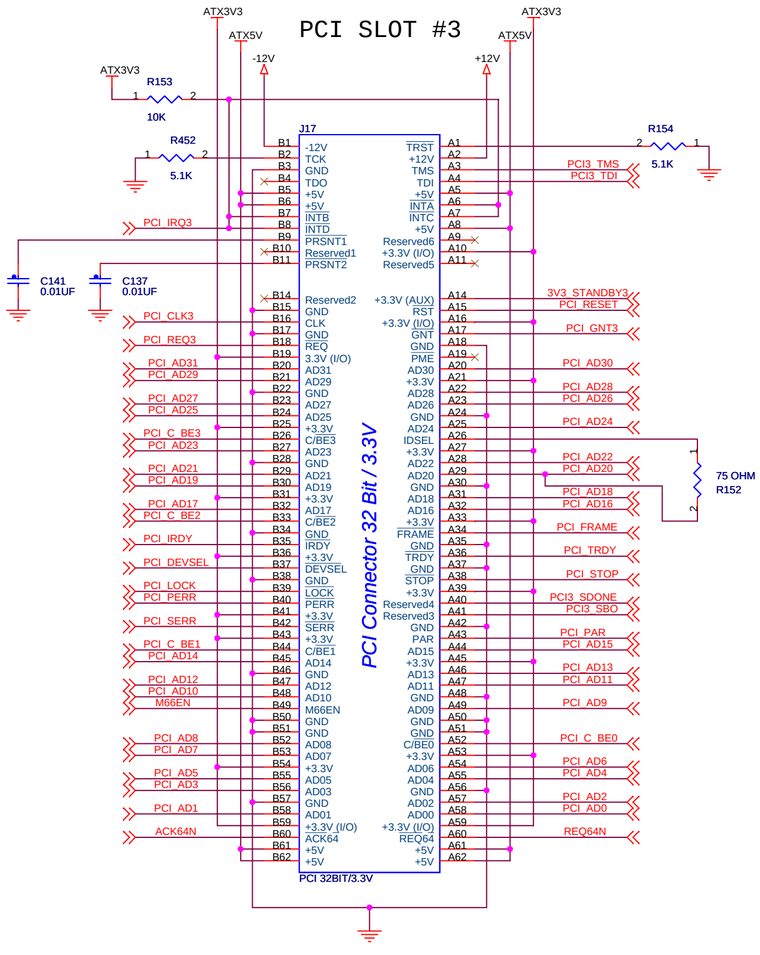




PCI Notes:

1. CF_PCI_GNTn and CF_PCI_REQn signals connect to the FPGA. PCI_GNTn and PCI_REQn signals are connected from the FPGA to the PCI slots.

2. PCI Slot #0 uses PCI_REQ0 and PCI_GNT0
   PCI Slot #1 uses PCI_REQ1 and PCI_GNT1
   PCI Slot #2 uses PCI_REQ2 and PCI_GNT2
   PCI Slot #3 uses PCI_REQ3 and PCI_GNT3

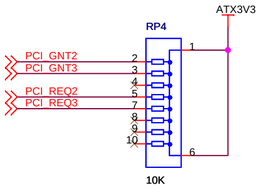
3. MCF5445x IDSEL connected to PCI_AD16
   PCI Slot #0 IDSEL connected to PCI_AD17
   PCI Slot #1 IDSEL connected to PCI_AD18
   PCI Slot #2 IDSEL connected to PCI_AD19
   PCI Slot #3 IDSEL connected to PCI_AD20

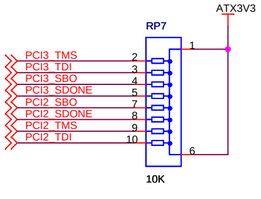
4. The FPGA gathers interrupts from the PCI slots.

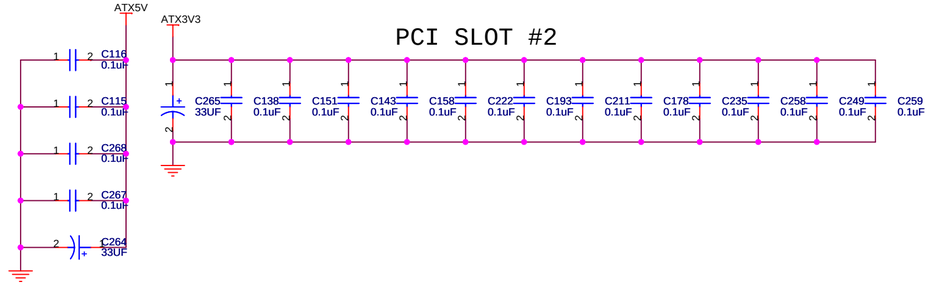
5. JTAG is unusable on PCI connectors

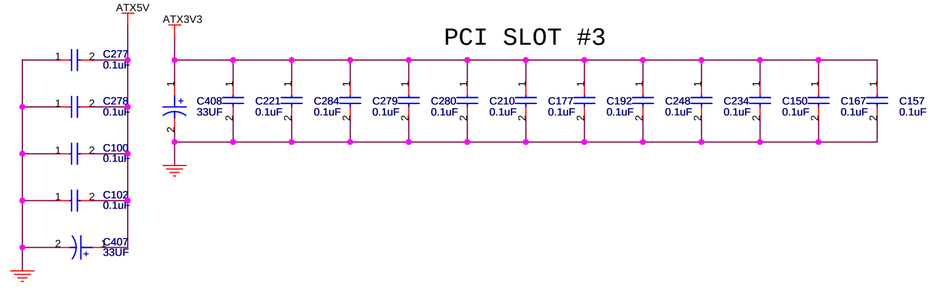
Cut-Trace Options - Slot 2
By default, PCI_REQ2 and PCI_GNT2 routed directly to PCI Slot 2 from U1.
To route through FPGA, cut trace between 1 and 2 on CT7 and solder 1 to 3. Then, cut trace between 1 and 2 on CT8 and solder 1 to 3.

Cut-Trace Options - Slot 3
By default, PCI_REQ3 and PCI_GNT3 routed directly to PCI Slot 3 from U1.
To route through FPGA, cut trace between 1 and 2 on CT9 and solder 1 to 3. Then, cut trace between 1 and 2 on CT10 and solder 1 to 3.









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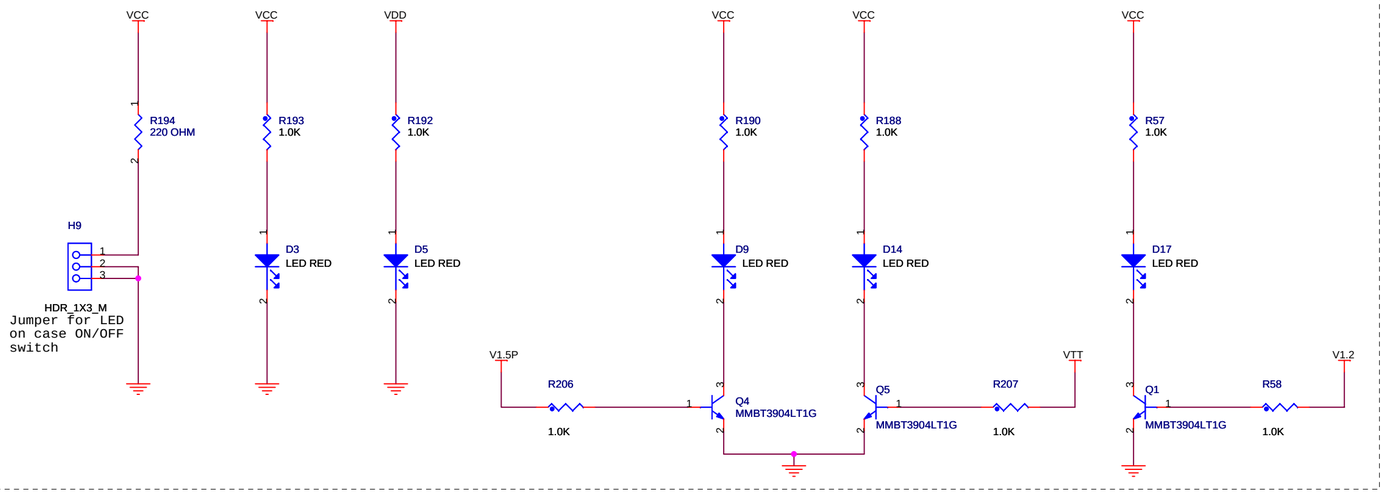
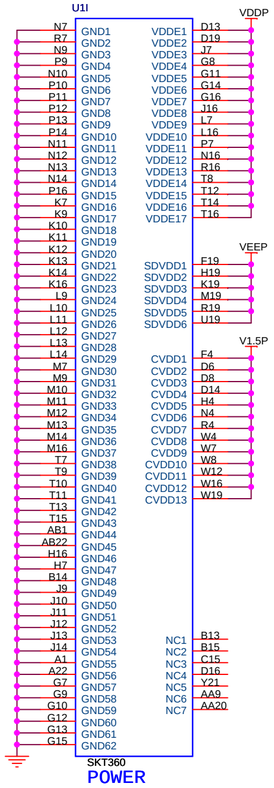
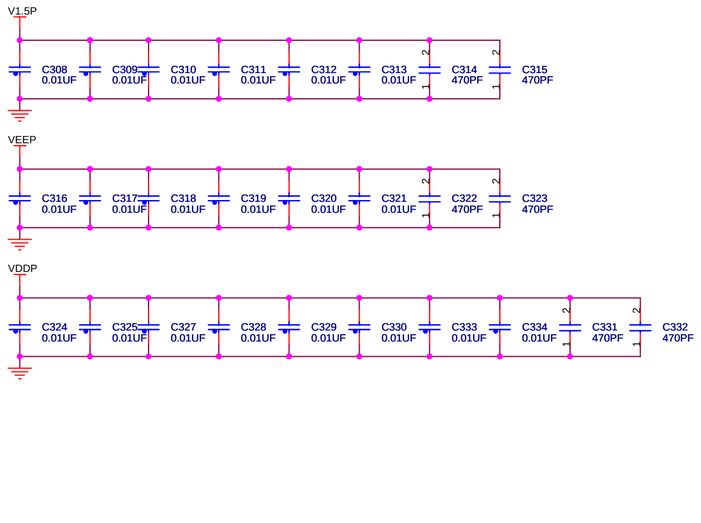
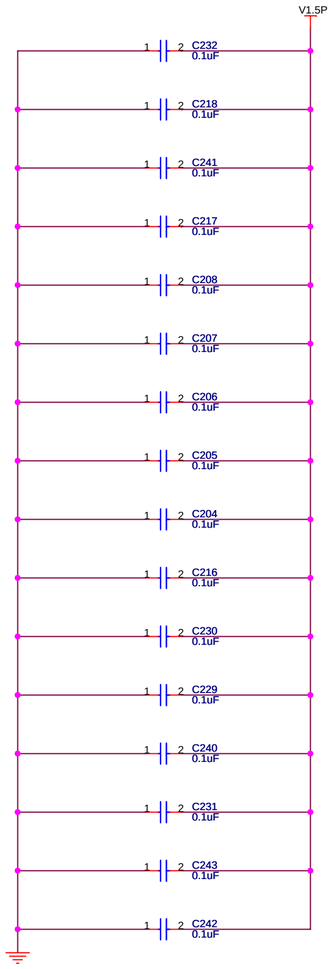
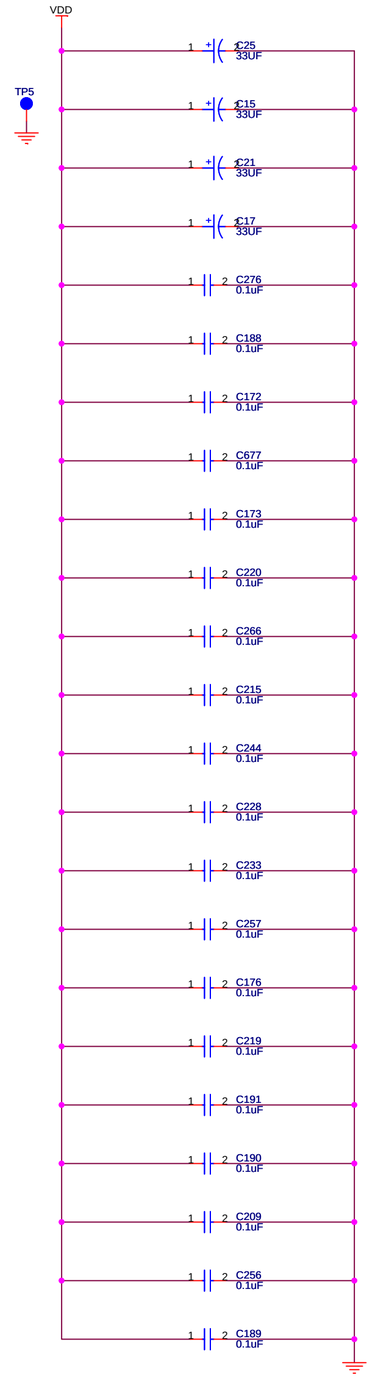
Power Indicators

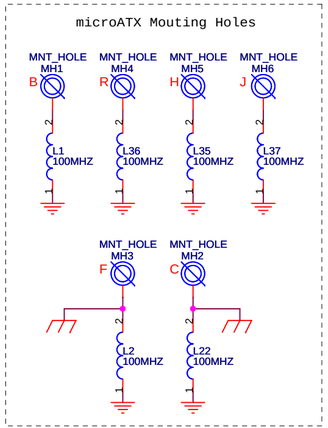












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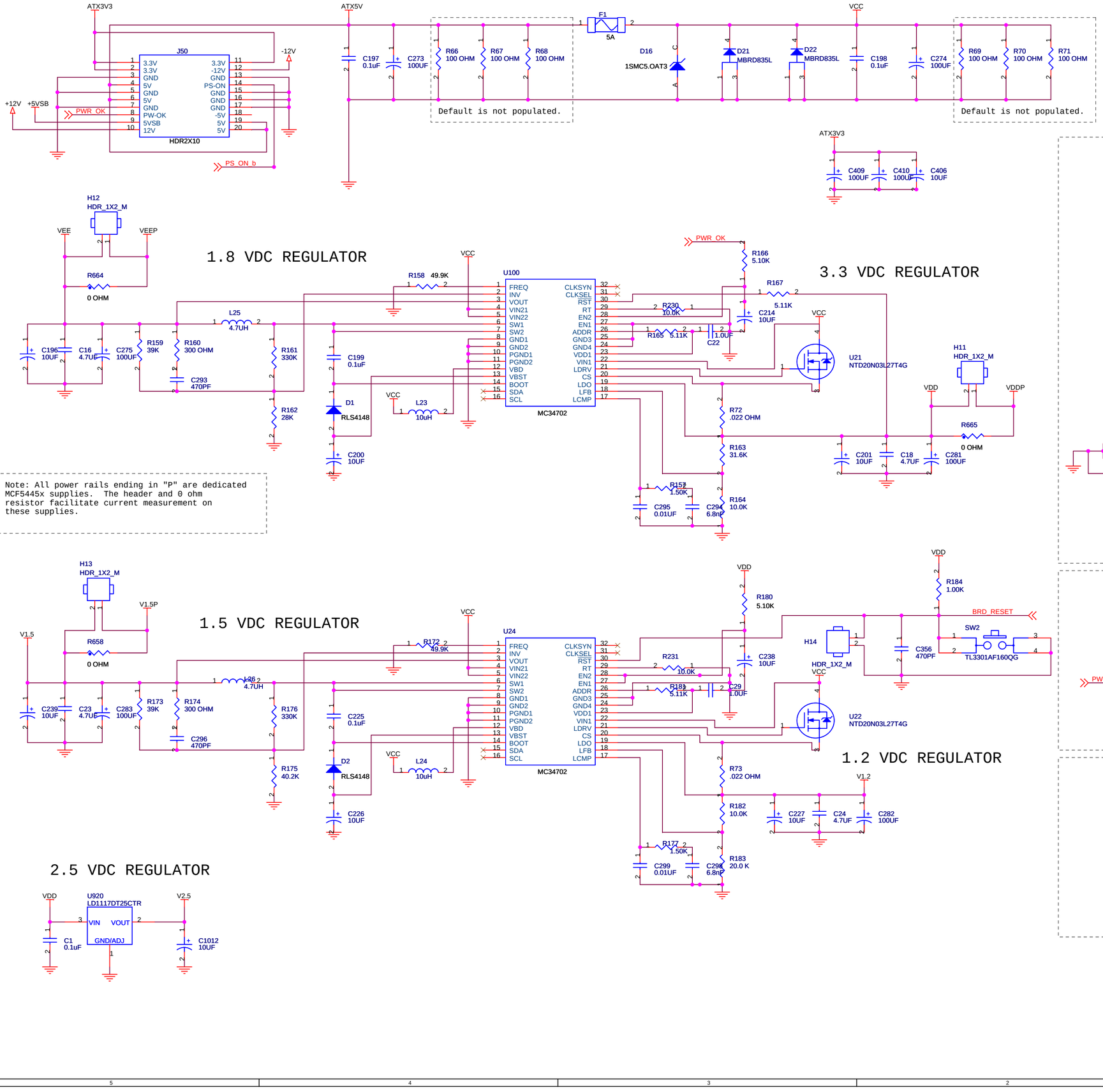

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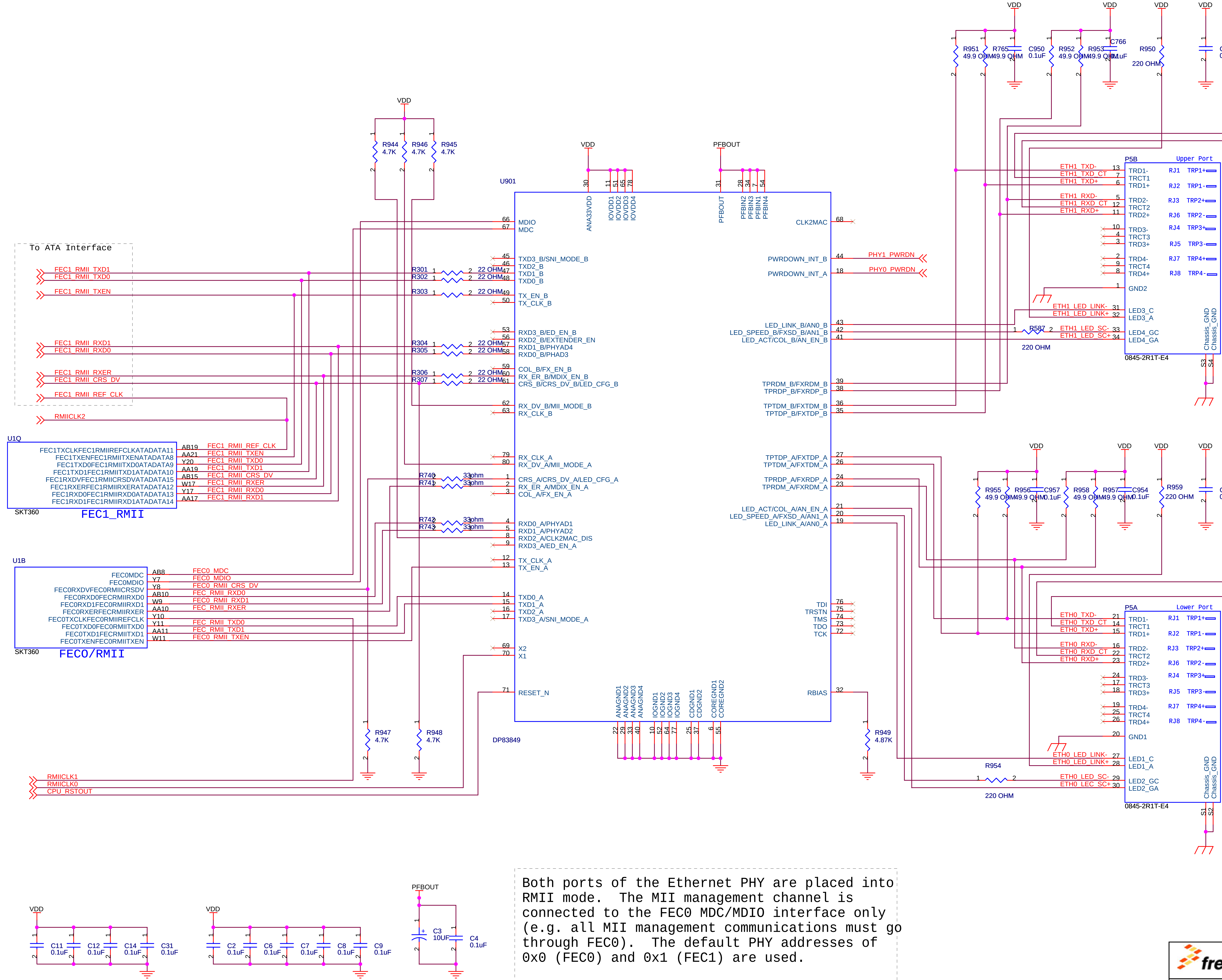

Ethernet Channel 1

LED1 indicates a LINK and blinks for activity.

LED2 indicates Speed (10/100 Mbps) and Collision (when in 10 Mbps mode). LED2 is GREEN for 100Mbps mode, OFF for 10Mbps, and blinking ORANGE for Collisions.

Ethernet Channel 0

LED1 indicates a LINK and blinks for activity.

LED2 indicates Speed (10/100 Mbps) and Collision (when in 10 Mbps mode). LED2 is GREEN for 100Mbps mode, OFF for 10Mbps, and blinking ORANGE for Collisions.

Both ports of the Ethernet PHY are placed into RMII mode. The MII management channel is connected to the FEC0 MDC/MDIO interface only (e.g. all MII management communications must go through FEC0). The default PHY addresses of 0x0 (FEC0) and 0x1 (FEC1) are used.

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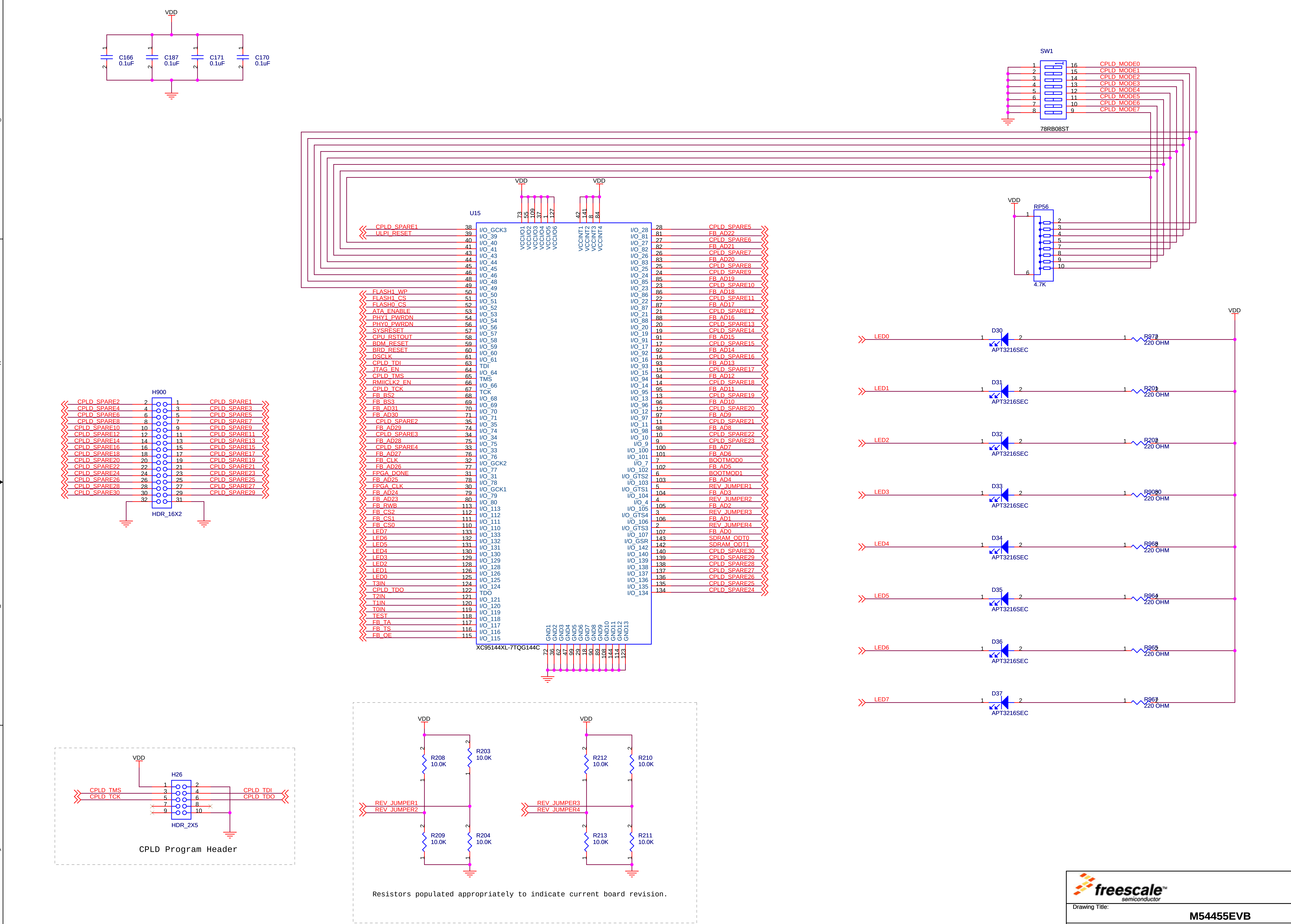

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Drawing Title: **M54455EVB**

Page Title: **CPLD**

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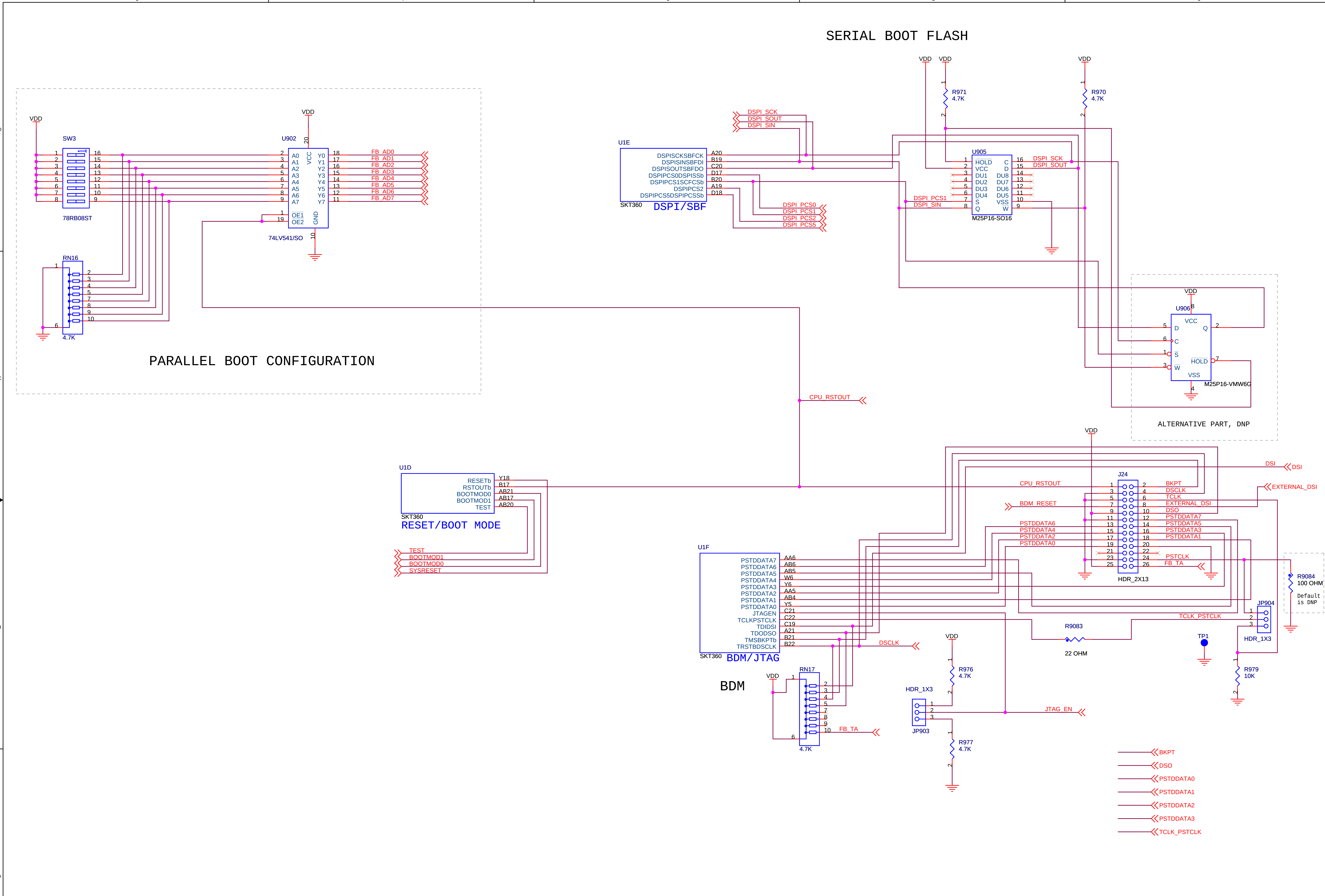

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Drawing Title: **M54455EVB**

Page Title: **BOOT, SBF & BDM**

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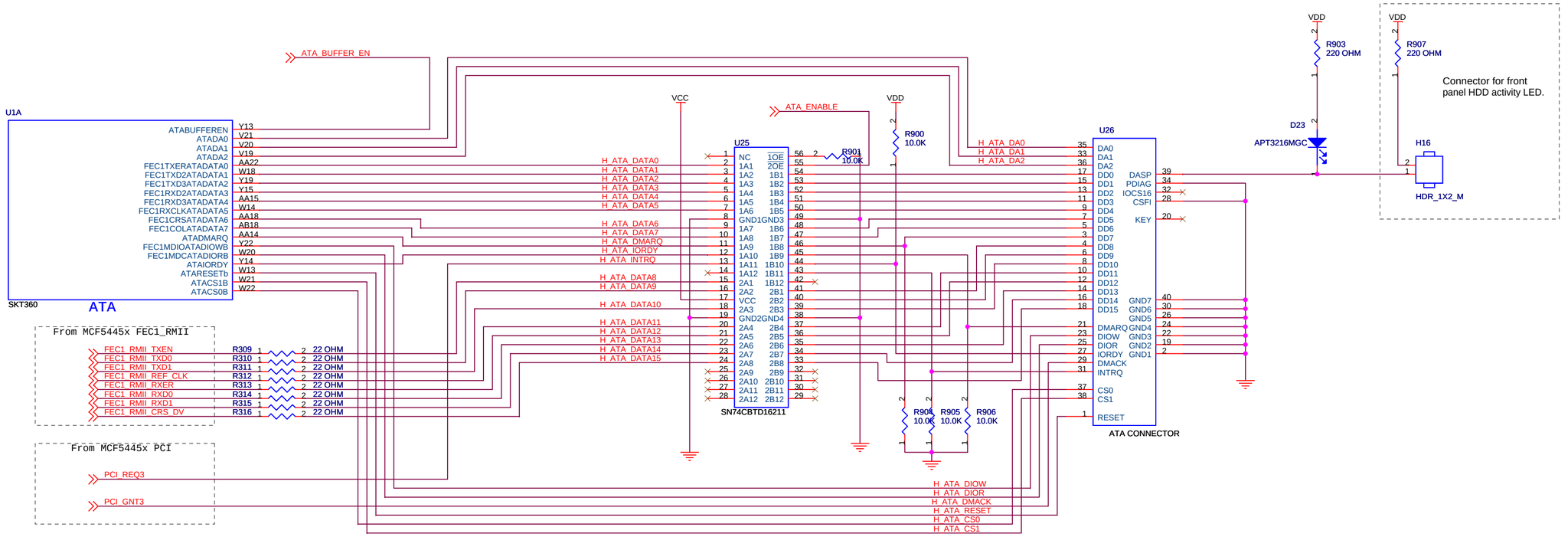

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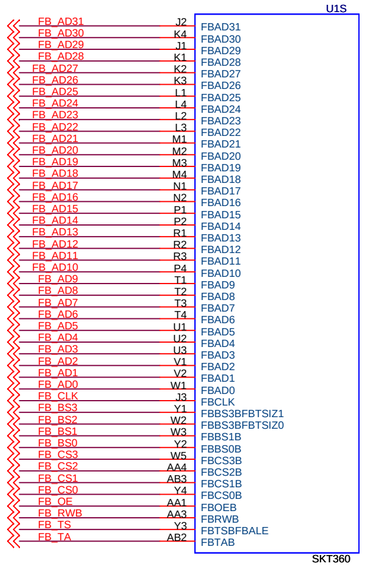
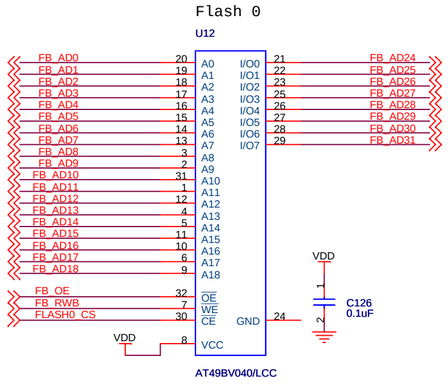
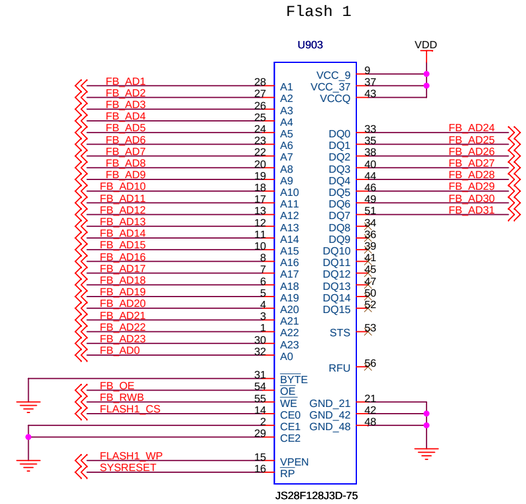
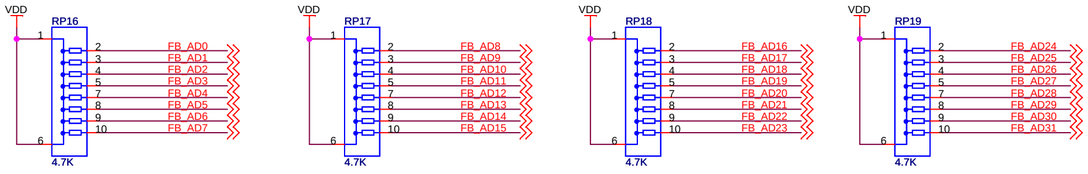
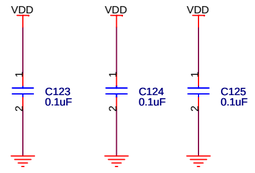






The CPLD_MODE[2] setting determines which flash device gets which chip-select (FB_CS0 or FB_CS1). The device connected to FB_CS0 is the boot device.





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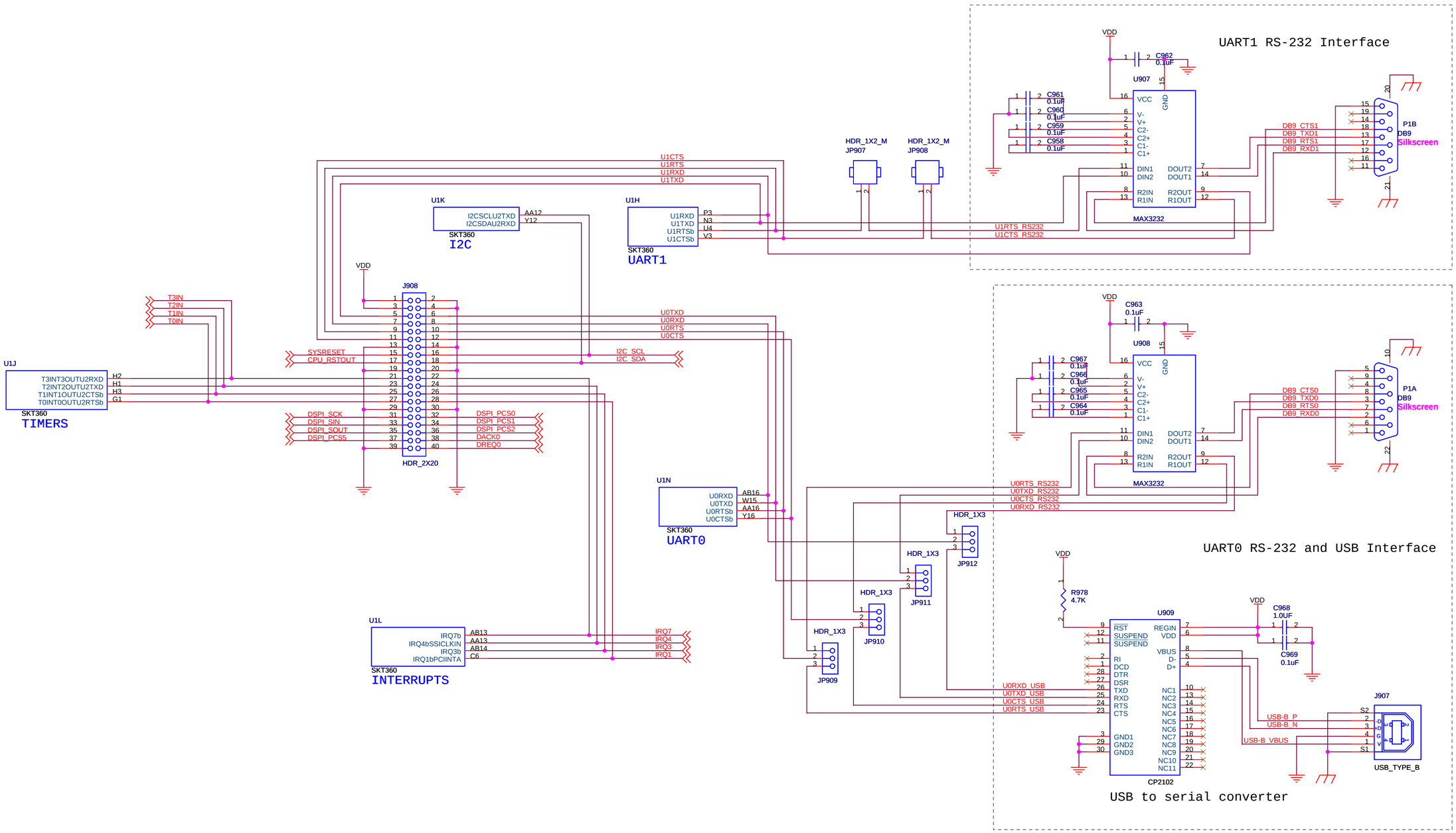

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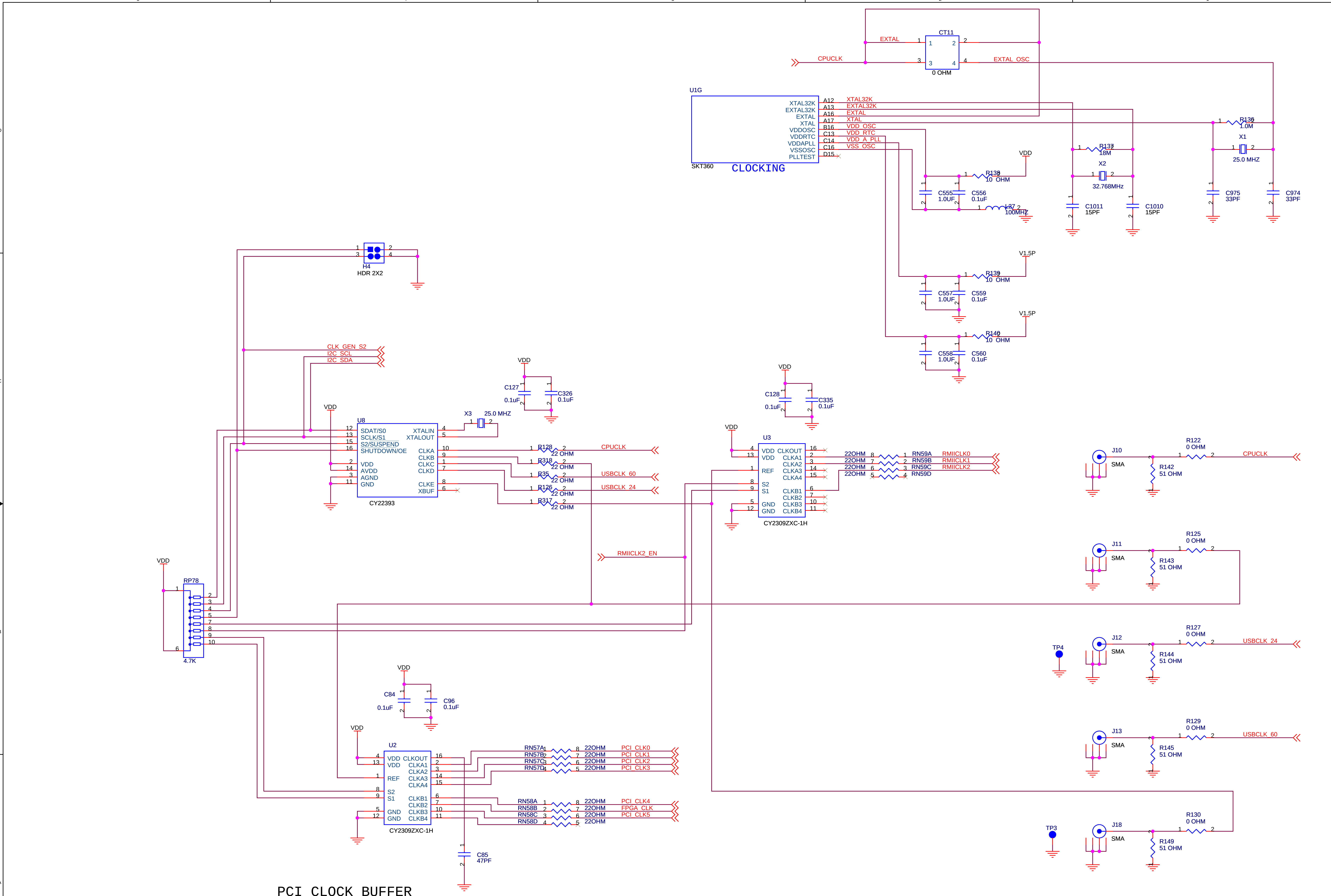
CT11
0 OHM
EXTAL
CPUCLK
EXTAL_OSC
U1G
XTAL32K
EXTAL32K
EXTAL
XTAL
VDDOSC
VDDRTC
VDDAPLL
VSSOSC
PLLTEST
SKT360
CLOCKING
A12
A13
A16
A17
B16
C13
C14
C16
D15
VDD_OSC
VDD_RTC
VDD_A_PLL
VSS_OSC
R136
1.0M
X1
25.0 MHZ
R137
18M
X2
32.768MHz
R138
10 OHM
VDD
C555
1.0UF
C556
0.1uF
L37
100MHZ
C1011
15PF
C1010
15PF
C975
33PF
C974
33PF
V1.5P
R139
10 OHM
C557
1.0UF
C559
0.1uF
R140
10 OHM
C558
1.0UF
C560
0.1uF
H4
HDR 2X2
CLK_GEN_S2
I2C_SCL
I2C_SDA
C127
0.1uF
C326
0.1uF
X3
25.0 MHZ
U8
SDAT/S0
SCLK/S1
S2/SUSPEND
SHUTDOWN/OE
VDD
AVDD
AGND
GND
XTALIN
XTALOUT
CLKA
CLKB
CLKC
CLKD
CLKE
XBUF
CY22393
R128
22 OHM
R318
22 OHM
R35
22 OHM
R126
22 OHM
R317
22 OHM
USBCLK_60
USBCLK_24
C128
0.1uF
C335
0.1uF
U3
CLKOUT
CLKA1
CLKA2
CLKA3
CLKA4
REF
S2
S1
CLKB1
CLKB2
CLKB3
CLKB4
CY2309ZXC-1H
22OHM
RN59A
RN59B
RN59C
RN59D
RMIICLK0
RMIICLK1
RMIICLK2
RMIICLK2_EN
J10
SMA
R122
0 OHM
R142
51 OHM
J11
R125
0 OHM
R143
51 OHM
J12
R127
0 OHM
R144
51 OHM
TP4
J13
R129
0 OHM
R145
51 OHM
J18
R130
0 OHM
R149
51 OHM
TP3
RP78
4.7K
C84
0.1uF
C96
0.1uF
U2
RN57A
RN57B
RN57C
RN57D
PCI_CLK0
PCI_CLK1
PCI_CLK2
PCI_CLK3
RN58A
RN58B
RN58C
RN58D
PCI_CLK4
FPGA_CLK
PCI_CLK5
C85
47PF
PCI CLOCK BUFFER

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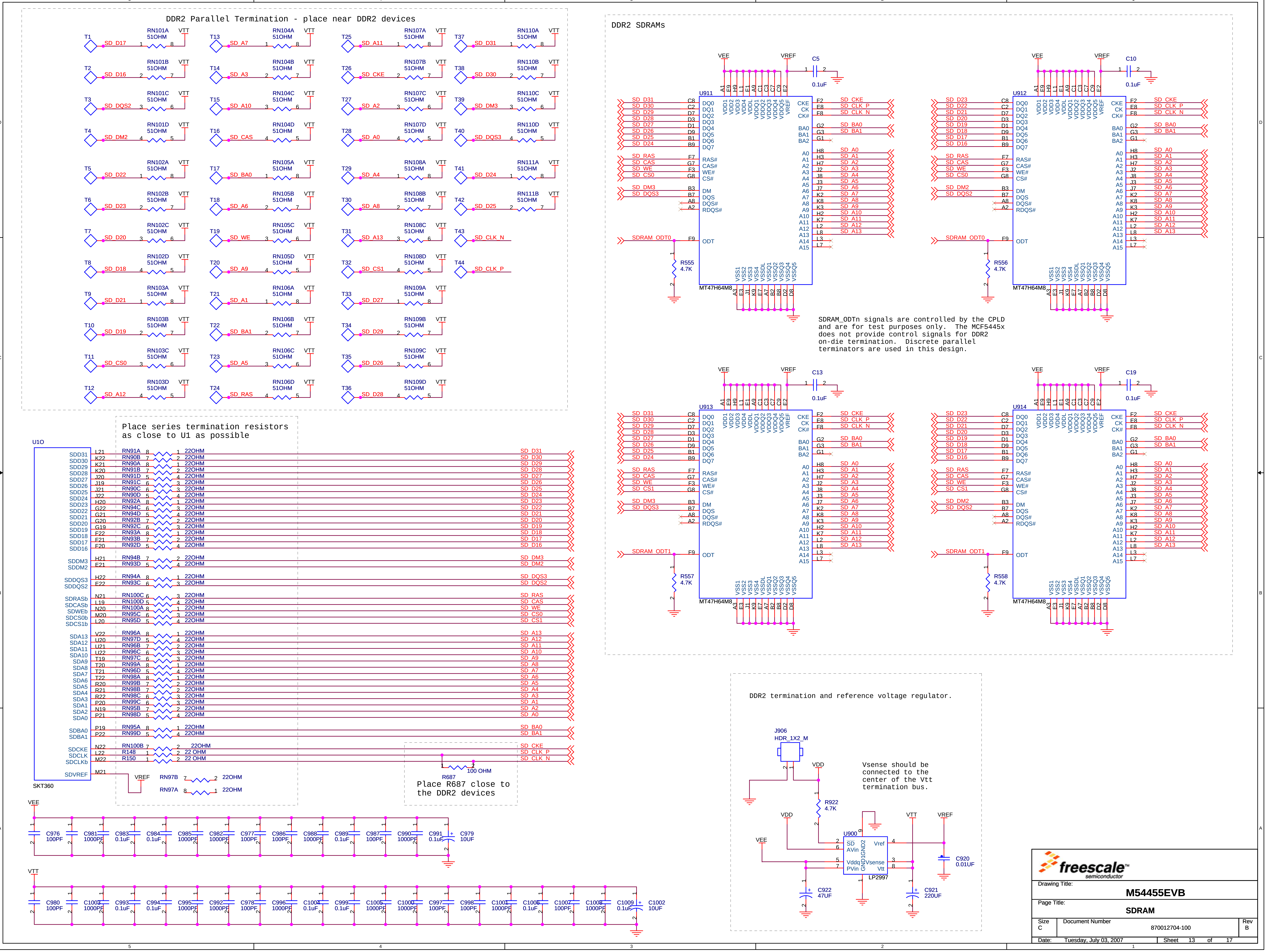
DDR2 Parallel Termination - place near DDR2 devices
DDR2 SDRAMs
SDRAM_ODTn signals are controlled by the CPLD and are for test purposes only. The MCF5445x does not provide control signals for DDR2 on-die termination. Discrete parallel terminators are used in this design.
Place series termination resistors as close to U1 as possible
Place R687 close to the DDR2 devices
DDR2 termination and reference voltage regulator.
Vsense should be connected to the center of the Vtt termination bus.
U911
U912
U913
U914
MT47H64M8
U1O
SKT360
U900
LP2997
J906
HDR_1X2_M
freescale semiconductor
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SDRAM
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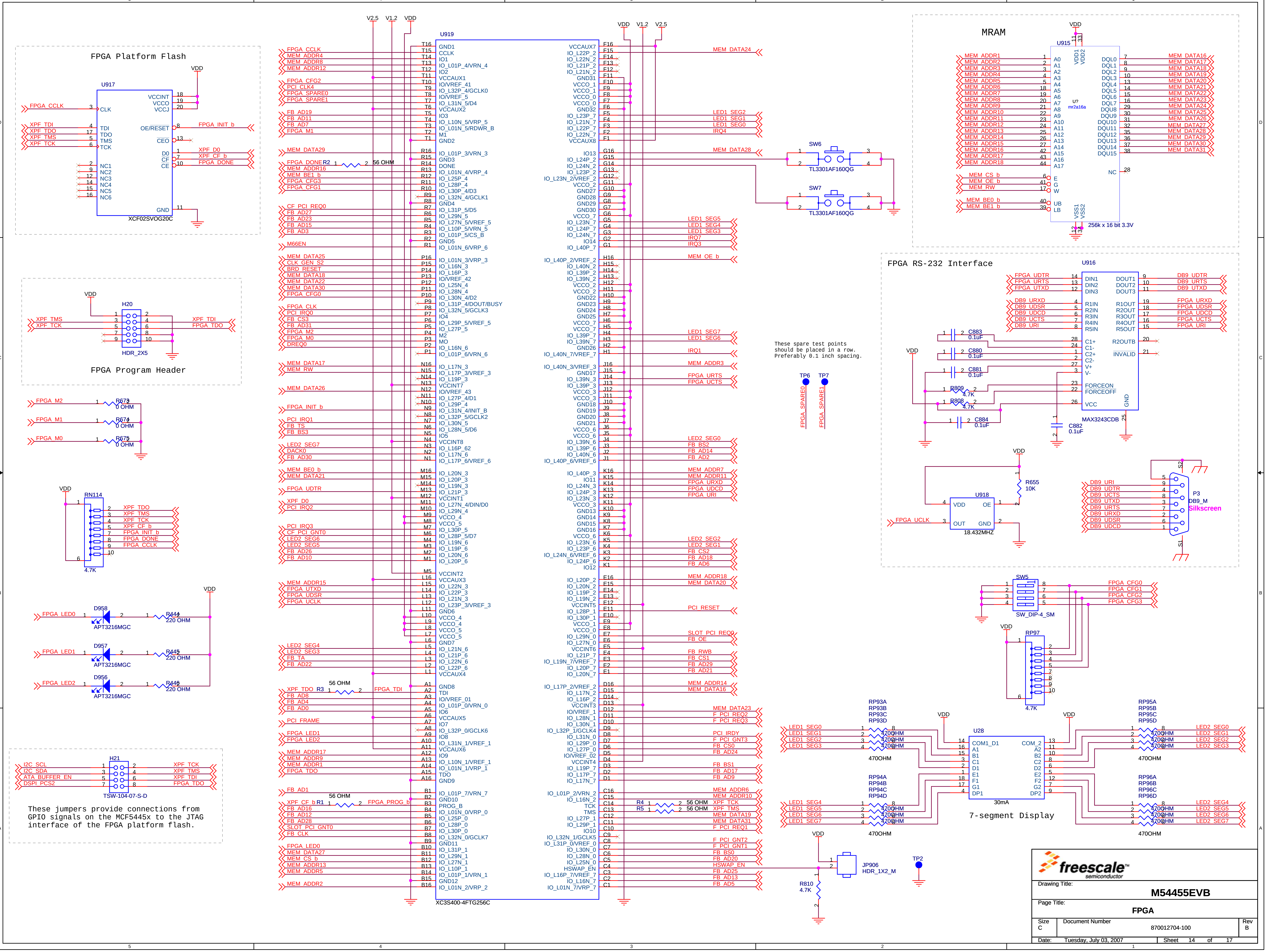

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Page Title: FPGA

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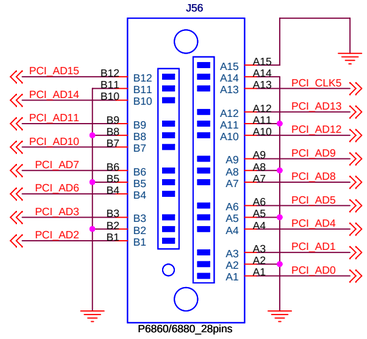
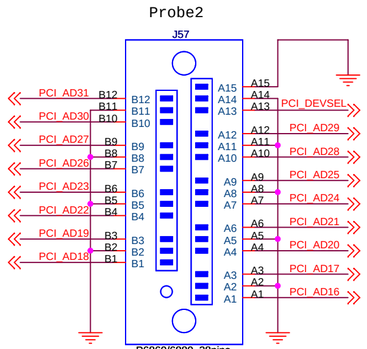
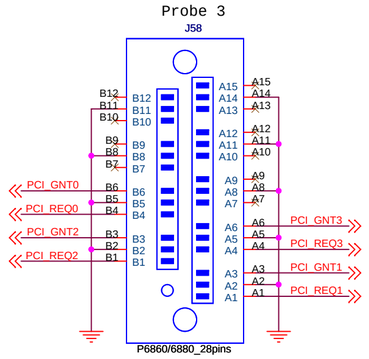
Probe 1



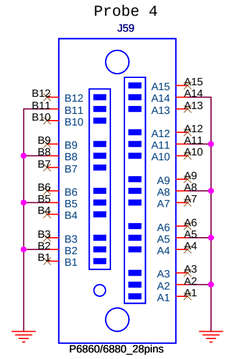
Probe2



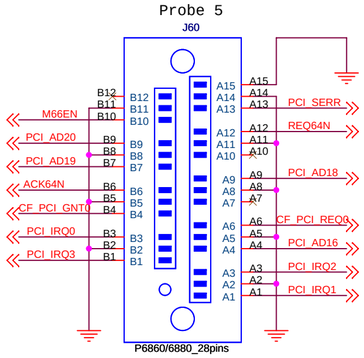
Probe 3



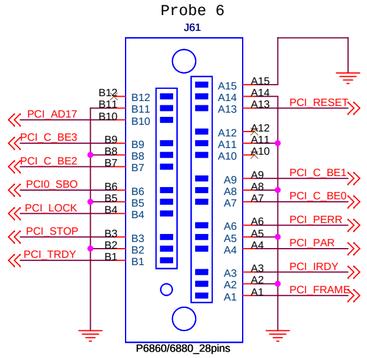
Probe 4



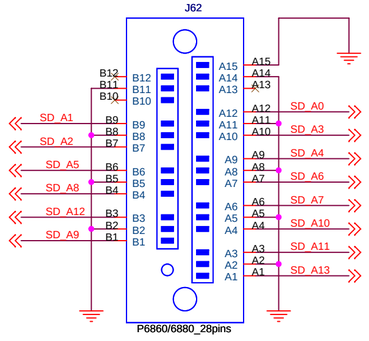
Probe 5



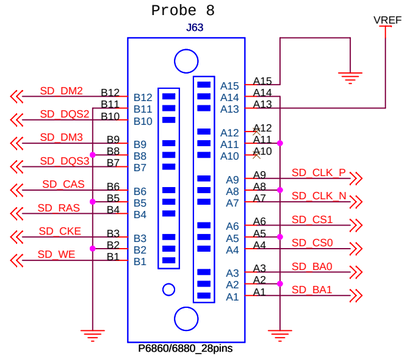
Probe 6



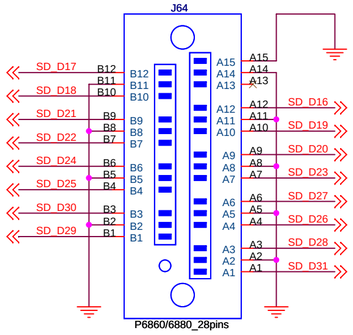
Probe 7



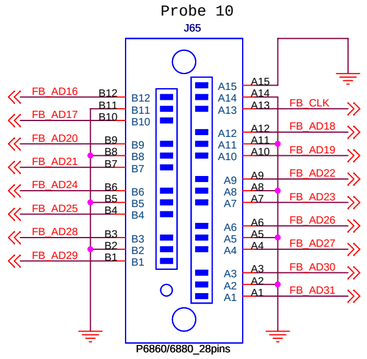
Probe 8



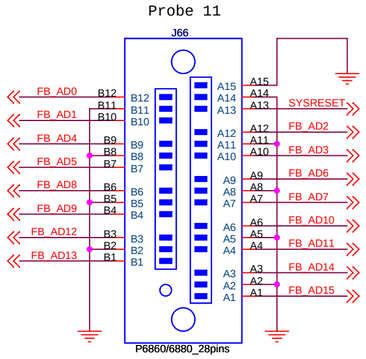
Probe 9



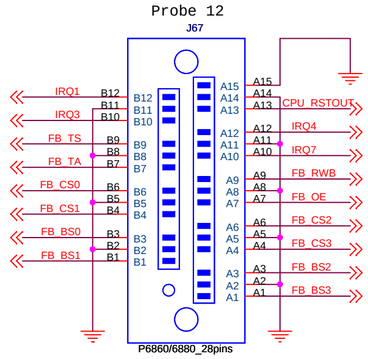
Probe 10



Probe 11



Probe 12



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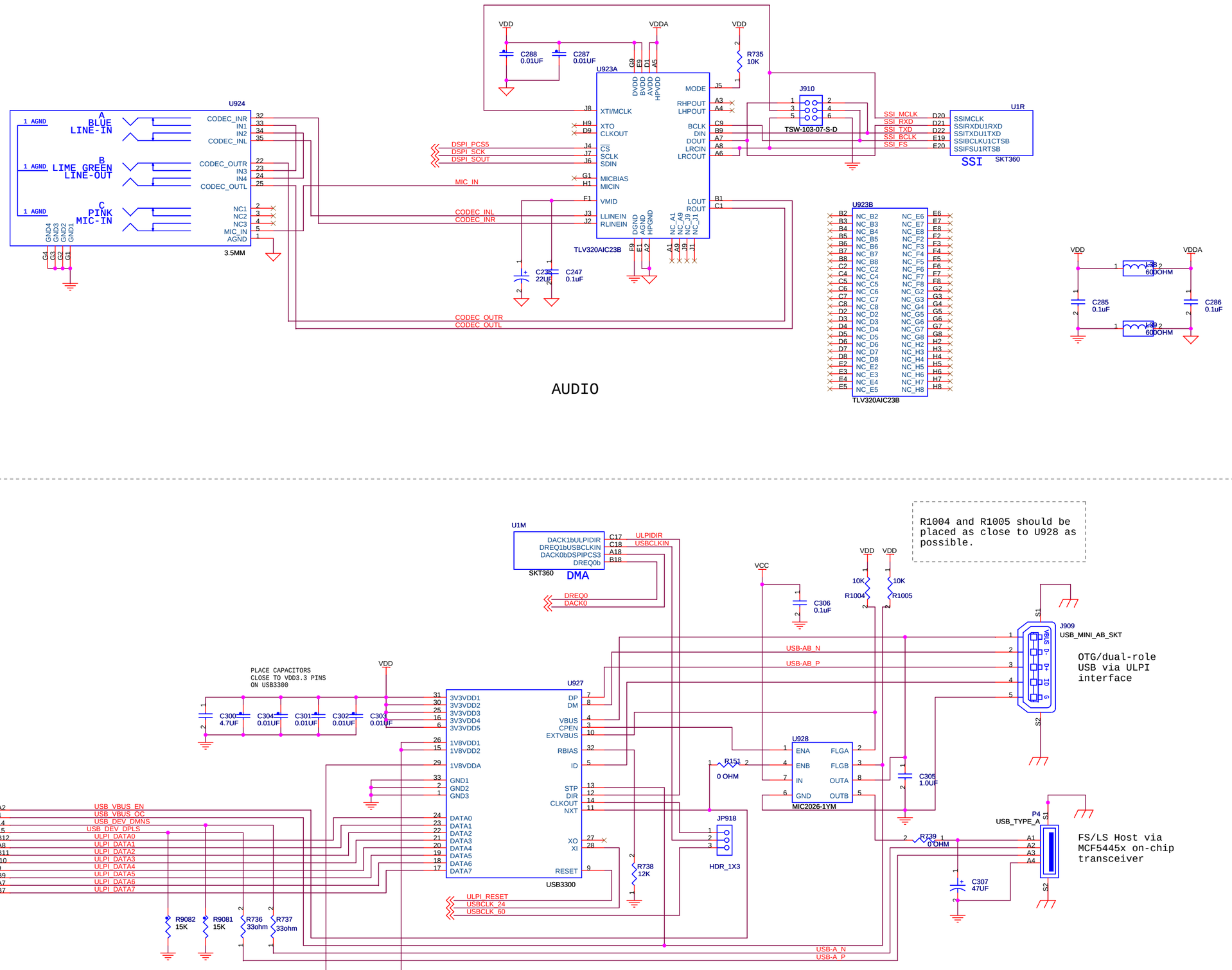

Layout Notes:
* The required 33 ohm series source termination resistors should be placed as closely to the USB_DEV_DMNS and USB_DEV_DPLS outputs as possible.
* Route D- and D+ signals on the top or bottom layer of the board keeping them as short as possible with a minimum amount of vias and corners.
* Use 45deg turns instead of 90deg turns.
* The trace width and spacing of the D- and D+ signals should be such that the differential impedance is 90 Ohms.
* Maintain the parallelism (skew matching) between D- and D+. These traces should be the same overall length.

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P&E Microcomputer Systems
USB ColdFire Multilink BDM Interface

CF_RESET — BDM_RESET

CF_TEA — FB_TA

CF_DSO — DSO

CF_FREEZE — TCLK_PSTCLK

CF_DSCLK — DSCLK

CF_BKPT — BKPT

PST0 — PSTDDATA0

PST1 — PSTDDATA1

PST2 — PSTDDATA2

PST3 — PSTDDATA3

CF_DSI — DSI

EXTERNAL_DSI — EXTERNAL_DSI

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Drawing Title:
P&E CONFIDENTIAL INFORMATION

Page Title:
USB TO BDM COLDFIRE REFERENCE DESIGN

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