PROGRAMMABLE ASIC I/O CELLS

6

Key concepts:

Input/output cell (I/O cell) • I/O requirements • DC output • AC output • DC input • AC input • Clock input • Power input

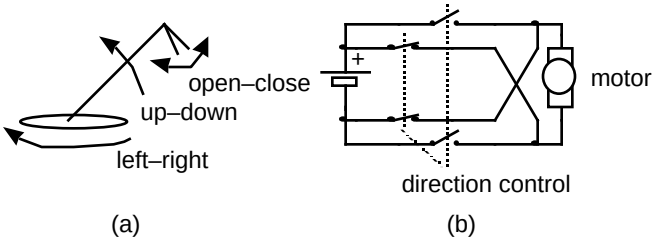
6.1 DC Output

A robot arm example

To design a system work from the outputs back to the inputs

(a) Three small DC motors drive the arm

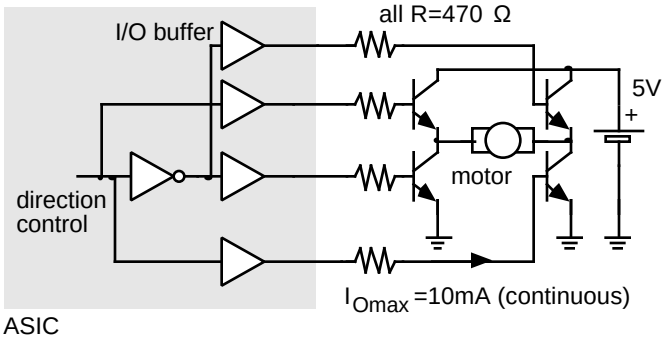
(b) Switches control each motor

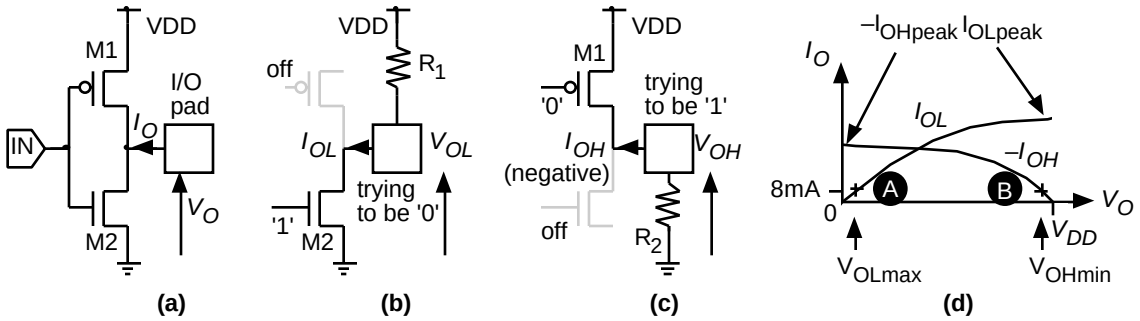


A circuit to drive a small electric motor (0.5A) using ASIC I/O buffers

Work from the outputs to the inputs

The 470Ω resistors drop up to 5V if an output buffer current approaches 10mA, reducing the drive to the output transistors





CMOS output buffer characteristics

(a) A CMOS complementary output buffer

(b) Transistor M2 (M1 off) sinks (to GND) a current I_{OL} through a pull-up resistor, R_1

(c) Transistor M1 (M2 off) sources (from VDD) a current $-I_{OH}$ (I_{OH} is negative) through a pull-down resistor, R_2

(d) Output characteristics:

• Data books specify characteristics at two points, A (V_{OHmin}, I_{OHmax}) and B (V_{OLmax}, I_{OLmax})

Example (Xilinx XC5200):

V_{OLmax}=0.4V, **low-level output voltage** at I_{OLmax}=8.0mA

V_{OHmin}=4.0V, **high-level output voltage** at I_{OHmax}=–8.0mA

• **Output current**, I_O, is positive if it flows into the output

• Input current, if there is any, is positive if it flows into the input

• Output buffer can force the output pad to 0.4V or lower and **sink** no more than 8mA

• When the output is 4V, the buffer can **source** 8mA

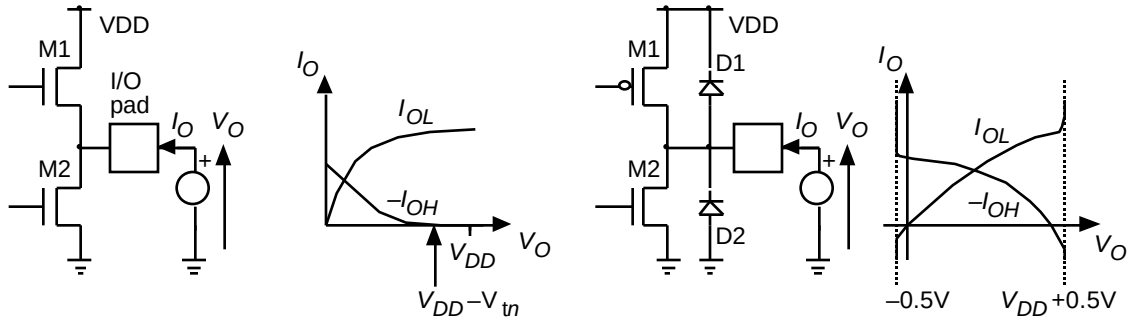
• Specifying only V_{OLmax}=0.4V and V_{OHmin}=4.0V for a technology is strictly incorrect

• We do not know the value of I_{OLpeak} or I_{OHpeak} (typical values are 50–200mA)

6.1.1 Totem-Pole Output

Keywords: totem-pole output buffer • similar to TTL totem-pole output • two n-channel transistors in a stack • reduced output voltage swing

6.1.2 Clamp Diodes



(a) **(b)** **(c)** **(d)**

Output buffer characteristics

(a) A CMOS totem-pole output stage (both M1 and M2 are n-channel transistors)

(b) Totem-pole output characteristics (notice the reduced signal swing)

(c) Clamp diodes, D1 and D2, in an output buffer (totem-pole or complementary) prevent the I/O pad from voltage excursions greater than V_{DD} and less than V_{SS}

(d) The clamp diodes conduct as the output voltage exceeds the supply voltage bounds

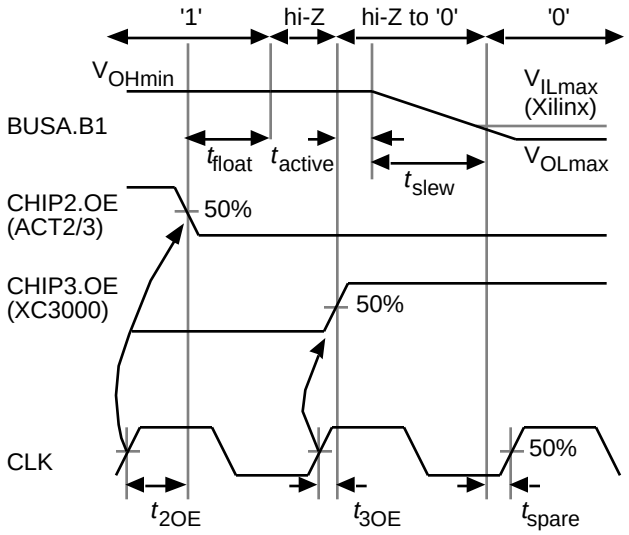
6.2 AC Output

Keywords: bus transceivers • bus transaction (a sequence of signals on a bus) • floating a bus • bus keeper • trip points • three-stated (high-impedance or hi-Z) • time to float • disable time, time to begin hi-Z, or time to turn off • slew • sustained three-state (s/t/s) • turnaround cycle

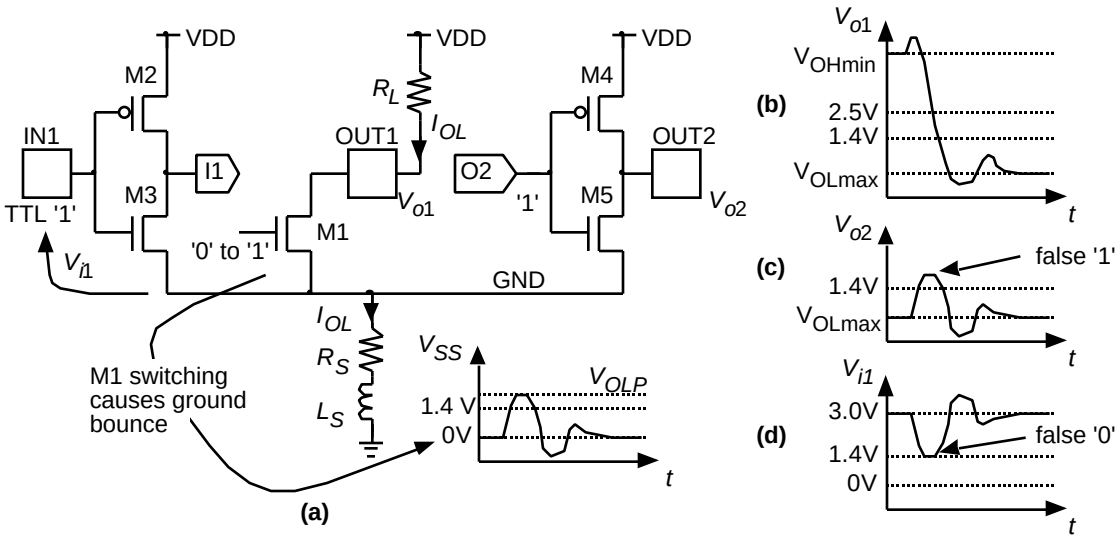
Three-state bus timing

The on-chip delays, t_{2OE} and t_{3OE}, for the logic that generates signals CHIP2.E1 and CHIP3.E1 are derived from the timing models

(The minimum values for each chip would be the clock-to-Q delay times)



6.2.1 Supply Bounce



Supply bounce

A substantial current I_{OL} may flow in the resistance, R_S, and inductance, L_S, that are between the on-chip GND net and the off-chip, external ground connection

(a) As the pull-down device, M1, switches, it causes the GND net (value V_{SS}) to **bounce**

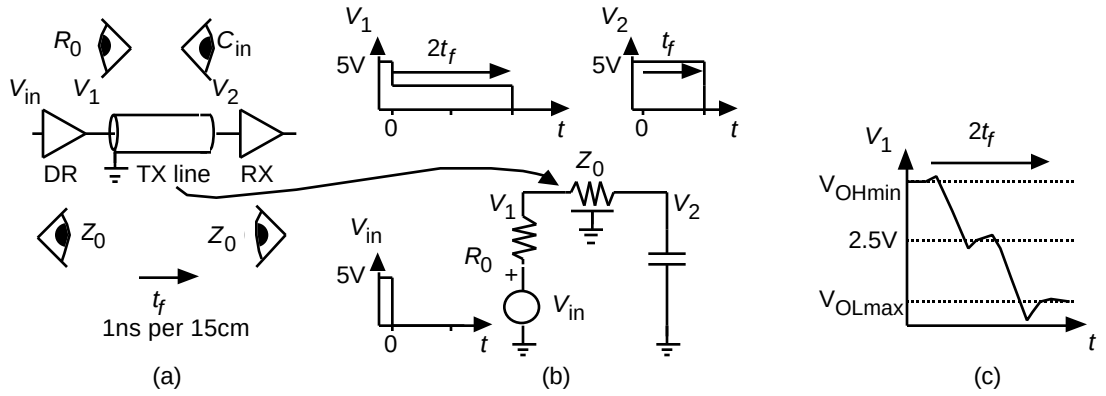
(b) The **supply bounce** is dependent on the output slew rate

(c) Ground bounce can cause other output buffers to generate a **logic glitch**

(d) Bounce can also cause errors on other inputs

Keywords: simultaneously-switching outputs (SSOs) • quiet I/O • slew-rate control • I/O management • packaging • PCB layout • ground planes • inductance

6.2.2 Transmission Lines



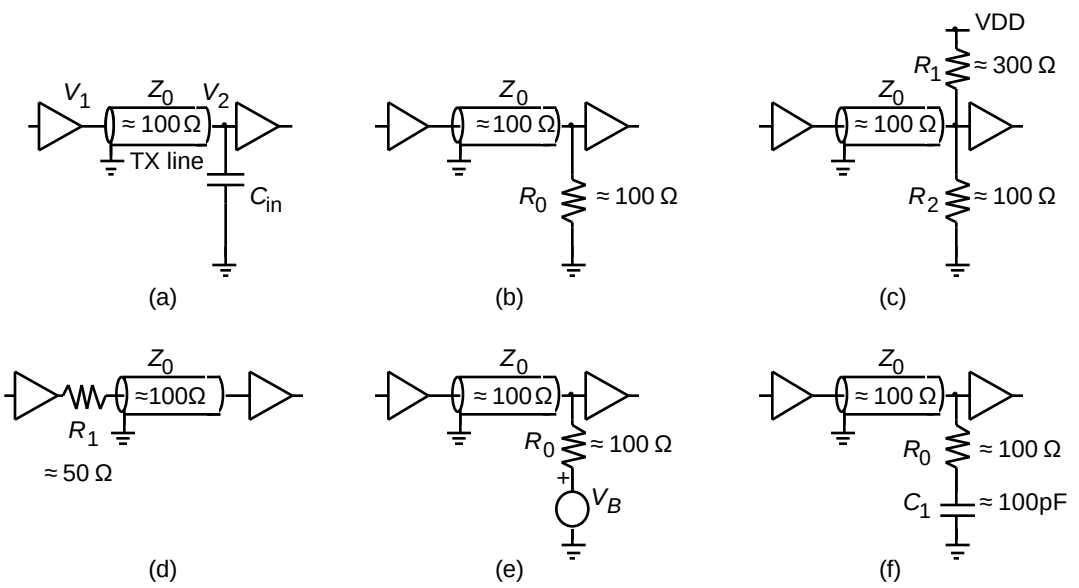
Transmission lines

(a) A printed-circuit board (PCB) trace is a transmission (TX) line (Z_0 = 50Ω–100Ω)

(b) A driver launches an incident wave, which is reflected at the end of the line

(c) A connection starts to look like a TX line when the rise time is about 2 × line delay ($2t_f$)

6.3 DC Input



Transmission line termination

(a) Open-circuit or capacitive termination

(b) Parallel resistive termination

(c) Thévenin termination

(d) Series termination at the source

(e) Parallel termination using a voltage bias

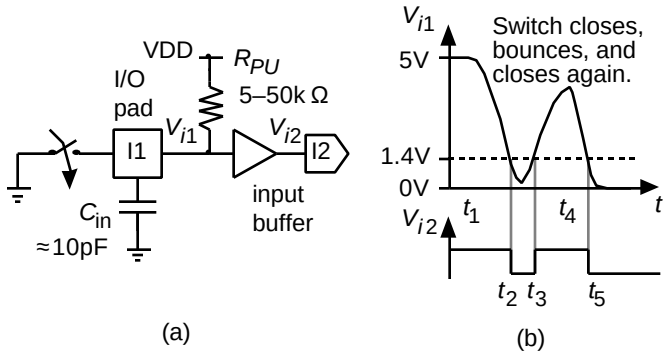
(f) Parallel termination with a series capacitor

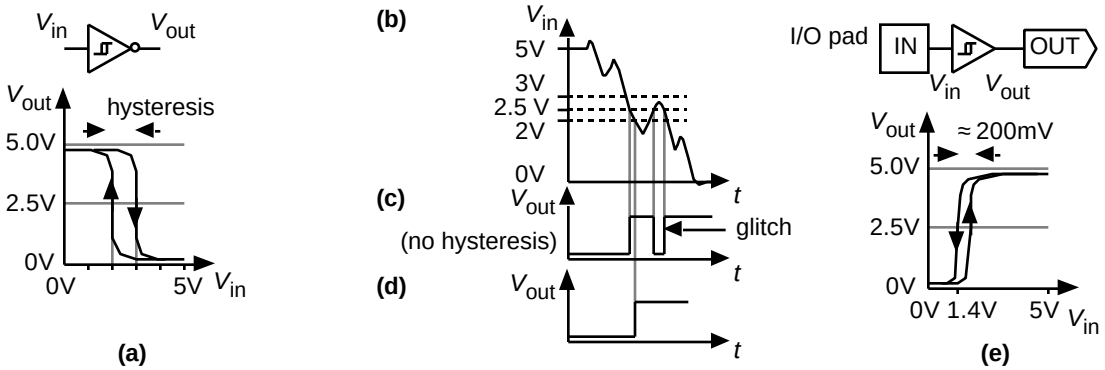
A switch input

(a) A pushbutton switch connected to an input buffer with a pull-up resistor

(b) As the switch bounces several pulses may be generated

We might have to **debounce** this signal using an SR flip-flop or small state machine





DC input

(a) A **Schmitt-trigger inverter** • lower switching threshold • upper switching threshold • difference between thresholds is the **hysteresis**

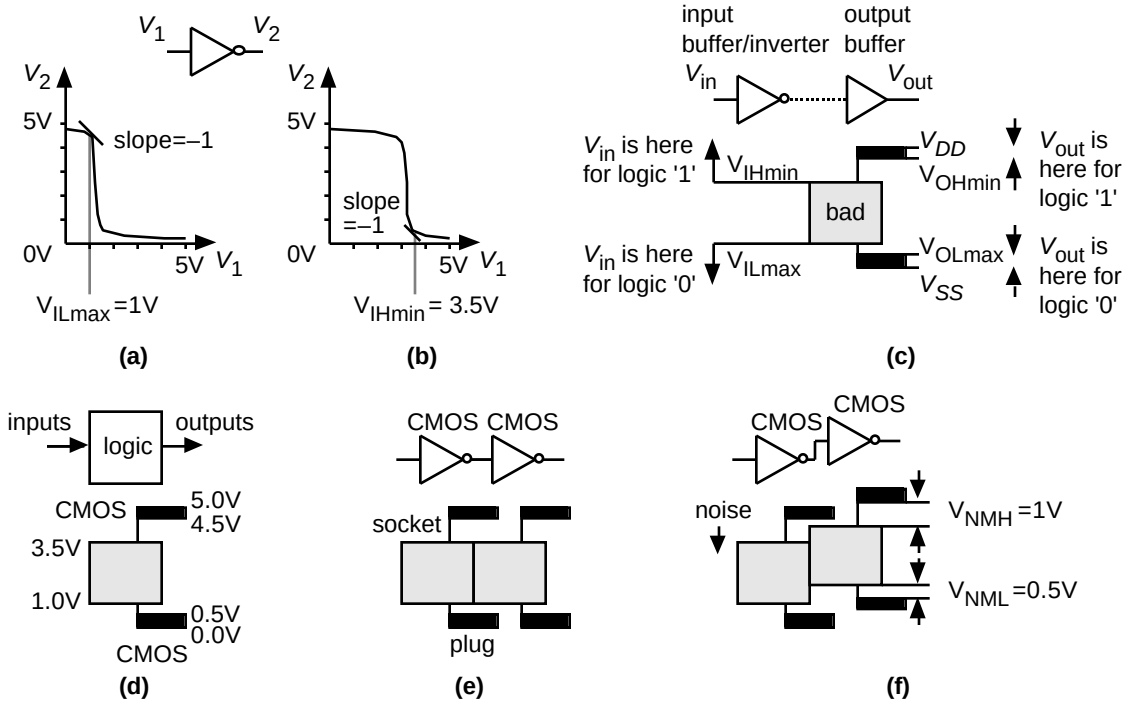
(b) A noisy input signal

(c) Output from an inverter with no hysteresis

(d) Hysteresis helps prevent **glitches**

(e) A typical FPGA input buffer with a hysteresis of 200mV and a threshold of 1.4V

6.3.1 Noise Margins



Noise margins

(a) Transfer characteristics of a CMOS inverter with the lowest switching threshold

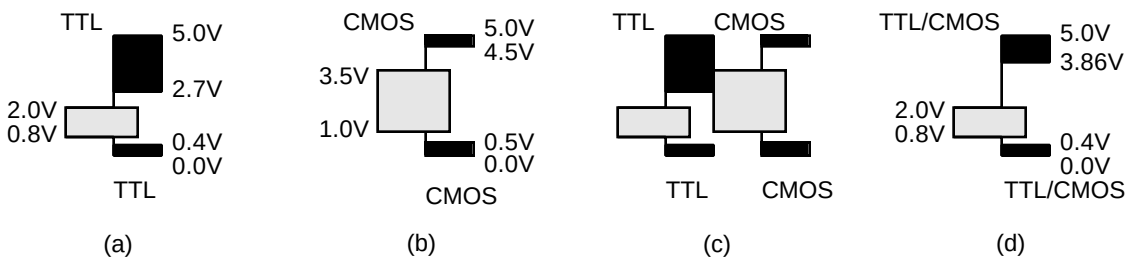
(b) The highest switching threshold

(c) A graphical representation of CMOS **logic thresholds**

(d) Logic thresholds at the inputs and outputs of a logic gate or an ASIC

(e) The switching thresholds viewed as a plug and socket

(f) CMOS plugs fit CMOS sockets and the clearances are the **noise margins**



TTL and CMOS logic thresholds

(a) TTL logic thresholds

(b) Typical CMOS logic thresholds

(c) A TTL plug will not fit in a CMOS socket

(d) Raising V_{OHmin} solves the problem

6.3.2 Mixed-Voltage Systems

FPGA logic thresholds

	I/O options		Input levels		Output levels (high current)				Output levels (low current)			
XC3000	TTL		2.0	0.8	3.86	–4.0	0.40	4.0				
	CMOS		3.85	0.9	3.86	–4.0	0.40	4.0				
XC3000L			2.0	0.8	2.40	–4.0	0.40	4.0	2.80	–0.1	0.2	0.1
XC4000			2.0	0.8	2.40	–4.0	0.40	12.0				
XC4000H	TTL	TTL	2.0	0.8	2.40	–4.0	0.50	24.0				
	CMOS	CMOS	3.85	0.9	4.00	–1.0	0.50	24.0				
XC8100	TTL	R	2.0	0.8	3.86	–4.0	0.50	24.0				
	CMOS	C	3.85	0.9	3.86	–4.0	0.40	4.0				
ACT 2/3			2.0	0.8	2.4	–8.0	0.50	12.0	3.84	–4.0	0.33	6.0
FLEX10k		3V/5V	2.0	0.8	2.4	–4.0	0.45	12.0				

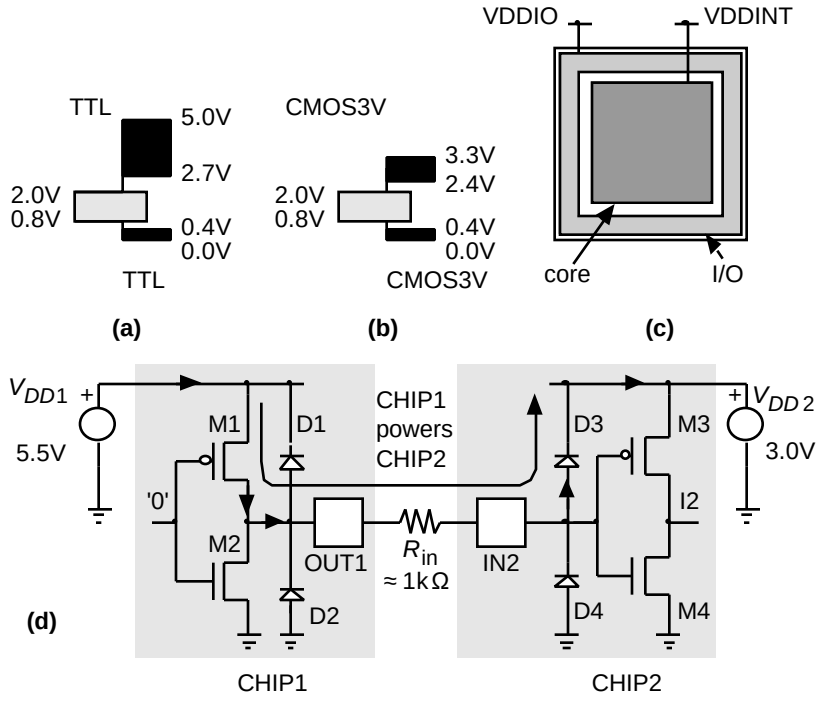
Mixed-voltage systems

(a) TTL levels

(b) Low-voltage CMOS levels • JEDEC 8 • 3.3±0.3V

(c) Mixed-voltage ASIC • 5V-tolerant I/O • V_{DDint} and $V_{DDI/O}$

(d) A problem when connecting two chips with different supply voltages—caused by the input clamp diodes



6.4 AC Input

Keywords and concepts: input bus • sampled data • clock frequency of 100kHz • FPGA • system clock • 10MHz • Data should be at the flip-flop input at least the flip-flop setup time before the clock edge. Unfortunately there is no way to guarantee this; the data clock and the system clock are completely independent

6.4.1 Metastability

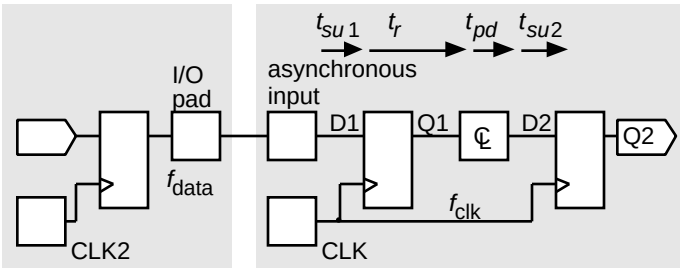
Metastability

(a) Data coming from one clocked system is an **asynchronous** input to another

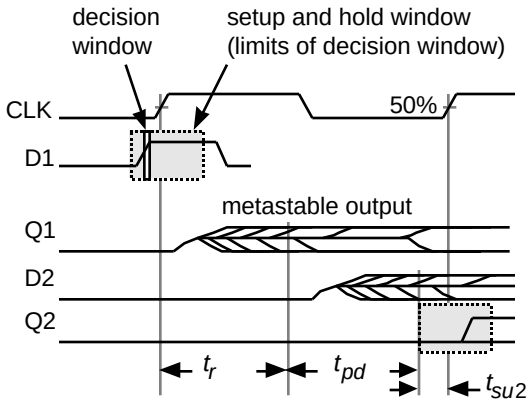
(b) A flip-flop (or latch, a **sampler**) has a very narrow decision window bounded by the setup and hold times to **resolve** the input

If the data input changes inside the decision window (a setup or hold-time **violation**) the output may be **metastable**—neither '1' or '0'—an **upset**

(a)



(b)



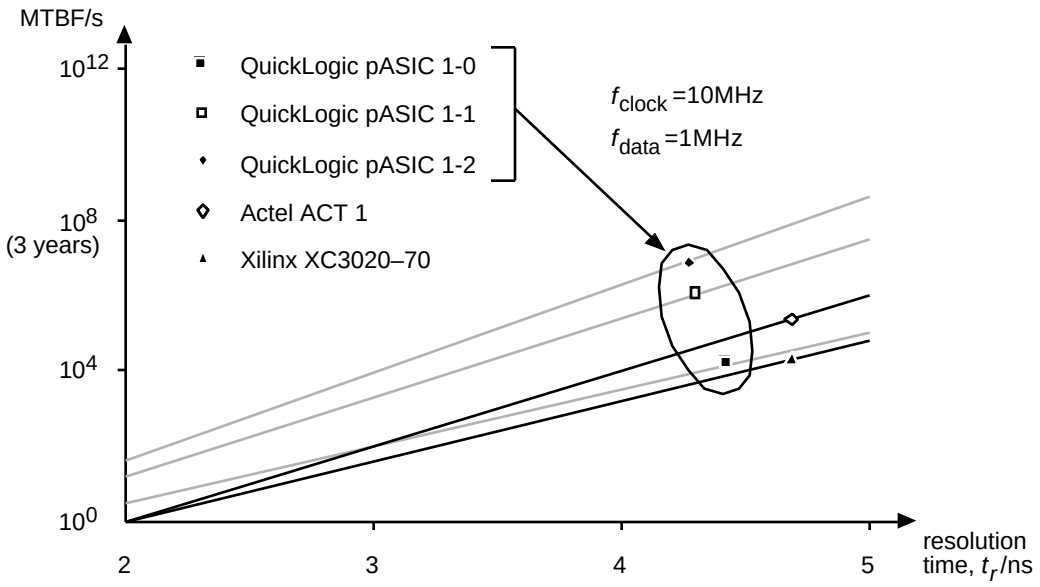
Metastability parameters for FPGA flip-flops (not guaranteed by the vendors)		
FPGA	**T_0/s**	**τ_c/s**
Actel ACT 1	1.0E–09	2.17E–10
Xilinx XC3020-70	1.5E–10	2.71E–10
QuickLogic QL12x16-0	2.94E–11	2.91E–10
QuickLogic QL12x16-1	8.38E–11	2.09E–10
QuickLogic QL12x16-2	1.23E–10	1.85E–10
Altera MAX 7000	2.98E–17	2.00E–10
Altera FLEX 8000	1.01E–13	7.89E–11

The **mean time between upsets** (**MTBU**) or MTBF is

$$\text{MTBU} = \frac{1}{p f_{\text{clock}} f_{\text{data}}} = \frac{\exp t_r/\tau_c}{f_{\text{clock}}\, f_{\text{data}}}$$

where f_{clock} is the clock frequency and f_{data} is the data frequency

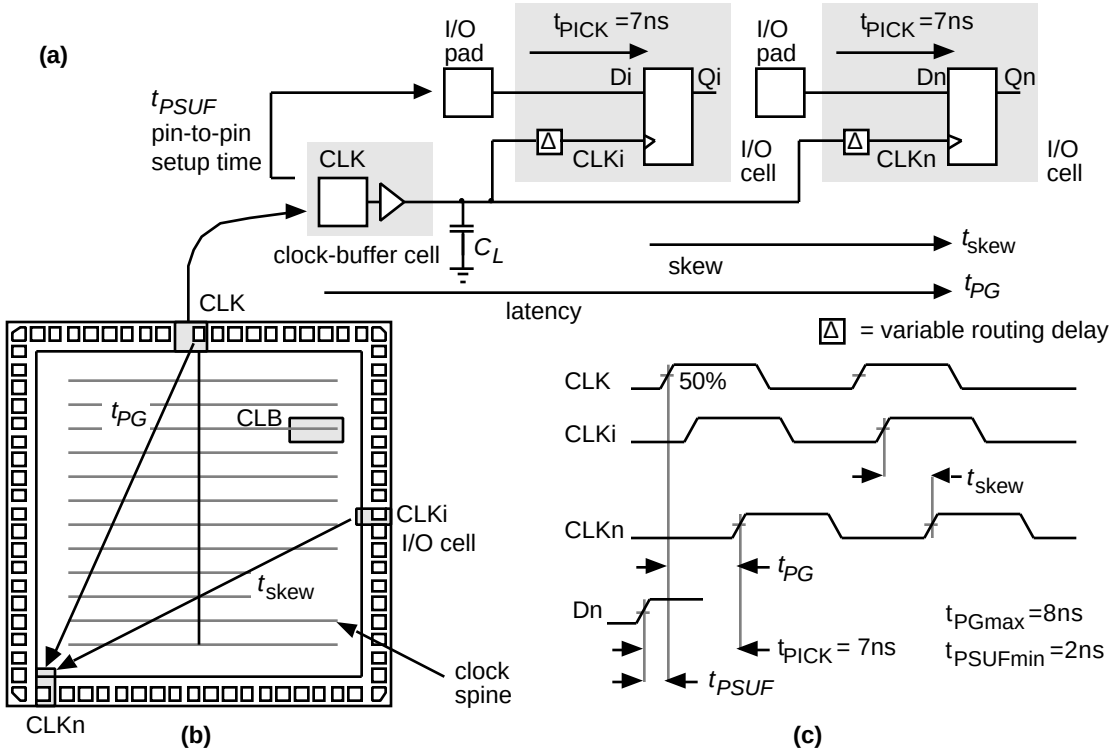
A **synchronizer** is built from two flip-flops in cascade, and greatly reduces the effective values of τ_c and T_0 over a single flip-flop. The penalty is an extra clock cycle of latency.



Mean time between failure (MTBF) as a function of resolution time

The data is from FPGA vendors' data books for a single flip-flop with clock frequency of 10MHz and a data input frequency of 1MHz

6.5 Clock Input



Clock input

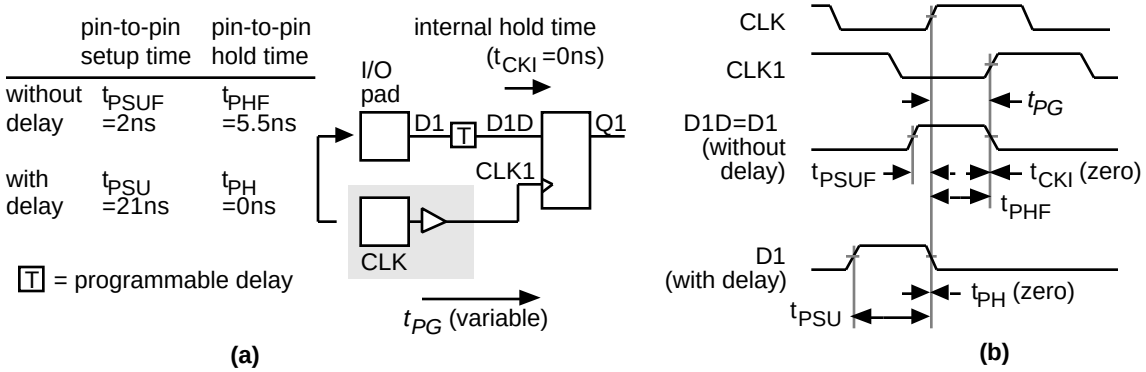
(a) Timing model (Xilinx XC4005-6)

(b) A simplified view of clock distribution • **clock skew** • **clock latency**

(c) Timing diagram

(Xilinx eliminates the variable internal delay t_{PG}, by specifying a **pin-to-pin setup time**, $t_{PSUFmin}$=2ns)

6.5.1 Registered Input



Programmable input delay

(a) Pin-to-pin timing model (XC4005-6) with pin-to-pin timing parameters

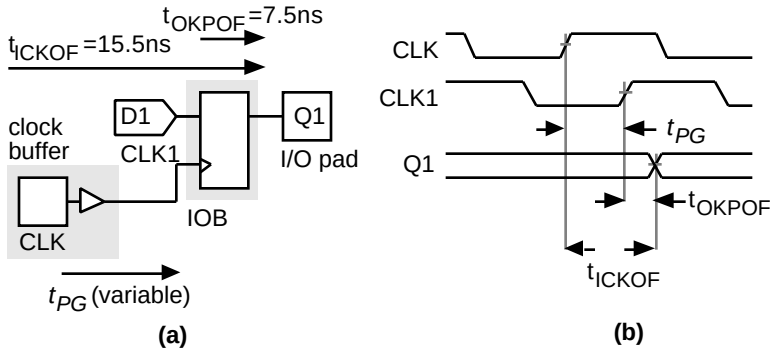
(b) Timing diagrams with and without programmable delay

Notice $t_{PSUFmin}$ = 2 ns ≠ t_{PICK} – t_{PGmax} = –1 ns

Registered output

(a) Timing model with values for an XC4005-6 programmed with the fast slew-rate option

(b) Timing diagram



6.6 Power Input

6.6.1 Power Dissipation

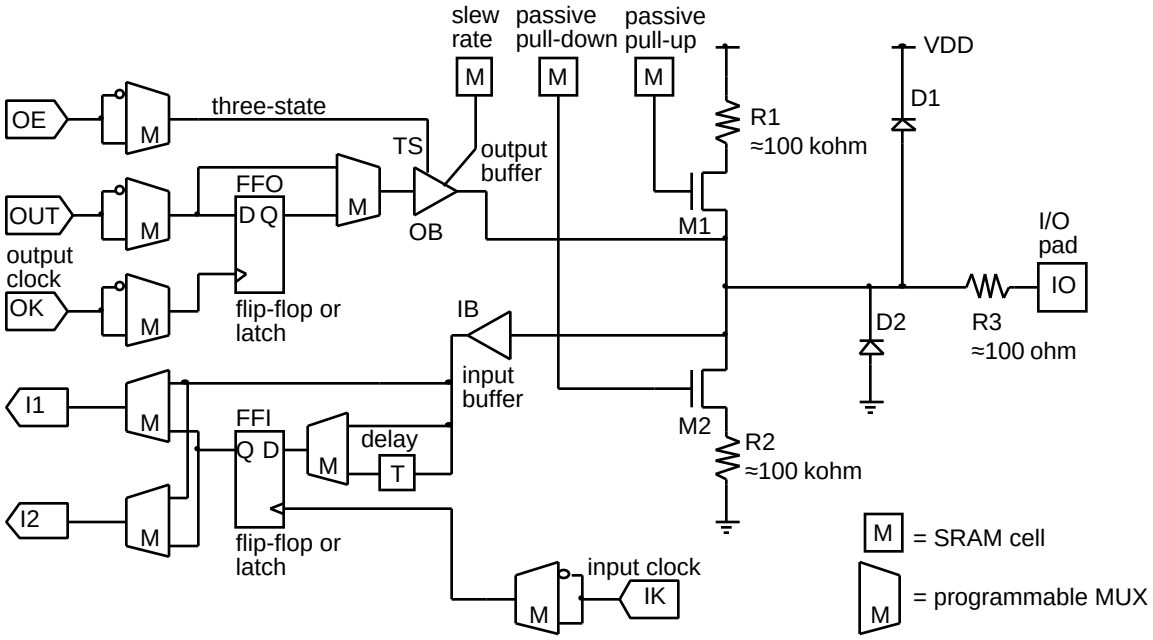
Thermal characteristics of ASIC packages

Package	Pin count	Max. power P_{max}/W	θ_{JA} /°CW^{-1} (still air)	θ_{JA} /°CW^{-1} (still air)
CPGA	84		33	32–38
CQFP	84		40	
CQFP	172		25	
VQFP	80		68	

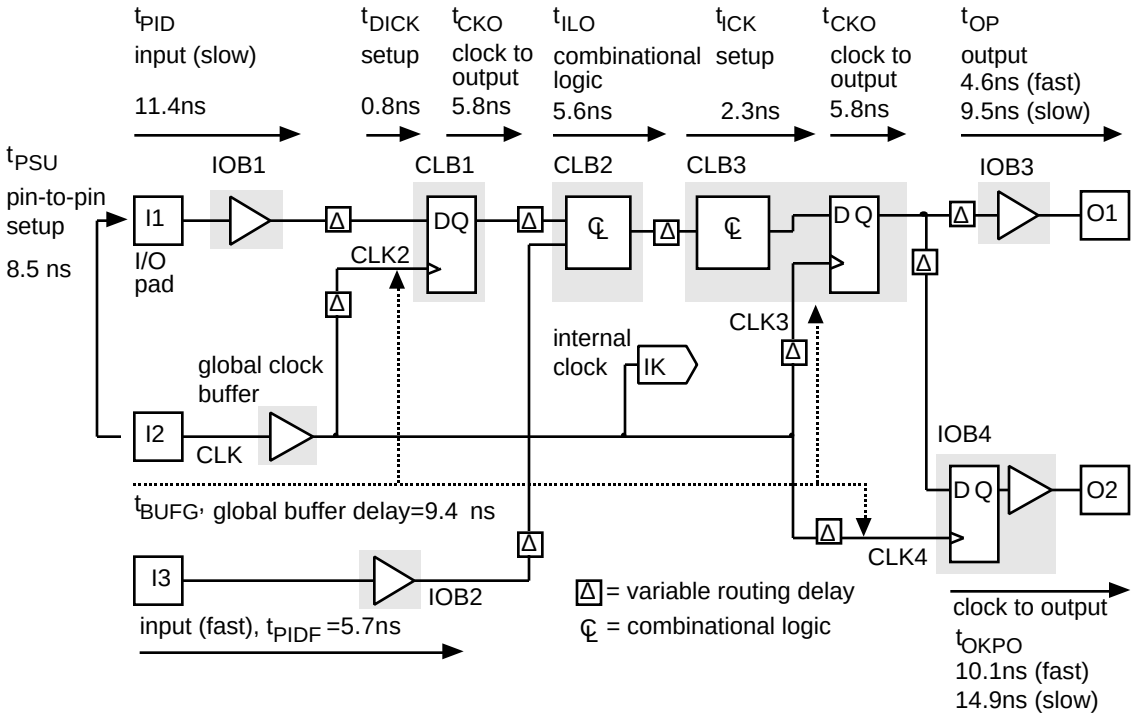
6.6.2 Power-On Reset

Key concepts: Power-on reset sequence • Xilinx FPGAs configure all flip-flops (in either the CLBs or IOBs) as either SET or RESET • after chip programming is complete, the global SET/RESET signal forces all flip-flops on the chip to a known state • this may determine the initial state of a state machine, for example

6.7 Xilinx I/O Block



The Xilinx XC4000 family IOB (input/output block). (*Source:* Xilinx.)



The Xilinx LCA (Logic Cell Array) timing model (XC5210-6). (*Source:* Xilinx.)

6.7.1 Boundary Scan

Key concepts: IEEE boundary-scan standard 1149.1 • Many FPGAs contain a standard boundary-scan test logic structure with a four-pin interface • **in-system programming** (ISP)

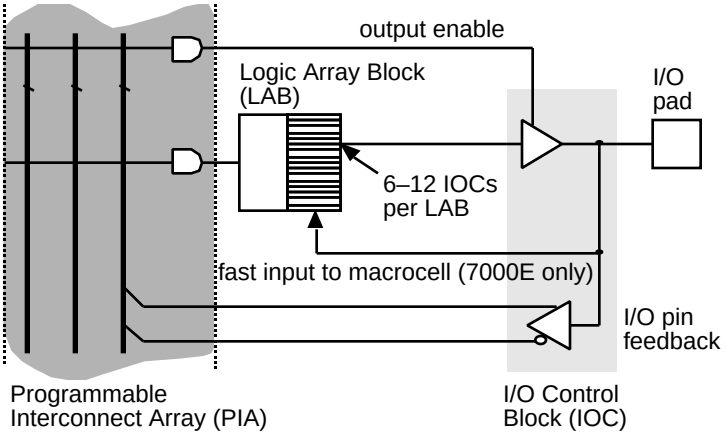
6.8 Other I/O Cells

A simplified block diagram of the Altera **I/O Control Block** (IOC) used in the MAX 5000 and MAX 7000 series

The **I/O pin feedback** allows the I/O pad to be isolated from the macrocell

It is thus possible to use a LAB without using up an I/O pad (as you often have to do using a PLD such as a 22V10)

The **PIA** is the chipwide interconnect

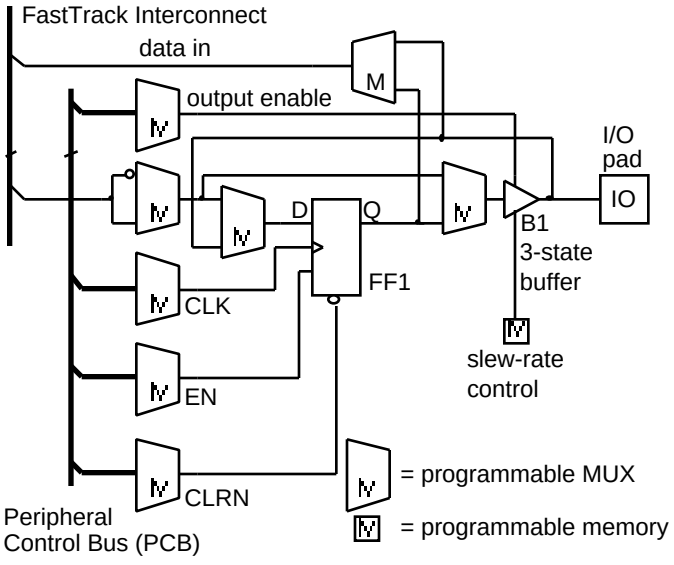


A simplified block diagram of the Altera **I/O Element** (IOE), used in the FLEX 8000 and 10k series

The MAX 9000 IOC (I/O Cell) is similar

The FastTrack Interconnect bus is the chipwide interconnect

The **Peripheral Control Bus** (PCB) is used for control signals common to each IOE



6.9 Summary

Key concepts:

Outputs can typically source or sink 5–10mA continuously into a DC load

Outputs can typically source or sink 50–200mA transiently into an AC load

Input buffers can be CMOS (threshold at $0.5V_{DD}$) or TTL (1.4V)

Input buffers normally have a small hysteresis (100–200mV)

CMOS inputs must never be left floating

Clamp diodes to GND and VDD are present on every pin

Inputs and outputs can be registered or direct

I/O registers can be in the I/O cell or in the core

Metastability is a problem when working with asynchronous inputs