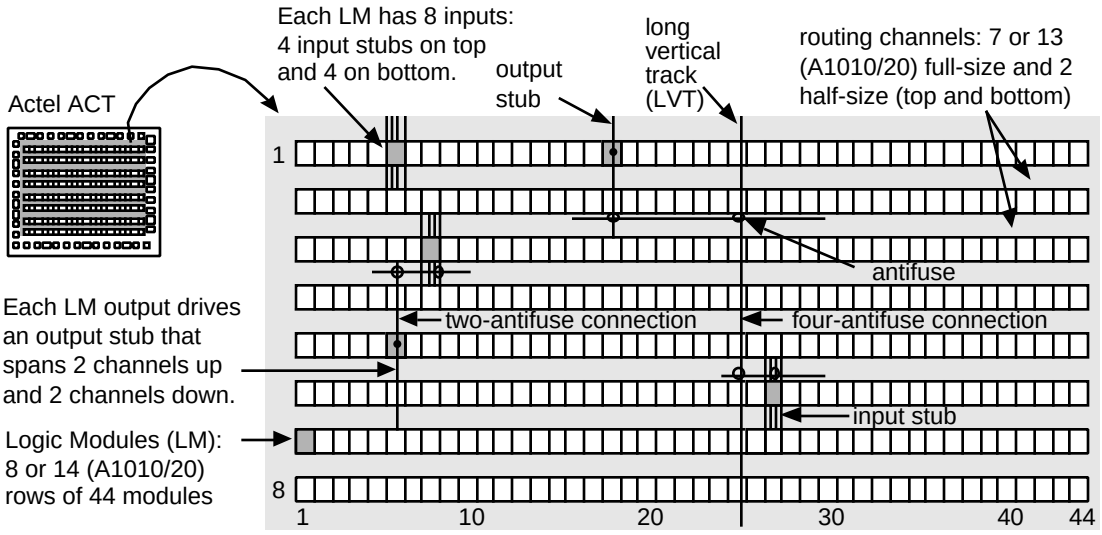
PROGRAMMABLE ASIC INTERCONNECT

7

Key concepts: programmable interconnect • raw materials: aluminum-based metallization and a line capacitance of 0.2pFcm^{-1}

7.1 Actel ACT



The interconnect architecture used in an Actel ACT family FPGA. (*Source:* Actel.)

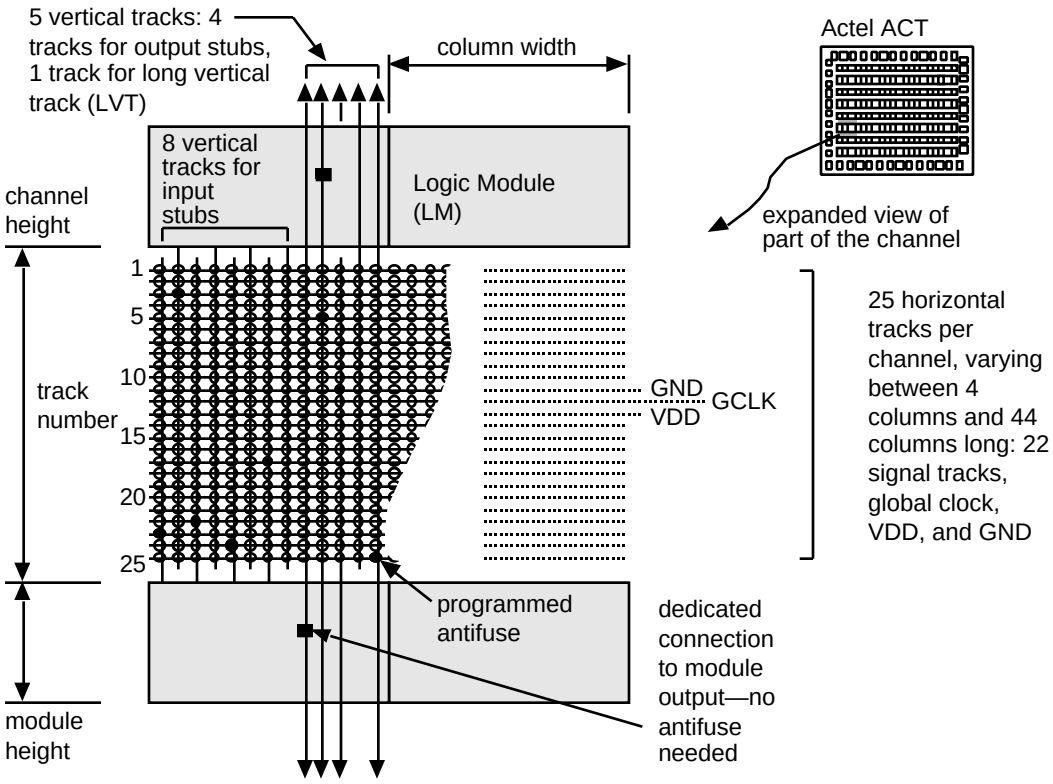
Features and keywords:

• Wiring channels (or just channels) • Horizontal channels • Vertical channels

• Tracks • Channel capacity • Long vertical tracks (LVTs)

• Input stubs and output stubs

• Wire segments • Segmented channel routing • Long lines



ACT 1 horizontal and vertical channel architecture. (*Source:* Actel.)

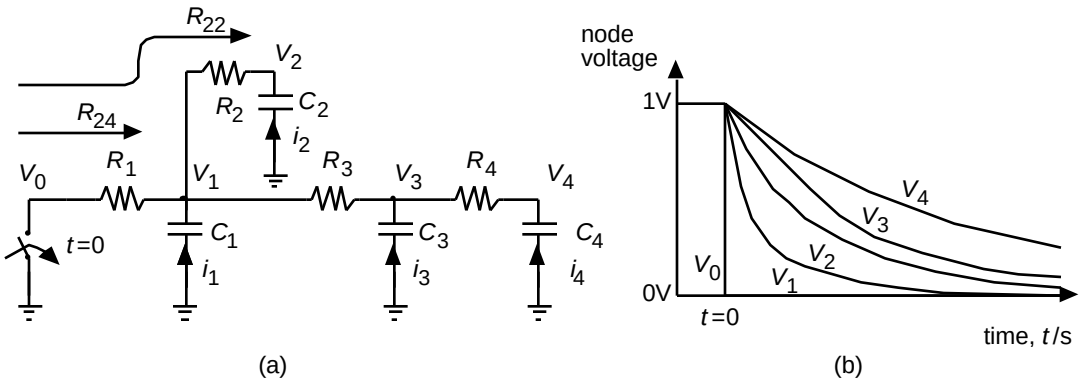
Features:

- Input stubs
- Output stubs
- Long vertical tracks (LVT)
- Fully populated interconect array

7.1.1 Routing Resources

Actel FPGA routing resources						
	Horizontal tracks per channel, H	**Vertical tracks per column, V**	**Rows, R**	**Columns, C**	**Total antifuses on each chip**	**H×V×R × C**
A1010	22	13	8	44	112,000	100,672
A1020	22	13	14	44	186,000	176,176
A1225A	36	15	13	46	250,000	322,920
A1240A	36	15	14	62	400,000	468,720
A1280A	36	15	18	82	750,000	797,040

7.1.2 Elmore's Constant



Measuring the delay of a net

(a) An RC tree

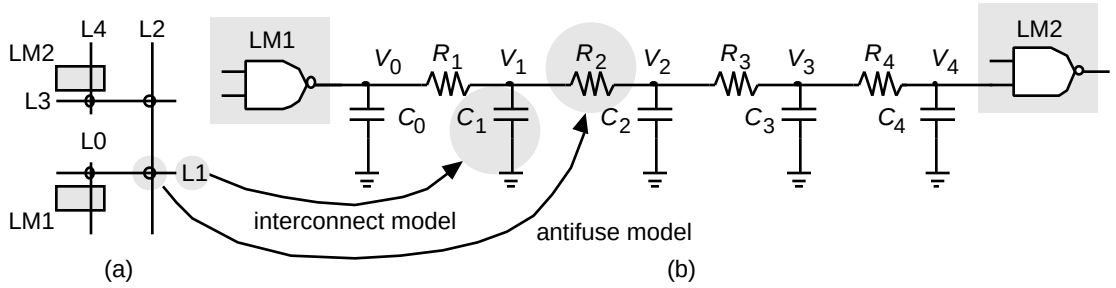
(b) The waveforms as a result of closing the switch at $t = 0$

$$V_i(t) = \exp(-t/\tau_{Di}) \quad ; \qquad \tau_{Di} = \sum_{k=1}^{n} R_{ki}C_k$$

The time constant τ_{Di} is often called the **Elmore delay** and is different for each node.

I call τ_{Di} the **Elmore time constant** as a reminder that, if we approximate V_i by an exponential waveform, the delay of the RC tree using 0.35/0.65 trip points is approximately τ_{Di} seconds.

7.1.3 RC Delay in Antifuse Connections



Actel routing model

(a) A four-antifuse connection. L0 is an output stub, L1 and L3 are horizontal tracks, L2 is a long vertical track (LVT), and L4 is an input stub

(b) An RC-tree model. Each antifuse is modeled by a resistance and each interconnect segment is modeled by a capacitance.

$$\tau_{D4} = R_{14}C_1 + R_{24}C_2 + R_{14}C_1 + R_{44}C_4$$
$$= (R_1 + R_2 + R_3 + R_4)C_4 + (R_1 + R_2 + R_3)C_3 + (R_1 + R_2)C_2 + R_1C_1$$

$$\tau_{D4} = 4RC_4 + 3RC_3 + 2RC_2 + RC_1$$

- Two antifuses will generate a 3*RC* time constant
- Three antifuses a 6*RC* time constant
- Four antifuses gives a 10*RC* time constant
- Interconnect delay grows quadratically (n^2) as we increase the interconnect length and the number of antifuses, *n*

7.1.4 Antifuse Parasitic Capacitance

7.1.5 ACT 2 and ACT 3 Interconnect

channel density • fast fuse

Actel interconnect parameters

Parameter	A1010/A1020	A1010B/A1020B
Technology	2.0µm, λ=1.0µm	1.2µm, λ=0.6µm
Die height (A1010)	240mil	144mil
Die width (A1010)	360mil	216mil
Die area (A1010)	86,400mil^2=56Mλ^2	31,104mil^2=56Mλ^2
Logic Module (LM) height (Y1)	180µm=180λ	108µm=180λ
LM width (X)	150µm=150λ	90µm=150λ
LM area (X×Y1)	27,000µm^2=27kλ^2	9,720µm^2=27kλ^2
Channel height (Y2)	25 tracks=287µm	25 tracks=170µm
Channel area per LM (X×Y2)	43,050µm^2=43kλ^2	15,300µm^2=43kλ^2
LM and routing area (X×Y1+X×Y2)	70,000µm^2=70kλ^2	25,000µm^2=70kλ^2
Antifuse capacitance	—	10 fF
Metal capacitance	0.2pFmm^{-1}	0.2pFmm^{-1}
Output stub length (spans 3 LMs + 4 channels)	4 channels=1688µm	4 channels=1012µm
Output stub metal capacitance	0.34pF	0.20pF
Output stub antifuse connections	100	100
Output stub antifuse capacitance	—	1.0pF
Horiz. track length	4–44 cols.= 600–6600µm	4–44 cols.= 360–3960µm
Horiz. track metal capacitance	0.1–1.3pF	0.07–0.8pF
Horiz. track antifuse connections	52–572 antifuses	52–572 antifuses
Horiz. track antifuse capacitance	—	0.52–5.72 pF
Long vertical track (LVT)	8–14 channels=3760–6580 µm	8–14 channels=2240–3920 µm
LVT metal capacitance	0.08–0.13pF	0.45–0.8pF
LVT track antifuse connections	200–350 antifuses	200–350 antifuses
LVT track antifuse capacitance		2–3.5pF
Antifuse resistance (ACT 1)		0.5kΩ (typ.), 0.7kΩ (max.)

Actel interconnect:

An input stub (1 channel) connects to 25 antifuses

An output stub (4 channels) connects to 100 (25×4) antifuses

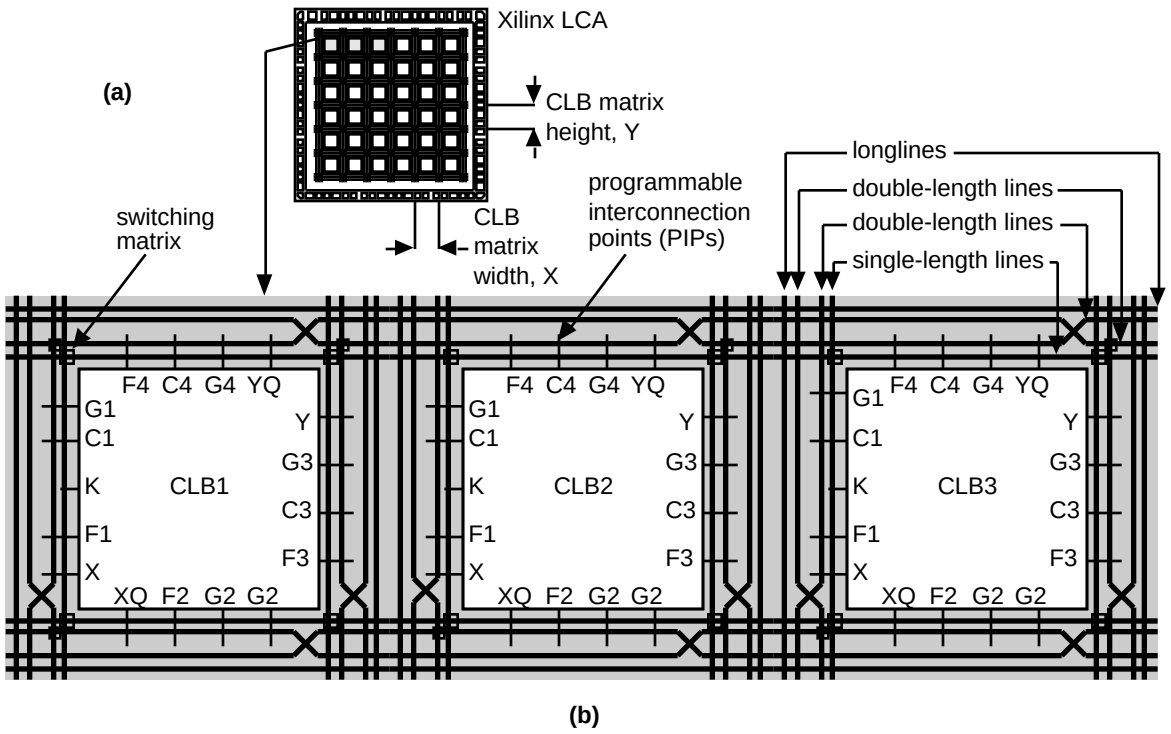
An LVT (1010, 8 channels) connects to 200 (25×8) antifuses

An LVT (1020, 14 channels) connects to 350 (25×14) antifuses

A four-column horizontal track connects to 52 (13×4) antifuses

A 44-column horizontal track connects to 572 (13×44) antifuses

7.2 Xilinx LCA



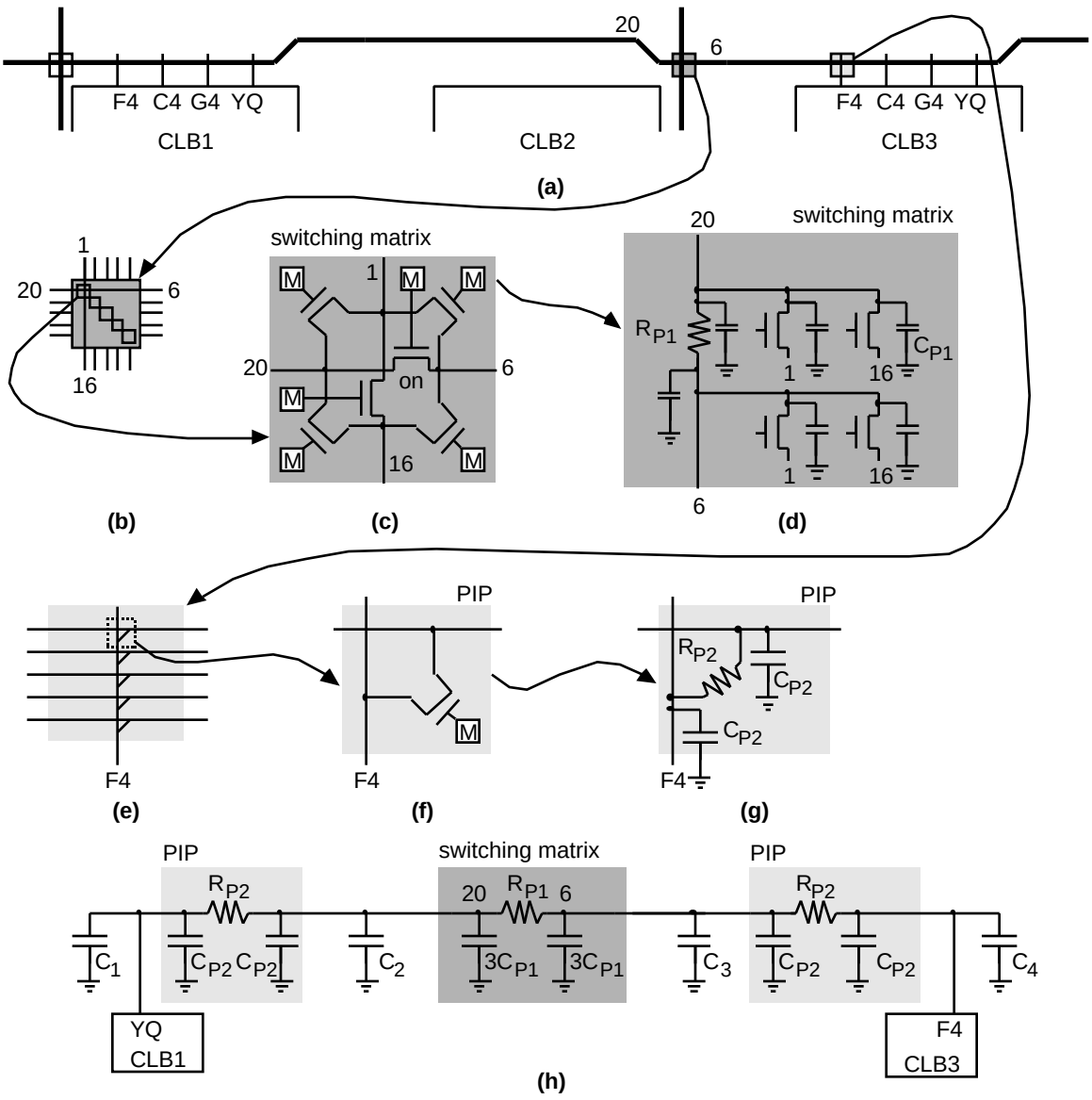
Xilinx LCA interconnect

(a) The LCA architecture (notice the **matrix element** size is larger than a CLB)

(b) A simplified representation of the interconnect resources. Each of the lines is a bus.

- The **vertical lines** and **horizontal lines** run between CLBs.
- The **general-purpose interconnect** joins **switch boxes** (also known as **magic boxes** or **switching matrices**).
- The **long lines** run across the entire chip. It is possible to form internal buses using long lines and the three-state buffers that are next to each CLB.
- The **direct connections** (not used on the XC4000) bypass the switch matrices and directly connect adjacent CLBs.
- The **Programmable Interconnection Points** (PIPs) are programmable pass transistors that connect the CLB inputs and outputs to the routing network.
- The **bidirectional (BIDI) interconnect buffers** restore the logic level and logic strength on long interconnect paths

XC3000 interconnect parameters	
Parameter	**XC3020**
Technology	1.0µm, λ=0.5µm
Die height	220mil
Die width	180mil
Die area	39,600mil^2=102Mλ^2
CLB matrix height (Y)	480µm=960λ
CLB matrix width (X)	370µm=740λ
CLB matrix area (X× Y)	17,600µm^2=710kλ^2
Matrix transistor resistance, R_{P1}	0.5–1kΩ
Matrix transistor parasitic capacitance, C_{P1}	0.01–0.02pF
PIP transistor resistance, R_{P2}	0.5–1kΩ
PIP transistor parasitic capacitance, C_{P2}	0.01–0.02pF
Single-length line (X, Y)	370µm, 480µm
Single-length line capacitance: C_{LX}, C_{LY}	0.075pF, 0.1pF
Horizontal Longline (8X)	8 cols.=2960µm
Horizontal Longline metal capacitance, C_{LL}	0.6pF



Components of interconnect delay in a Xilinx LCA array

(a) A portion of the interconnect around the CLBs

(b) A switching matrix

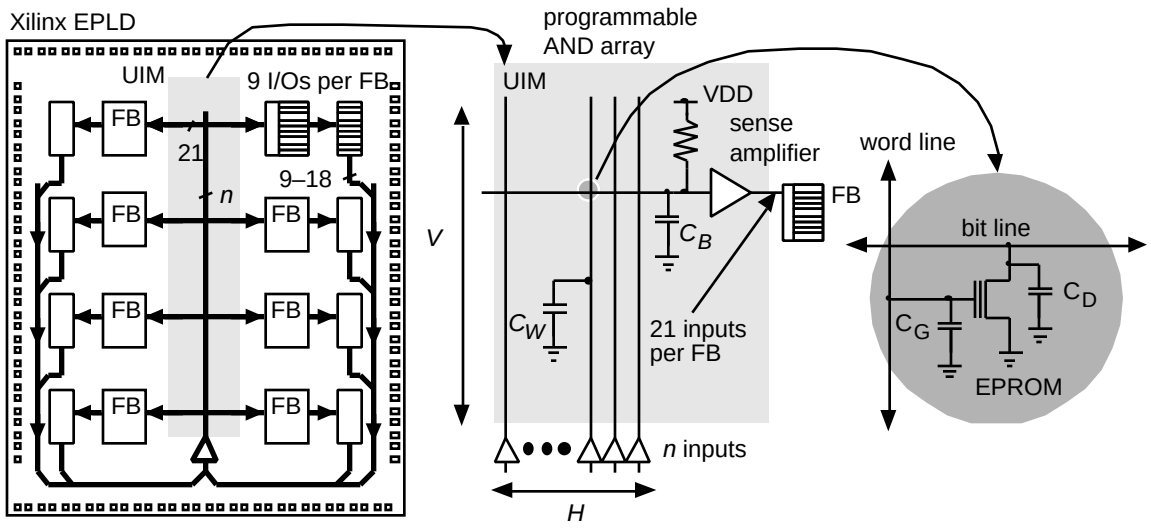
(c) A detailed view inside the switching matrix showing the pass-transistor arrangement

(d) The equivalent circuit for the connection between nets 6 and 20 using the matrix

(e) A view of the interconnect at a Programmable Interconnection Point (PIP)

(f) and **(g)** The equivalent schematic of a PIP connection **(h)** The complete RC delay path

7.3 Xilinx EPLD



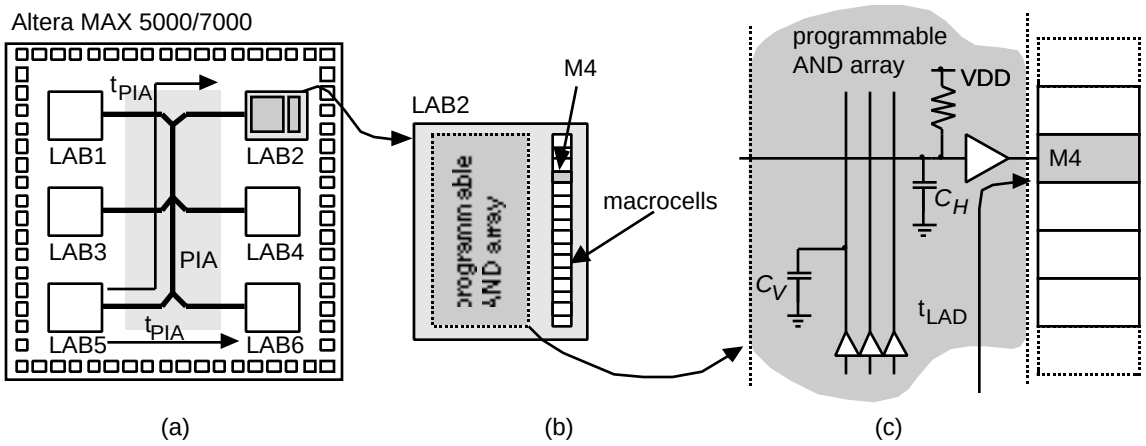
The Xilinx EPLD UIM (Universal Interconnection Module)

(a) A simplified block diagram of the UIM. The UIM bus width, *n*, varies from 68 (XC7236) to 198 (XC73108)

(b) The UIM is actually a large programmable AND array

(c) The parasitic capacitance of the EPROM cell

7.4 Altera MAX 5000 and 7000



A simplified block diagram of the Altera MAX interconnect scheme

(a) The PIA (Programmable Interconnect Array) is deterministic—delay is independent of the path length

(b) Each LAB (Logic Array Block) contains a programmable AND array

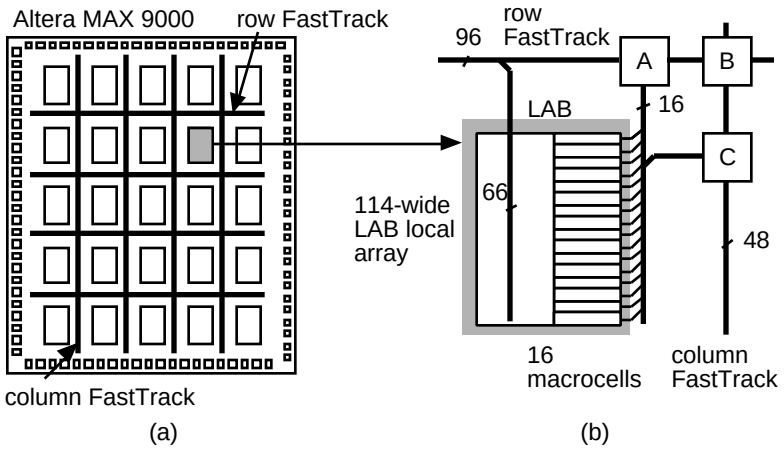
(c) Interconnect timing within a LAB is also fixed

7.5 Altera MAX 9000

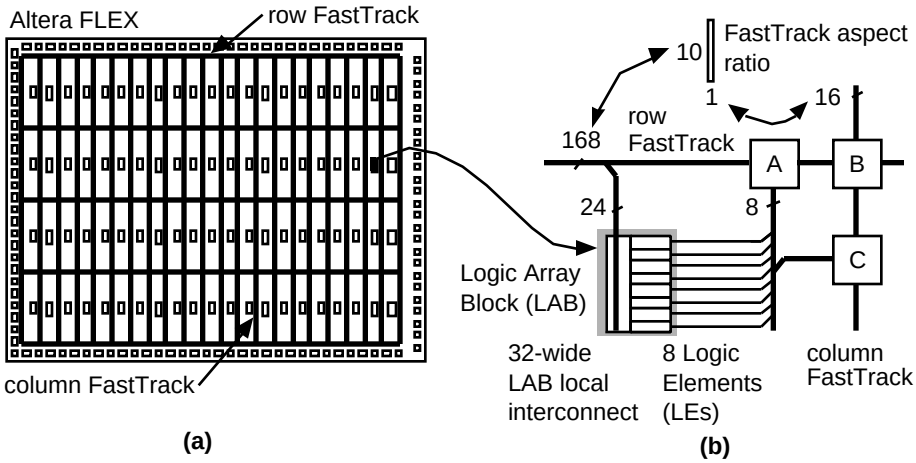
The Altera MAX 9000 interconnect scheme

(a) A 4×5 array of Logic Array Blocks (LABs), the same size as the EMP9400 chip

(b) A simplified block diagram of the interconnect architecture showing the connection of the FastTrack buses to a LAB



7.6 Altera FLEX



The Altera FLEX interconnect scheme

(a) The row and column FastTrack interconnect. The chip shown, with 4 rows × 21 columns, is the same size as the EPF8820

(b) A simplified diagram of the interconnect architecture showing the connections between the FastTrack buses and a LAB. Boxes A, B, and C represent the bus-to-bus connections

7.7 Summary

The RC product of the parasitic elements of an antifuse and a pass transistor are not too different. However, an SRAM cell is much larger than an antifuse which leads to coarser interconnect architectures for SRAM-based programmable ASICs. The EPROM device lends itself to large wired-logic structures.

These differences in programming technology lead to different architectures:

• The antifuse FPGA architectures are dense and regular.

• The SRAM architectures contain nested structures of interconnect resources.

• The complex PLD architectures use long interconnect lines but achieve deterministic routing.

Key points:

• The difference between deterministic and nondeterministic interconnect

• Estimating interconnect delay

• Elmore’s constant

7.8 Problems