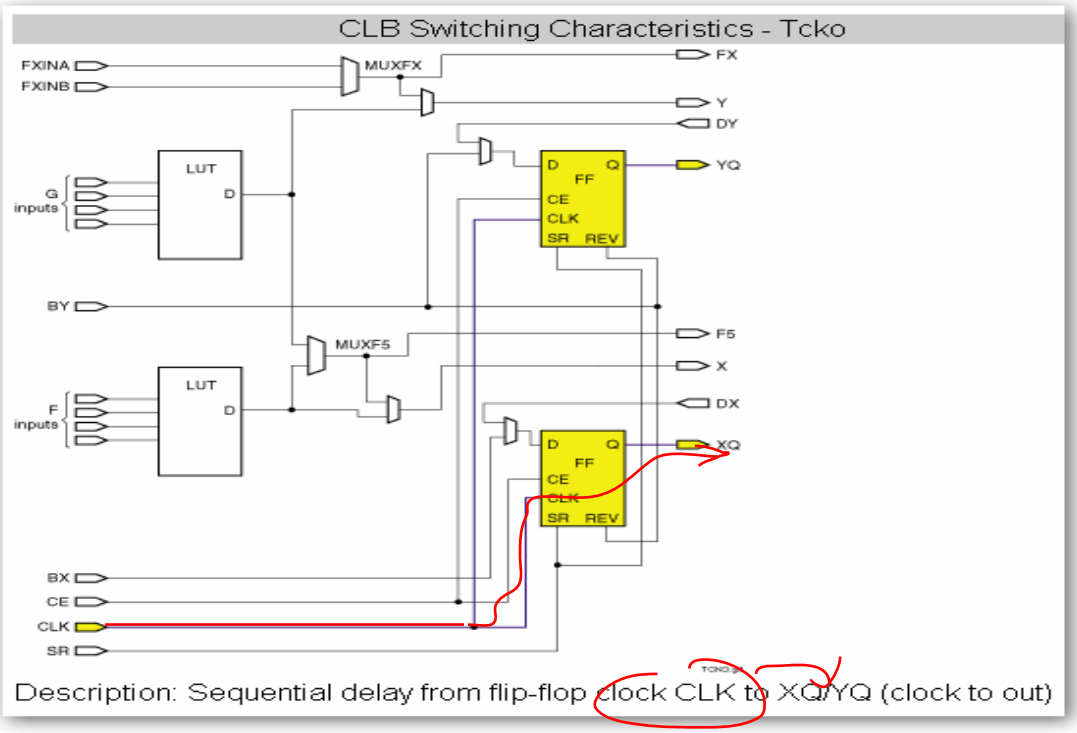
```
--------------------------------------------------------------------------------
Slack:                  -3.711ns (requirement - (data path - clock path skew + uncertainty))
  Source:               RAM_416/dp_ram.waddr_tmp[8] (FF)
  Destination:          RAM_416/dp_ram.adreq_0.DOUTB_ret_13 (FF)
  Requirement:          5.400ns
  Data Path Delay:      9.111ns (Levels of Logic = 3)
  Clock Path Skew:      0.000ns
  Source Clock:         clk_c rising at 0.000ns
  Destination Clock:    clk_c falling at 5.400ns
  Clock Uncertainty:    0.000ns
  Timing Improvement Wizard
  Data Path: RAM_416/dp_ram.waddr_tmp[8] to RAM_416/dp_ram.adreq_0.DOUTB_ret_13
    Delay type         Delay(ns)  Physical Resource
                                  Logical Resource(s)
    -------------------------  --------------------
    Tcko                0.494  RAM_416/waddr_tmp(8)
                               RAM_416/dp_ram.waddr_tmp[8]
    net (fanout=1)      1.510  RAM_416/waddr_tmp(8)
    Topxb               0.860  RAM_416/N_1_ret_0i
                               RAM_416/dp_ram.adreq_0.N_7_i
                               RAM_416/dp_ram.adreq_0.I_37
    net (fanout=36)     2.817  RAM_416/N_1_ret_0i
    Tilo                0.382  RAM_416/DOUTB_ret_1
                               RAM_416/dp_ram.N_1_ret_0i_17
    net (fanout=2)      0.634  RAM_416/N_1_ret_0i_17
    Tilo                0.382  RAM_416/DOUTB_ret_12
                               RAM_416/dp_ram.N_1_ret_0i_17_0
    net (fanout=8)      1.710  RAM_416/N_1_ret_0i_17_0
    Tdick               0.322  RAM_416/DOUTB_ret_13
                               RAM_416/dp_ram.adreq_0.DOUTB_ret_13
    -------------------------  --------------------------
    Total               9.111ns (2.440ns logic, 6.671ns route)
                                (26.8% logic, 73.2% route)
--------------------------------------------------------------------------------
```

单击会出现提示改进方法

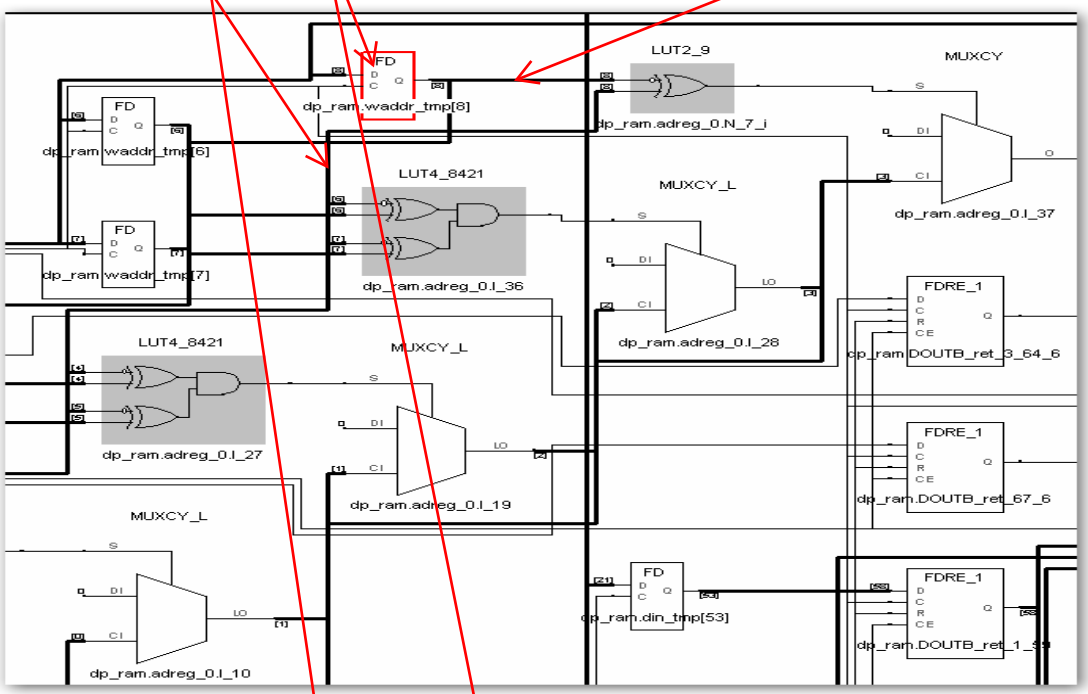
LOGIC为打钩的和

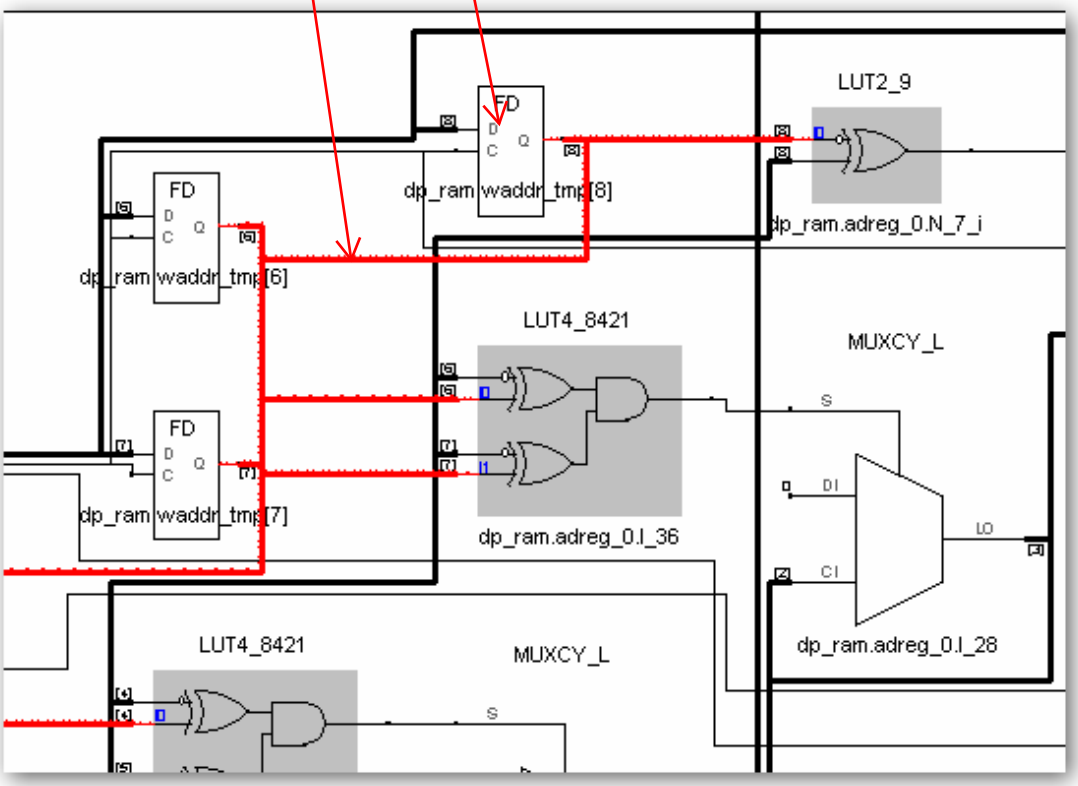
TCKO：在 CLB 内部的情况

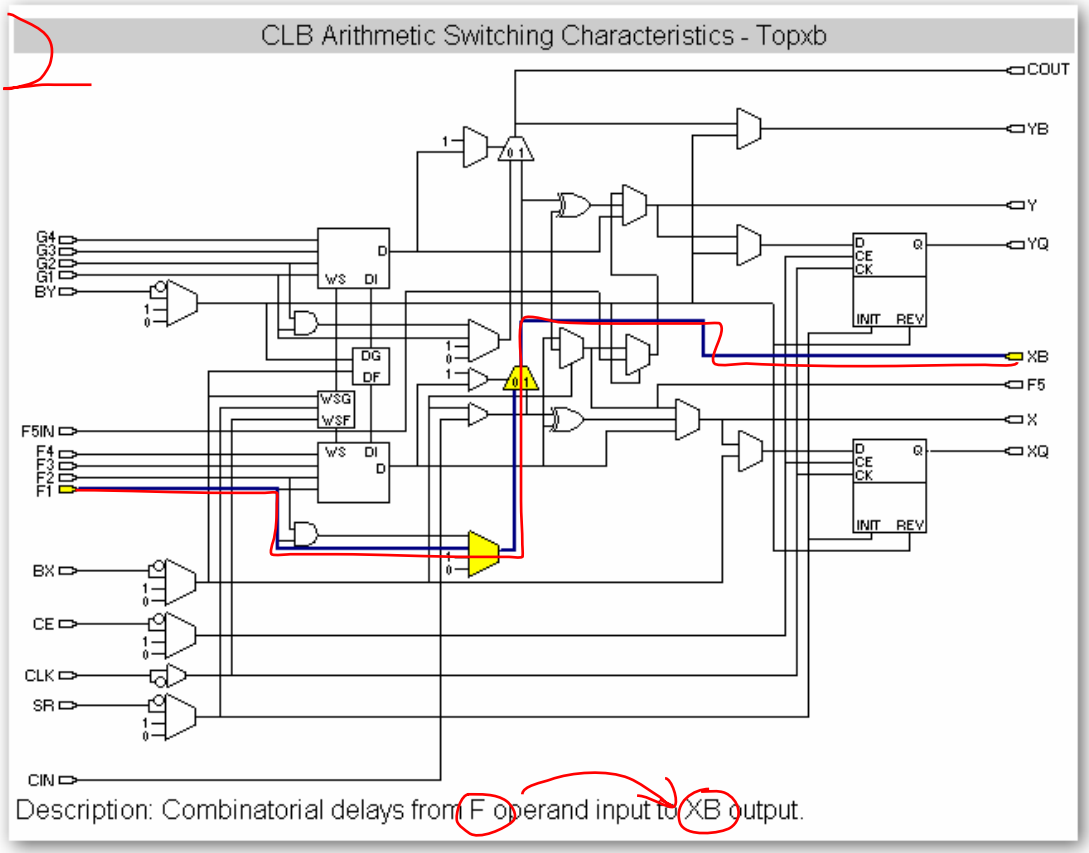


RAM_416/dp_ram.waddr_tmp[8] ：为原件，LOGIC延迟 出发点

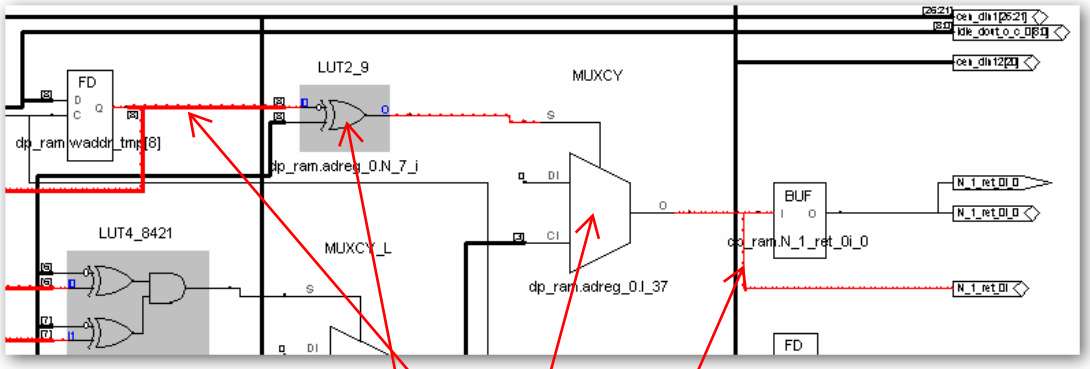
RAM_416/waddr_tmp(8)：走线（NET），ROUTE 延迟







对应上图的实际中的 TOPXB 的延迟

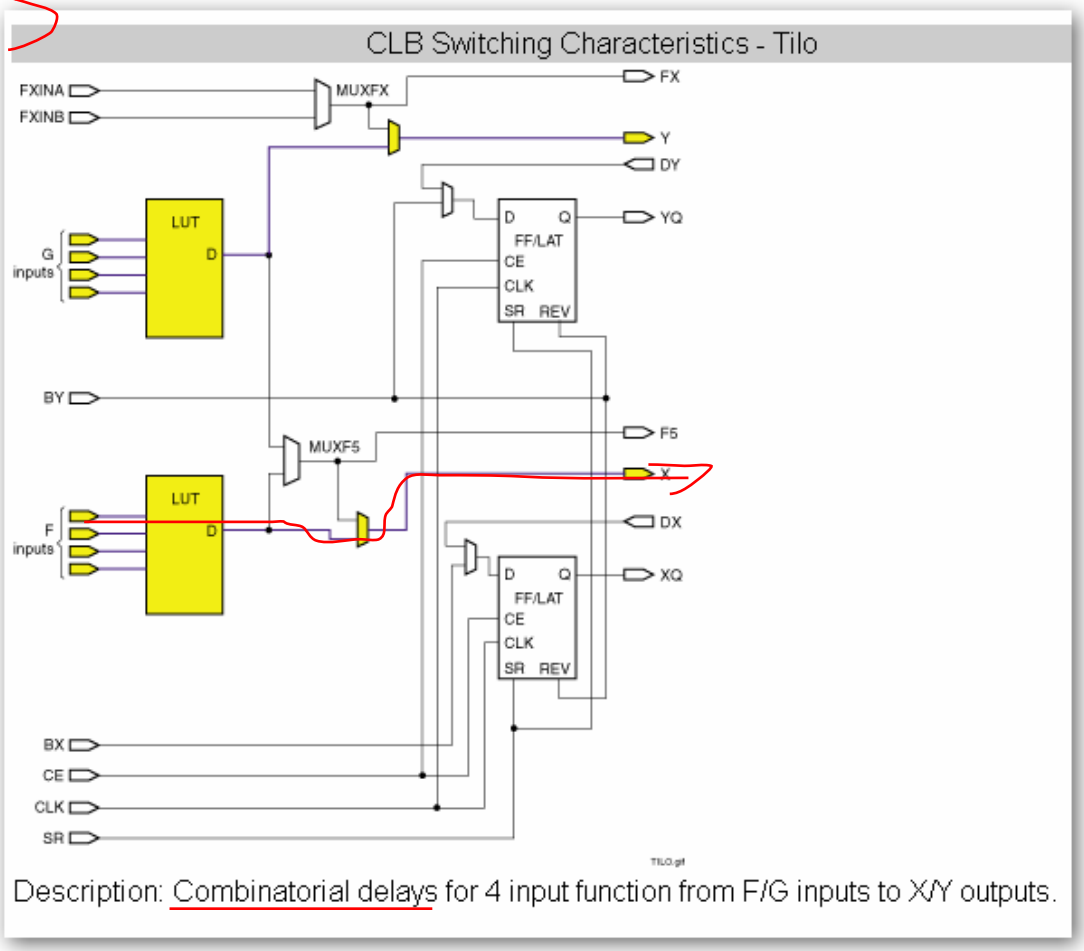


[Topxb](#) 0.860 RAM_416/N_1_ret_0i

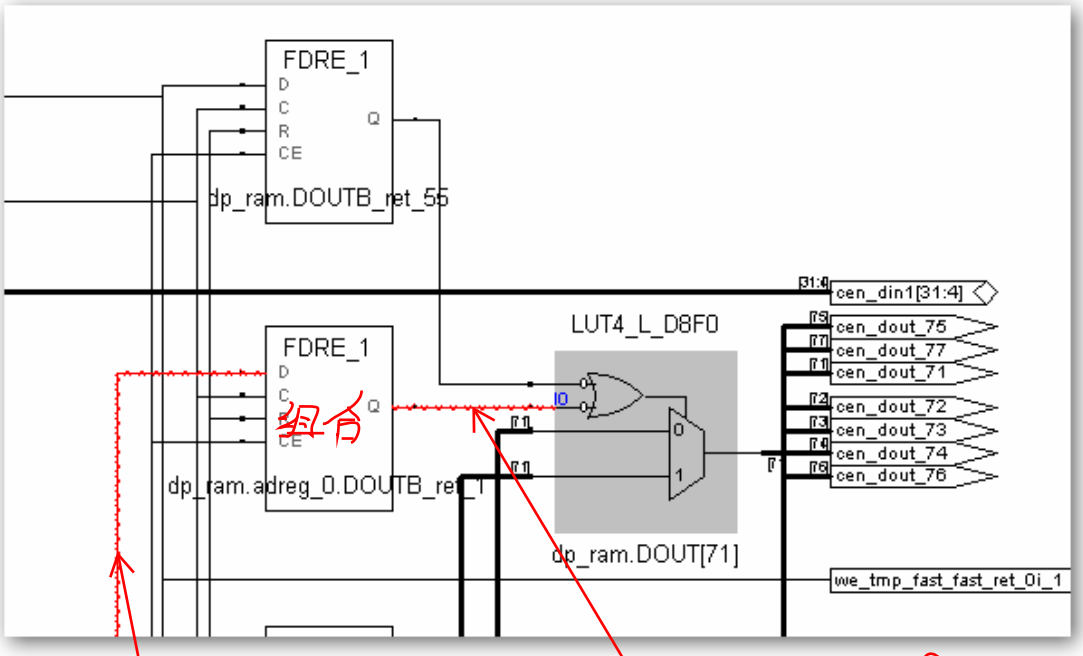
[RAM_416/dp_ram.adreg_0.N_7_i（LOGIC延迟](#)

[RAM_416/dp_ram.adreg_0.I_37（LOGIC延迟](#)

net （fanout=36） 2.817 [RAM_416/N_1_ret_0i（route延迟）](#)

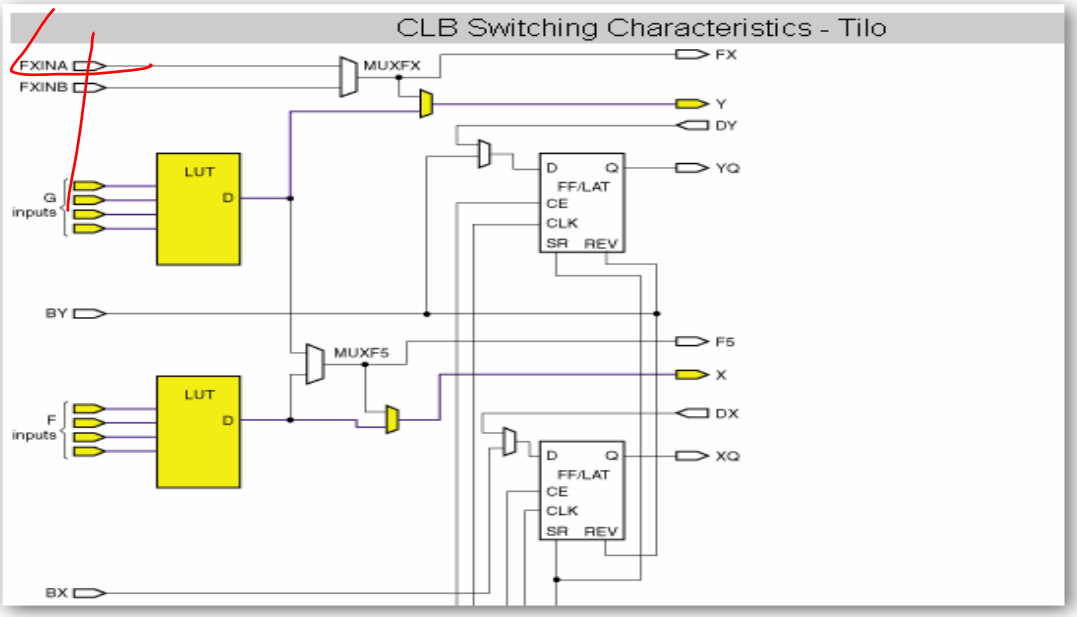


RAM_416/N_1_ret_0i-→ RAM_416/DOUTB_ret_1

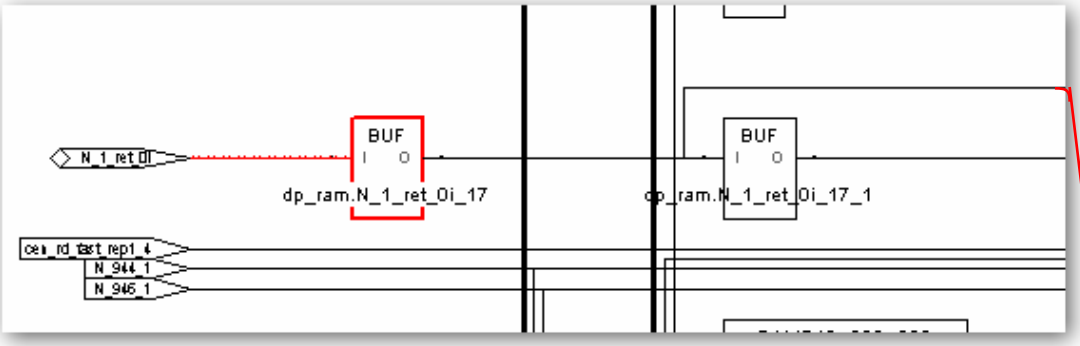


RAM_416/dp_ram.N_1_ret_0i_17(左边)→ RAM_416/DOUTB_ret_1（右边）

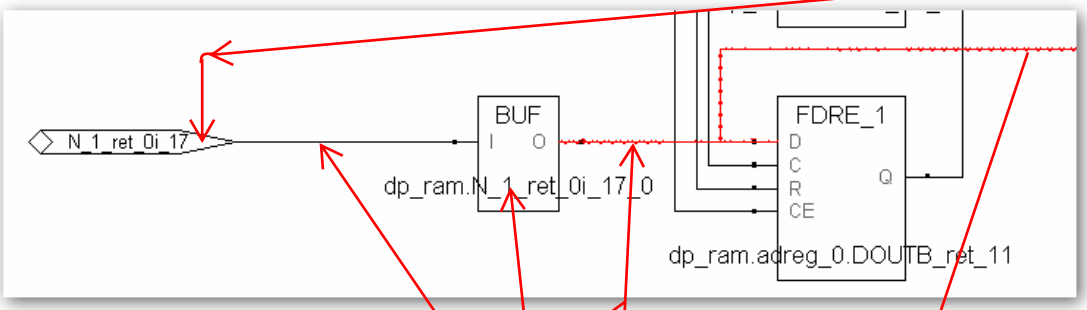
RAM_416/dp_ram.N_1_ret_0i_17? ? ? ? ?



RAM_416/DOUTB_ret_12（下图buf的输入）→RAM_416/dp_ram.N_1_ret_0i_17_0(第二图中的第一个BUF)

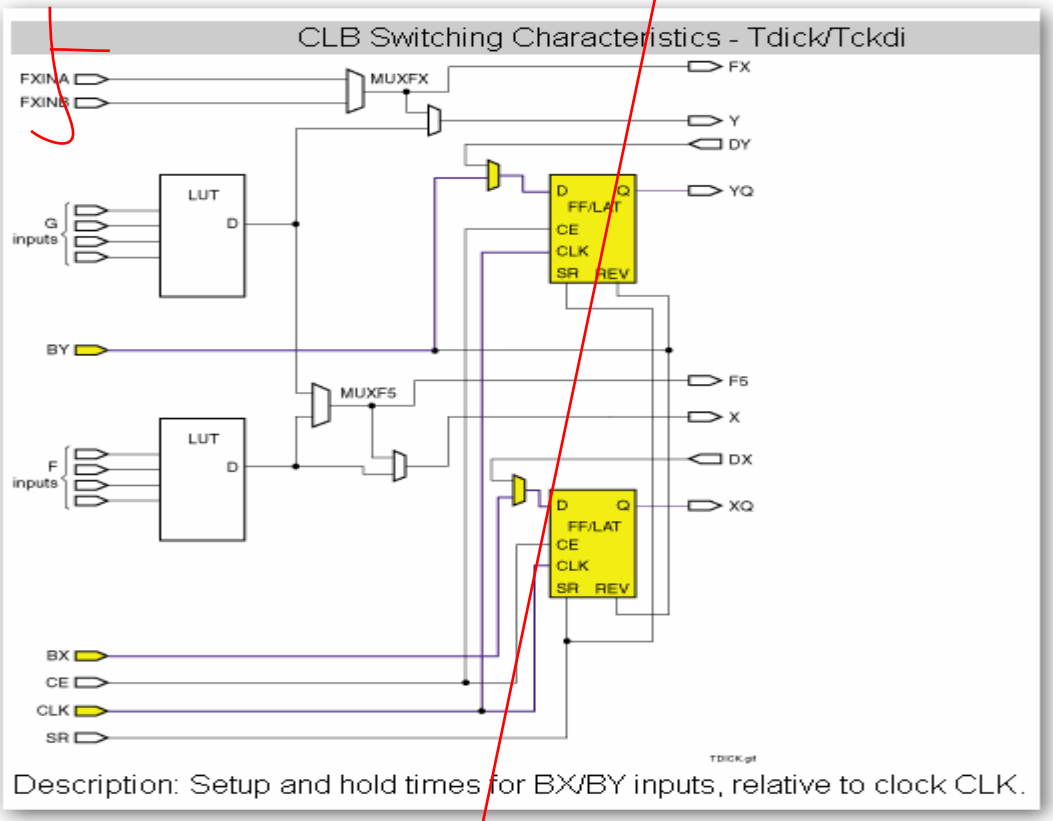


（上面这个BUF的输出就是这个BUF的输入）



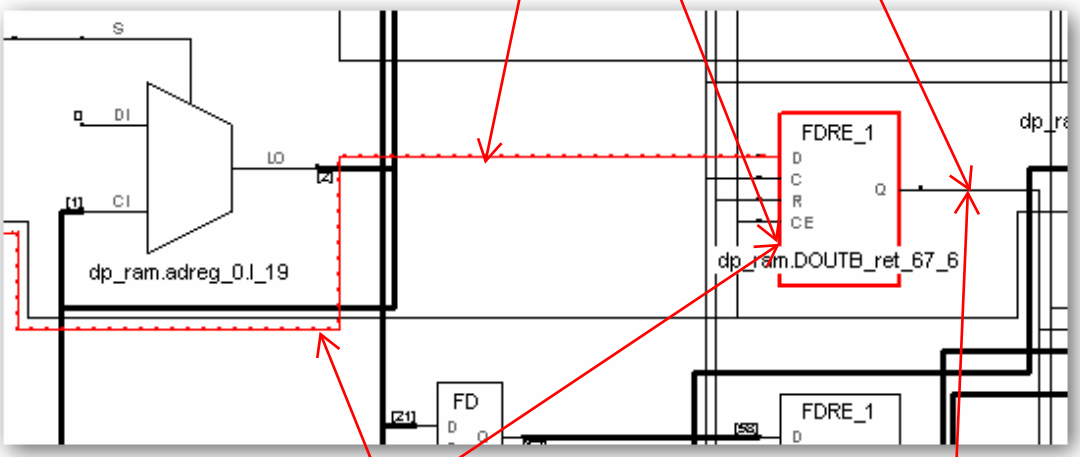
RAM_416/N_1_ret_0i_17_0（上图中的红线）

Tilo	0.382	RAM_416/DOUTB_ret_12
		RAM_416/dp_ram.N_1_ret_0i_17_0
net (fanout=8)	1.630	RAM_416/N_1_ret_0i_17_0 route



Tdick 0.322 RAM_416/DOUTB_ret_67_6

RAM_416/dp_ram.DOUTB_ret_67_6 route



上图中左边的进入的是RAM_416/N_1_ret_0i_17_0（红线）

-->RAM_416/DOUTB_ret_67_6(FDER上图)--> RAM_416/dp_ram.DOUTB_ret_67_6

（FDRE的输出）