Chapter 8. Using MAX II Devices in Multi-Voltage Systems

MII51009-1.6

Introduction

Technological advancements in deep submicron processes have lowered the supply voltage levels of semiconductor devices, creating a design environment where devices on a system board may potentially use many different supply voltages such as 5.0, 3.3, 2.5, 1.8, and 1.5 V, which can ultimately lead to voltage conflicts.

To accommodate interfacing with a variety of devices on system boards, MAX® II devices have MultiVolt I/O interfaces that allow devices in a mixed-voltage design environment to communicate directly with MAX II devices. The MultiVolt interface separates the power supply voltage (V_{CCINT}) from the output voltage (V_{CCIO}), enabling MAX II devices to interface with other devices using a different voltage level on the same printed circuit board (PCB).

Additionally, the MAX II device family supports the MultiVolt core feature. For 1.8-V operation, use the MAX IIG or MAX IIZ devices. The 1.8-V input directly powers the core of the devices. For 2.5-V or 3.3-V operation, use the MAX II devices. MAX II devices that support 2.5-V and 3.3-V operation have an internal voltage regulator that regulates at 1.8 V.

This chapter discusses several features that allow you to implement Altera® devices in multiple-voltage systems without damaging the device or the system, including:

- Hot Socketing—Insert or remove MAX II devices to and from a powered-up system without affecting the device or system operation
- Power-Up Sequence Flexibility—MAX II devices can accommodate any possible power-up sequence
- Power-On Reset—MAX II devices maintain a reset state until voltage is within operating range

This chapter contains the following sections:

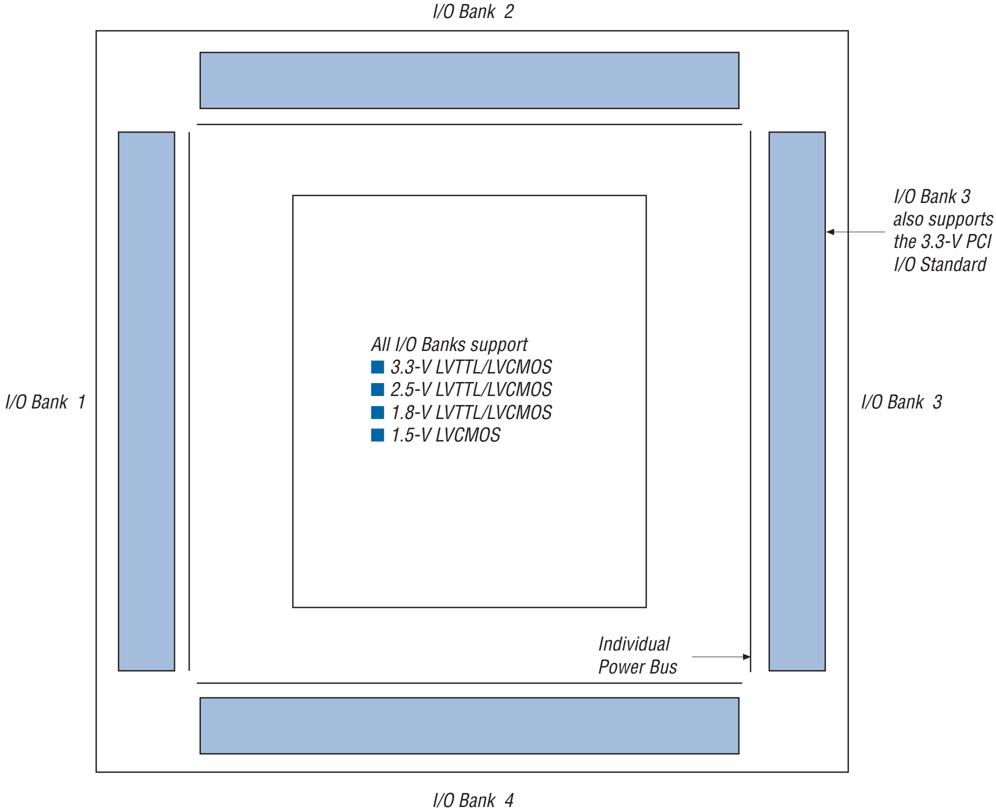
I/O Standards

The I/O buffer of MAX II devices is programmable and supports a wide range of I/O voltage standards. Each I/O bank in a MAX II device can be programmed to comply with a different I/O standard. All I/O banks can be configured with the following standards:

- 3.3-V LVTTL/LVCMOS
- 2.5-V LVTTL/LVCMOS
- 1.8-V LVTTL/LVCMOS
- 1.5-V LVCMOS

The Schmitt trigger input option is supported by the 3.3-V and 2.5-V I/O standards. The I/O Bank 3 also includes 3.3-V PCI I/O standard interface capability on the EPM1270 and EPM2210 devices. See Figure 8–1.

Figure 8–1. I/O Standards Supported by MAX II Devices *Notes (1), (2), (3), (4), (5)*



Notes to Figure 8–1:

(1) Figure 8–1 is a top view of the silicon die.

(2) Figure 8–1 is a graphical representation only. Refer to the pin list and the Quartus® II software for exact pin locations.

(3) EPM240 and EPM570 devices only have two I/O banks.

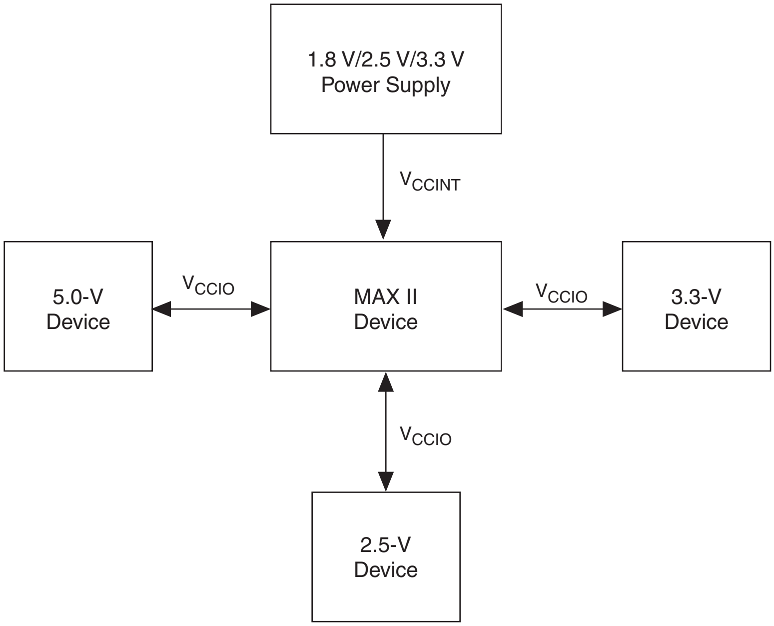
(4) The 3.3-V PCI I/O standard is only supported in EPM1270 and EPM2210 devices.

(5) The Schmitt trigger input option for 3.3-V and 2.5-V I/O standards is supported for all I/O pins.

MultiVolt Core and I/O Operation

MAX II devices include MultiVolt core I/O operation capability, allowing the core and I/O blocks of the device to be powered-up with separate supply voltages. The `VCCINT` pins supply power to the device core and the `VCCIO` pins supply power to the device I/O buffers. The `VCCINT` pins can be powered-up with 1.8 V for MAX IIG and MAX IIZ devices or 2.5/3.3 V for MAX II devices. All the `VCCIO` pins for a given I/O bank that have MultiVolt capability should be supplied from the same voltage level (for example, 5.0, 3.3, 2.5, 1.8, or 1.5 V). See Figure 8–2.

Figure 8–2. Implementing a Multiple-Voltage System with a MAX II Device Notes (1), (2), (3), (4)



Notes to Figure 8–2:

(1) For MAX IIG and MAX IIZ devices, `VCCINT` pins will only accept a 1.8-V power supply.

(2) For MAX II devices, `VCCINT` pins will only accept a 2.5-V or 3.3-V power supply.

(3) MAX II devices can drive a 5.0-V TTL input when V_{CCIO} = 3.3 V. To drive a 5.0-V CMOS, an open-drain setting with internal PCI clamp diode and external resistor are required.

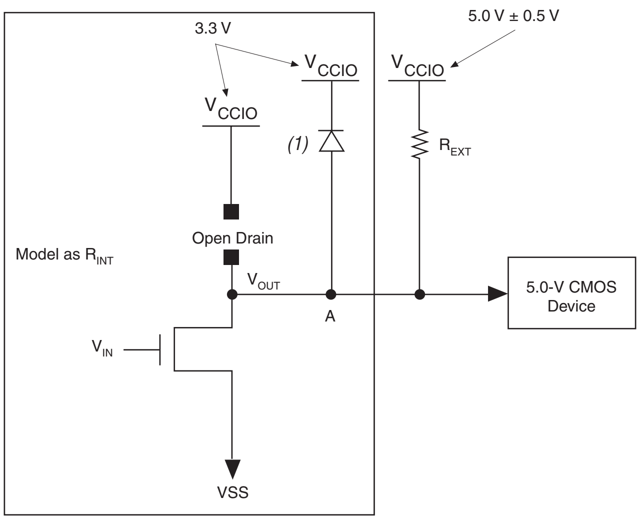
(4) MAX II devices can be 5.0-V tolerant with the use of an external resistor and the internal PCI clamp diode on EPM1270 and EPM2210 devices.

5.0-V Device Compatibility

A MAX II device can drive a 5.0-V TTL device by connecting the `VCCIO` pins of the MAX II device to 3.3 V. This is possible because the output high voltage (V_{OH}) of a 3.3-V interface meets the minimum high-level voltage of 2.4 V of a 5.0-V TTL device.

A MAX II device may not correctly interoperate with a 5.0-V CMOS device if the output of the MAX II device is connected directly to the input of the 5.0-V CMOS device. If the MAX II device's V_{OUT} is greater than V_{CCIO}, the PMOS pull-up transistor still conducts if the pin is driving high, preventing an external pull-up resistor from pulling the signal to 5.0 V. To make MAX II device outputs compatible with 5.0-V CMOS devices, configure the output pins as open-drain pins with the PCI clamp diode enabled, and use an external pull-up resistor. See Figure 8–3.

Figure 8–3. MAX II Device Compatibility with 5.0-V CMOS Devices



Note to Figure 8–3:

(1) This diode is only active after power-up. MAX II devices require an external diode if driven by 5.0 V before power-up.

The open-drain pin never drives high, only low or tri-state. When the open-drain pin is active, it drives low. When the open-drain pin is inactive, the pin is tri-stated and the trace pulls up to 5.0 V by the external resistor. The purpose of enabling the PCI clamping diode is to protect the MAX II device's I/O pins. The 3.3-V V_{CCIO} supplied to the PCI clamping diodes causes the voltage at point A to clamp at 4.0 V, which meets the MAX II device's reliability limits when the trace voltage exceeds 4.0 V. The device operates successfully because a 5.0-V input is within its input specification.

The PCI clamping diode is only supported in the EPM1270 and EPM2210 device's I/O Bank 3. An external protection diode is needed for other I/O banks in EPM1270 and EPM2210 devices and all I/O pins in EPM240 and EPM570 devices.

The pull-up resistor value should be small enough for sufficient signal rise time, but large enough so that it does not violate the I_{OL} (output low) specification of MAX II devices.

The maximum MAX II device I_{OL} depends on the programmable drive strength of the I/O output. Table 8–1 shows the programmable drive strength settings that are available for the 3.3-V LVTTL/LVCMOS I/O standard for MAX II devices. The Quartus II software uses the maximum current strength as the default setting. The PCI I/O standard is always set at 20 mA with no alternate setting.

Table 8–1. 3.3-V LVTTL/LVCMOS Programmable Drive Strength

I/O Standard	I_{OH}/I_{OL} Current Strength Setting (mA)
3.3-V LVTTL	16
	8
3.3-V LVCMOS	8
	4

To compute the required value of R_{EXT}, first calculate the model of the open-drain transistors on the MAX II device. This output resistor (R_{EXT}) can be modeled by dividing V_{OL} by I_{OL} ($R_{EXT} = V_{OL}/I_{OL}$). Table 8–2 shows the maximum V_{OL} for the 3.3-V LVTTL/LVCMOS I/O standard for MAX II devices.

For more information about I/O standard specifications, refer to the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*.

Table 8–2. 3.3-V LVTTL/LVCMOS Maximum V_{OL}

I/O Standard	Voltage (V)
3.3-V LVTTL	0.45
3.3-V LVCMOS	0.20

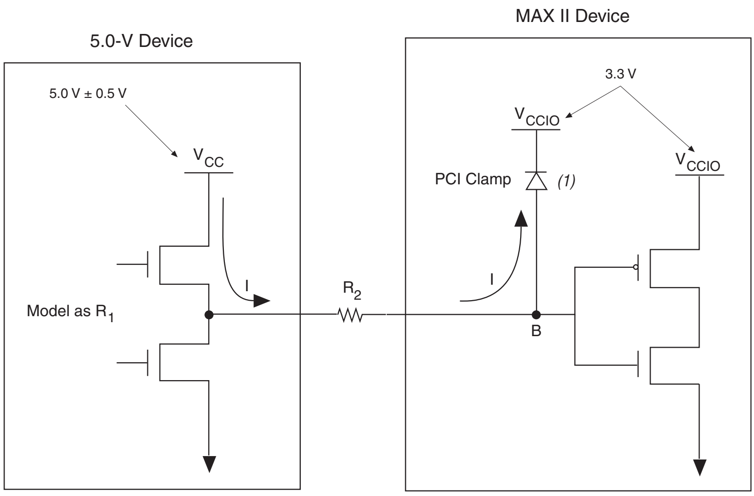
Select R_{EXT} so that the MAX II device's I_{OL} specification is not violated. You can compute the required pull-up resistor value of R_{EXT} by using the equation: $R_{EXT} = (V_{CC}/I_{OL}) - R_{INT}$. For example, if an I/O pin is configured as a 3.3-V LVTTL with a 16 mA drive strength, given that the maximum power supply (V_{CC}) is 5.5 V, the value of R_{EXT} can be calculated as follows:

$$R_{EXT} = \frac{(5.5\text{ V} - 0.45\text{ V})}{16\text{ mA}} = 315.6\ \Omega$$

This resistor value computation assumes worst-case conditions. You can adjust the R_{EXT} value according to the device configuration drive strength. Additionally, if your system does not see a wide variation in voltage-supply levels, you can adjust these calculations accordingly.

Because MAX II devices are 3.3-V, 32-bit, 66-MHz PCI compliant, the input circuitry accepts a maximum high-level input voltage (V_{IH}) of 4.0 V. To drive a MAX II device with a 5.0-V device, you must connect a resistor (R_2) between the MAX II device and the 5.0-V device. See Figure 8–4.

Figure 8–4. Driving a MAX II PCI-Compliant Device with a 5.0-V Device



Note to Figure 8–4:

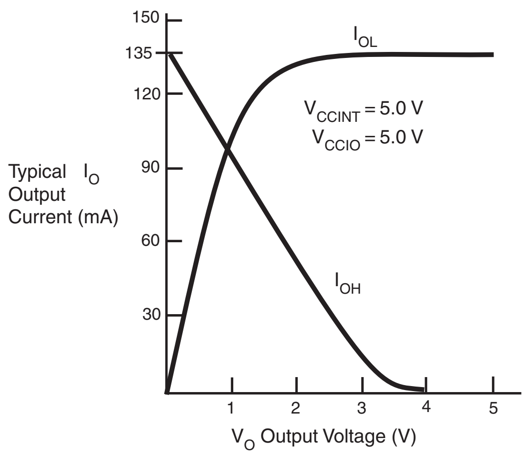
(1) This diode is only active after power-up. MAX II devices require an external diode if driven by 5.0 V before power-up.

If V_{CCIO} for MAX II devices is 3.3 V and the PCI clamping diode is enabled, the voltage at point B in Figure 8–4 is 4.0 V, which meets the MAX II devices reliability limits when the trace voltage exceeds 4.0 V. To limit large current draw from the 5.0-V device, R_2 should be small enough for a fast signal rise time and large enough so that it does not violate the high-level output current (I_{OH}) specifications of the devices driving the trace.

To compute the required value of R_2, first calculate the model of the pull-up transistors on the 5.0-V device. This output resistor (R_1) can be modeled by dividing the 5.0-V device supply voltage (V_{CC}) by the I_{OH}: $R_1 = V_{CC}/I_{OH}$.

Figure 8–5 shows an example of typical output drive characteristics of a 5.0-V device.

Figure 8–5. Output Drive Characteristics of a 5.0-V Device



As shown above, $R_1 = 5.0\text{ V}/135\text{ mA}$.

The values usually shown in data sheets reflect typical operating conditions. Subtract 20% from the data sheet value for guard band. This subtraction applied to the above example gives R_1 a value of 30.

Select R_2 so that the MAX II device's I_{OH} specification is not violated. For example, if the above device has a maximum I_{OH} of 8 mA, given the PCI clamping diode, $V_{IN} = V_{CCIO} + 0.7\text{ V} = 3.7\text{ V}$. Given that the maximum supply load of a 5.0-V device (V_{CC}) is 5.5 V, the value of R_2 can be calculated as follows:

$$R_2 = \frac{(5.5\text{ V} - 3.7\text{ V}) - (8\text{ mA} \times 30\ \Omega)}{8\text{ mA}} = 194\ \Omega$$

This analysis assumes worst-case conditions. If your system does not see a wide variation in voltage-supply levels, you can adjust these calculations accordingly.

Because 5.0-V device tolerance in MAX II devices requires use of the PCI clamp, and this clamp is activated only after power-up, 5.0-V signals may not be driven into the device until it is configured. The PCI clamping diode is only supported in the EPM1270 and EPM2210 devices' I/O Bank 3. An external protection diode is needed for other I/O banks for EPM1270 and EPM2210 devices and all I/O pins in EPM240 and EPM570 devices.

Recommended Operating Condition for 5.0-V Compatibility

As mentioned earlier, a 5.0-V tolerance can be supported with the PCI clamp diode enable with external series/pull-up resistance. To guarantee long term reliability of the device's I/O buffer, there are restrictions on the signal duty cycle that drive the MAX II I/O, which is based on the maximum clamp current. Table 8–3 shows the maximum signal duty cycle for 3.3-V V_{CCIO} given a PCI clamp current-handling capability.

Table 8–3. Maximum Signal Duty Cycle

V_{IN} (V) *(1)*	I_{CH} (mA) *(2)*	Max Duty Cycle (%)
4.0	5.00	100
4.1	11.67	90
4.2	18.33	50
4.3	25.00	30
4.4	31.67	17
4.5	38.33	10
4.6	45.00	5

Notes to Table 8–3:
(1) V_{IN} is the voltage at the package pin.
(2) The I_{CH} is calculated with a 3.3-V V_{CCIO}. A higher V_{CCIO} value will have a lower I_{CH} value with the same V_{IN}.

For signals with duty cycle greater than 30% on MAX II input pins, Altera recommends a V_{CCIO} voltage of 3.0 V to guarantee long-term I/O reliability. For signals with duty cycle less than 30%, the V_{CCIO} voltage can be 3.3 V.

Hot Socketing

For information about hot socketing, refer to the *Hot Socketing and Power-On Reset in MAX II Devices* chapter in the *MAX II Device Handbook*.

Power-Up Sequencing

MAX II devices are designed to operate in multiple-voltage environments where it may be difficult to control power sequencing. Therefore, MAX II devices are designed to tolerate any possible power-up sequence. Either V_{CCINT} or V_{CCIO} can initially supply power to the device, and 3.3-V, 2.5-V, 1.8-V, or 1.5-V input signals can drive the devices without special precautions before V_{CCINT} or V_{CCIO} is applied. MAX II devices can operate with a V_{CCIO} voltage level that is higher than the V_{CCINT} level.

When V_{CCIO} and V_{CCINT} are supplied from different power sources to a MAX II device, a delay between V_{CCIO} and V_{CCINT} may occur. Normal operation does not occur until both power supplies are in their recommended operating range. When V_{CCINT} is powered-up, the IEEE Std. 1149.1 Joint Test Action Group (JTAG) circuitry is active. If the `TMS` and `TCK` are connected to V_{CCIO} and V_{CCIO} is not powered-up, the JTAG signals are left floating. Thus, any transition on `TCK` can cause the state machine to transition to an unknown JTAG state, leading to incorrect operation when V_{CCIO} is finally powered-up. To disable the JTAG state during the power-up sequence, `TCK` should be pulled low to ensure that an inadvertent rising edge does not occur on `TCK`.

Power-On Reset

For information about Power-On Reset (POR), refer to the *Hot Socketing and Power-On Reset in MAX II Devices* chapter in the *MAX II Device Handbook*.

Conclusion

MAX II devices have MultiVolt I/O support, allowing 1.5-V, 1.8-V, 2.5-V, and 3.3-V devices to interface directly with MAX II devices without causing voltage conflicts. In addition, MAX II devices can interface with 5.0-V devices by slightly modifying the external hardware interface and enabling PCI clamping diodes via the Quartus II software. This MultiVolt capability also enables the device core to run at its core voltage, V_{CCINT}, while maintaining I/O pin compatibility with other devices. Altera has taken further steps to make system design easier by designing devices that allow V_{CCINT} and V_{CCIO} to power-up in any sequence and by incorporating support for hot socketing.

Referenced Documents

This chapter references the following documents:

- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*
- *Hot Socketing and Power-On Reset in MAX II Devices* chapter in the *MAX II Device Handbook*

Document Revision History

Table 8–4 shows the revision history for this chapter.

Table 8–4. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
December 2007 v1.6	• Updated "Introduction" section. • "MultiVolt Core and I/O Operation" section. • Updated *Note (1)* to Figure 8–2. • Added "Referenced Documents" section.	Updated document with MAX IIZ information.
December 2006 v1.5	Added document revision history.	—
August 2006 v1.4	Updated "5.0-V Device Compatibility" section.	—
February 2006 v1.3	Updated Figure 8–3.	—
January 2005 v1.2	Previously published as Chapter 9. No changes to content.	—
December 2004 v1.1	Corrected typographical errors in Note 3 of Figure 8–2.	—