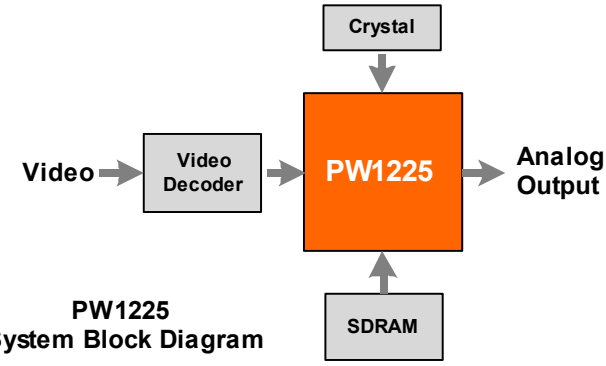
PW1225

Product Specification

General

The PW1225 is a high-quality, digital video signal processor that incorporates Pixelworks' patented deinterlacing, scaling, and video enhancement algorithms. The PW1225 accepts industry-standard video formats and resolutions, and converts the input into any desired output format.The video algorithms are highly efficient, providing excellent quality video.

The PW1225 Video SignalProcessor combines many functions into a single device, including SVM, triple Digital-to-Analog Converter (DAC), memory controller, auto-configuration, and others. This high level of integration enables simple, flexible, cost-effective solutions featuring fewer required components.



PW1225
System Block Diagram

Features

- SVM
- Built-In Memory Controller
- Motion-Adaptive Deinterlace Processor
- Intelligent Edge Deinterlacing
- Digital Color/Luminance Transient Improvement (DCTI/DLTI)
- Interlaced Video Input Options, including NTSC and PAL
- Independent horizontal and vertical scaling
- Copy Protection
- Two-Wire Serial Interface

Applications:
For use with Analog Displays

- Progressive Scan CRT TVs
- Rear Projection TVs
- Progressive Scan DVD Players

Device	Application	Package
PW1225	Up to XGA	160-pin PQF

pixelworks

8100 SW Nyberg Road
Tualatin, OR 97062 USA
Telephone: 503.454.1750
FAX: 503.612.0848
www.pixelworks.com

P/N 001-0072-10 Rev C
December 2002

CONFIDENTIAL

Copyright © 2002 by Pixelworks, Inc. All rights reserved.

Pixelworks owns all right, title and interest in the property and products described herein, unless otherwise indicated. No part of this document may be translated to another language or produced or transmitted in any form or by any information storage and retrieval system without written permission from Pixelworks.

Pixelworks reserves the right to change products and specifications without written notice. Customers are advised to obtain the latest versions of any product specifications.

PIXELWORKS MAKES NO WARRANTIES, EXPRESSED OR IMPLIED, OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OTHER THAN COMPLIANCE WITH THE APPLICABLE PIXELWORKS SPECIFICATION SHEET FOR THE PRODUCT AT THE TIME OF DELIVERY. IN NO EVENT SHALL PIXELWORKS BE LIABLE FOR ANY INDIRECT, INCIDENTAL OR CONSEQUENTIAL DAMAGES AS A RESULT OF THE PRODUCT'S PERFORMANCE OR FAILURE TO MEET ANY ASPECT OF SUCH SPECIFICATION.

PIXELWORKS PRODUCTS ARE NOT DESIGNED OR INTENDED FOR USE IN LIFE SUPPORT APPLIANCES, DEVICES OR SYSTEMS WHERE A MALFUNCTION OF A PIXELWORKS DEVICE COULD RESULT IN A PERSONAL INJURY OR LOSS OF LIFE. CUSTOMERS USING OR SELLING PIXELWORKS DEVICES FOR USE IN SUCH APPLICATIONS DO SO AT THEIR OWN RISK AND AGREE TO FULLY INDEMNIFY PIXELWORKS FOR ANY DAMAGES RESULTING FROM SUCH IMPROPER USE OR SALE.

Information contained herein is presented only as a guide for the applications of our products. Pixelworks does not warrant this product to be free of claims of patent infringement by any third party and disclaims any warranty or indemnification against patent infringement. No responsibility is assumed by Pixelworks for any patent infringement resulting from use of its products by themselves or in combination with any other products.

No license is hereby granted by implication or otherwise under any patent or patent rights of Pixelworks or others. The products described herein may be protected by US Patent No. 6,339,434 with other foreign and domestic patents pending. Other restrictions of rights may also apply.

Trademarks

Pixelworks and Fail-Safe are trademarks of Pixelworks, Inc. All other brand names, product names, trademarks, and registered trademarks are the property of their respective owners.

Visit our web page at www.pixelworks.com

For support requests, contact us at support@pixelworks.com

For documentation suggestions, corrections, or requests, contact techpubs@pixelworks.com

Revision History

Revision	Date	Description of Changes
LIMITED RELEASE	October 2002	Preliminary draft. LIMITED RELEASE.
P/N 001-0072-10 Rev A	November 2002	Added Pin Diagram. Added Theory of Operations.
P/N 001-0072-10 Rev B	December 2002	Minor edits.
P/N 001-0072-10 Rev C	December 2002	Edits to clarify product features.

CONFIDENTIAL

Contents

Chapter 4: Theory of Operations

Chapter 5: Register Maps

1

Functional Description

This chapter provides an overview of the PW1225 Video SignalProcessor, and describes the features and modes of operation.

1.1 Features

The PW1225 Video SignalProcessor offers the following features:

- Input Unit
- Programming Unit
- Memory Unit
- PLL and Oscillator
- Display Unit

Figure 1-1 provides a detailed functional block diagram of the PW1225 Video SignalProcessor, with descriptions of each functional areas shown provided later in this chapter.

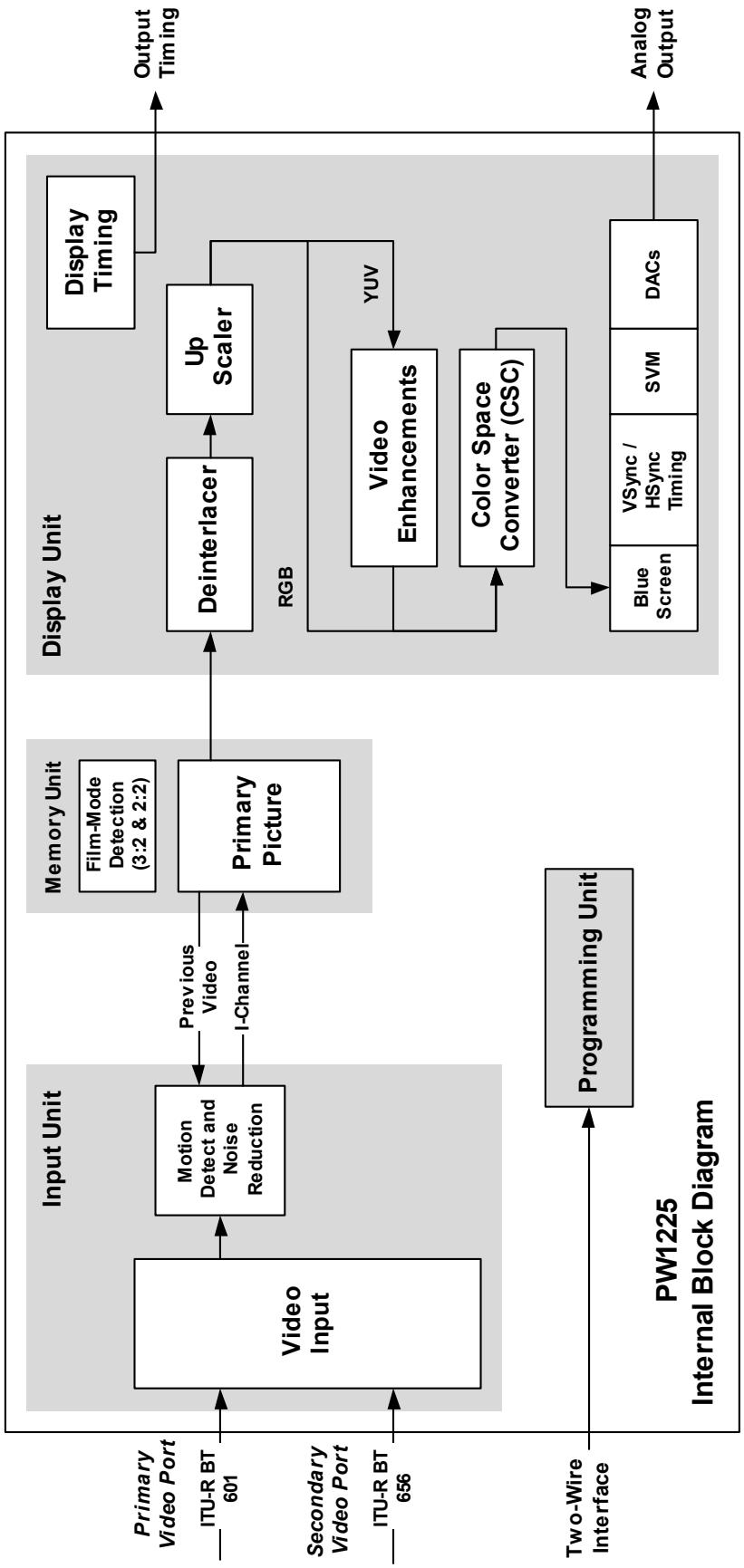


Figure 1-1 Internal Block Diagram

1.2 Input Ports

The PW1225 supports acquisition on either of the following input ports:

- Primary Video (PV) Port, primarily for ITU-R BT601 connections
- Secondary Video (SV) Port, primarily for ITU-R BT656 connections

Each input port has its own sync decoder and automatic image optimization circuitry.

1.2.1 Video Input Ports

The Primary Video (PV) Port and Secondary Video (SV) Port are generally used to support video inputs. These ports are designed to work directly with popular digital video decoders and MPEG decoders.

- The Primary Video (PV) Port supports standard interlaced video in the ITU-R BT601 (4:1:1, 4:2:2, and 4:4:4 YUV) data format.
- The Secondary Video (SV) Port supports standard interlaced video in the ITU-R BT656 (4:2:2 YUV) data format.

1.3 I-Channel

The I-Channel performs pixel-based motion detection and noise reduction on interlaced video.

1.3.1 PLL and Oscillator

The PW1225 integrates several PLLs to generate the MCLK to the Memory interface and the DCLK to the display. Only an external crystal or clock oscillator is required to be connected to the XTALI pin. On power-up, these PLLs are initialized to provide an 80 MHz MCLK and a 27MHz DCLK when a 10MHz reference is used. Alternatively, the MCLK and DCLK can be driven directly by external clocks.

1.3.2 Memory Controller

The internal Memory Controller supports addressing and control of the external SDRAM. The external SDRAM memory buffer is used to store video fields and motion data. Generally, 2MB of storage is required for NTSC input and 4MB of storage is required for PAL inputs. The Memory Controller also supports frame rate up-conversion with different input and output refresh rates.

1.3.3 Deinterlace Processor

The Deinterlace Processor automatically determines the type of incoming video content – film, static interlaced video and moving interlaced video. Different algorithms are applied for each of the content types.

The PW1225 incorporates a per-pixel, motion-compensated architecture to produce artifact-free progressive scan video signals. Video content is analyzed on a single pixel granularity to detect presence or absence of noise and compute the amount of motion. Motion video is processed using a highly intelligent DNX^{TM} algorithm that *simultaneously* eliminates noise and interpolates pixels along any angle to produce a noise-free picture without jagged-edge artifacts.

The Deinterlace Processor detects film-originated content by analyzing consecutive images and detecting a 3:2 or 2:2 pull-down pattern. Film-originated content is deinterlaced by merging the two fields from the original frame.

1.4 Video Scalers

The Video Scalers provide high-quality video up scaling. The PW1225 incorporates a flexible video scaling architecture using the latest Pixelworks processing. The vertical and horizontal scaling factors are independently programmable.

1.5 Video Enhancer

The Video Enhancer is a high-quality programmable processor that brings out details and color in the video. The PW1225 improves sharpness in three ways:

- First, by increasing the slope of large luminance transients of vertical features (DLTI) and enhancing transient details in natural scenes (luminance peaking).
- Second, our digital color transient improvement (DCTI) logic improves the color transitions of vertical objects and reduces color smearing introduced by the video decoder.
- Finally, our black level expansion logic offers the capability of giving a programmably larger weight to the black parts of the video signals.

Brightness, contrast, hue, and saturation controls are also built into the video enhancer.

1.6 Analog Display Port

The Analog Display Port generates analog RGB, YUV, or YPbPr with triple 10-bit Digital-to-Analog Converters (DACs). The analog RGB or YUV output is generated in synchronization with timing signals.

1.7 2-Wire Bus Slave Interface

Access to the PW1225 registers is provided by a 2-wire serial bus interface. Only slave mode is supported in the PW1225 Video SignalProcessor.

2

Pinout Information

2.1 Pin Diagram

The PW1225 Video SignalProcessor is manufactured in a 160-pin PQFP package. The pin locations are shown in Figure 2-1. The remainder of this chapter provides descriptions for these pins. Refer to Table 2-9, on page 2-7, at the end of this chapter for a list of pinouts by pin number.

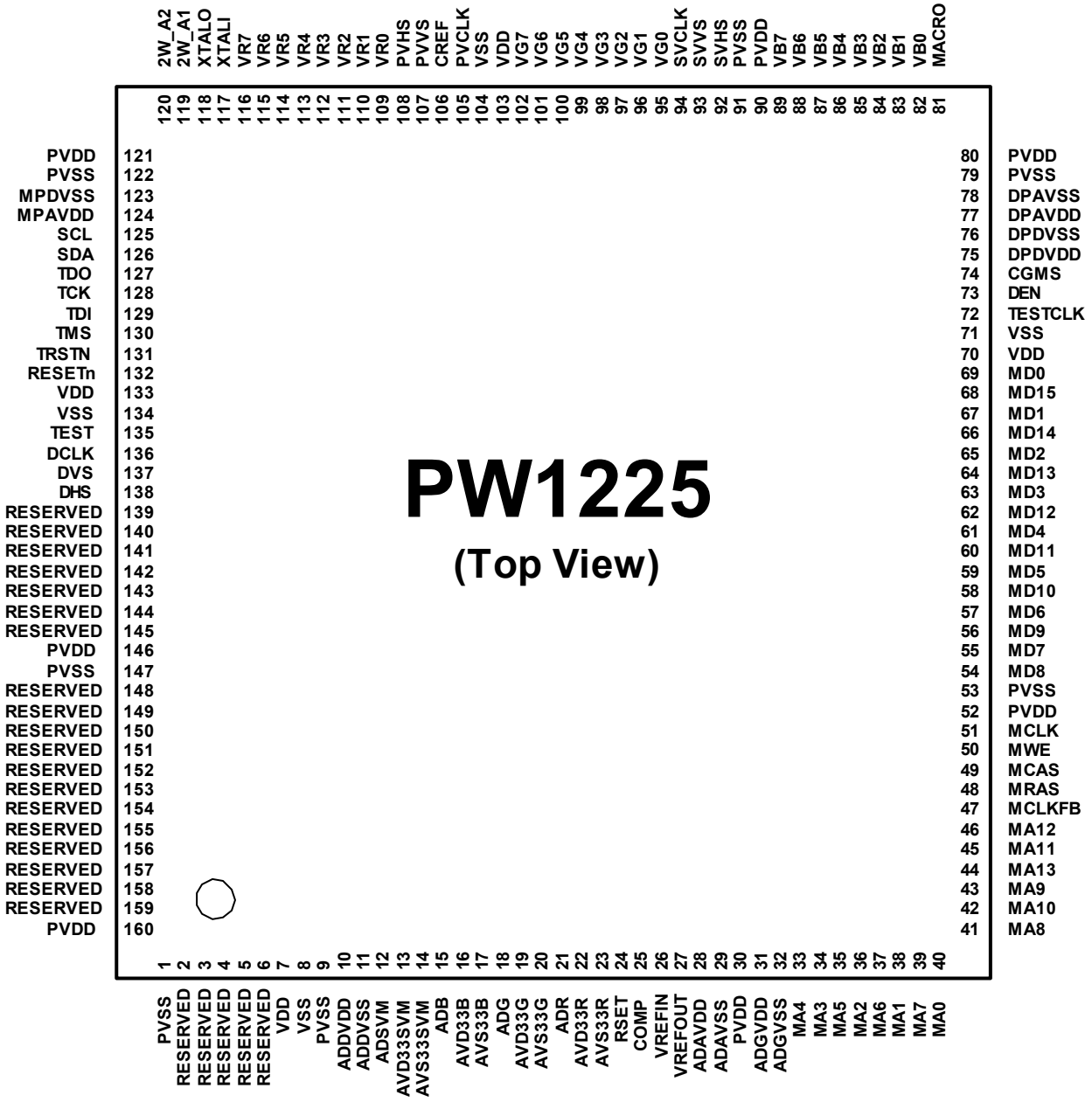


Figure 2-1 PW1225 Pin Layout

2.2 Pin Descriptions

Pin types include the following:

- I Input
- IU Input with pull-up
- ID Input with pull-down
- O Output
- I/O Bidirectional (input/output)
- P Power
- GND Ground
- NC No connect

2.2.1 Clock Generator Pins

Table 2-1 provides detailed pin descriptions for the Clock Generator.

Table 2-1 Clock Generator Pin Descriptions

Name	Pin(s)	Type	Function
XTALI	117	I	External crystal input for the fixed clock *fclk*. Connect to a 10 MHz crystal. Analog.
XTALO	118	O	External crystal output for the fixed clock *fclk*. Connect to a 10 MHz crystal. Analog.
TESTCLK	72	I/O	Test clock (5v-to1, 8mA). • When test=0, use for external DCLK source. • When test=1 and 2W_a1=0, use as display clock PLL test output. • When test=1 and 2W_a1=1, use as display clock PLL test output.
MPAVDD	124	P	Power pin for the memory clock PLL.
MPDVSS	123	GND	Ground pin for the memory clock PLL.
DPDVDD	75	P	Digital power pin for the display clock PLL.
DPAVDD	77	P	Analog power pin for the display clock PLL.
DPDVSS	76	GND	Digital ground pin for the display clock PLL.
DPAVSS	78	GND	Analog ground pin for the display clock PLL.

2.2.2 System Interface Pins

Table 2-2 provides detailed pin descriptions for the System Interface.

Table 2-2 System Interface Pin Descriptions

Name	Pin(s)	Type	Function
RESETn	132	I	Asynchronous reset. Asserting this signal initializes the IC to a known state. Active low. Must be continuously asserted for a minimum of 100 µs after power-up to satisfy the SDRAM power-up requirement.
2W_A1	119	I	Programmable address bit 1 of the 2-wire bus (5V-to1).
2W_A2	120	I	Programmable address bit 2 of the 2-wire bus (5V-to1).
SCL	125	I	Clock signal for the 2-wire bus (5V-to1, pull-up).
SDA	126	I/O	Data signal for the 2-wire bus (5V-to1, 2mA, pull-up).
TEST	135	I	Test mode enable. Active high (5V-to1, pull-down).

2.2.3 JTAG Interface Pins

Table 2-3 provides detailed pin descriptions for the JTAG Interface.

Table 2-3 JTAG Interface Pin Descriptions

Name	Pin(s)	Type	Function
TCK	128	I	Test/Debug port test data clock (5V-tol).
TDI	129	I	Test/Debug port test data in (5V-tol, pull-down).
TDO	127	O	Test/Debug port test data out (5V-tol, 2mA).
TMS	130	I	Test/Debug port test mode select (5V-tol, pull-down).
TRSTN	131	I	Test/Debug port reset. Must be driven low during power-on (5V-tol, pull-down).

2.2.4 Video Input Pins

Table 2-4 provides detailed descriptions for Video Input Pins.

Table 2-4 Video Input Pin Descriptions

Name	Pin(s)	Type	Function
VG[7:0]	95–102	I	Video Green (5V-tol). Y data for 4:4:4 and 16-bit 4:2:2 modes.
VB[7:0]	82–89	I	Video Blue (5V-tol). • U data in 4:4:4 mode. • ITU656 data in 8-bit 4:2:2 mode.
VR[7:0]	109–116	I	Video Red (5V-tol). • V data in 4:4:4 mode. • UV data in 16-bit 4:2:2 mode.
SVCLK	94	I	Input clock for 8-bit 4:2:2 mode (5V-tol, pull-down).
SVVS	93	I/O	Vertical sync for 8-bit 4:2:2 mode (5V-tol, 8mA).
SVHS	92	I/O	Horizontal sync for 8-bit 4:2:2 mode (5V-tol, 8mA).
PVCLK	105	I	Input clock for 4:4:4 and 16-bit 4:2:2 modes (5V-tol, pull-down).
PVVS	107	I	Vertical sync for 4:4:4 and 16-bit 4:2:2 modes (5V-tol).
PVHS	108	I	Horizontal sync for 4:4:4 and 16-bit 4:2:2 modes (5V-tol).

2.2.5 SDRAM Interface Pins

Table 2-5 provides detailed pin descriptions for SDRAM Interface.

Table 2-5 SDRAM Interface Pin Descriptions

Name	Pin(s)	Type	Function
MA[13:0]	33–40	O	Memory address bus (4maA). Multiplexed row and column address and bank select. Row addresses use MA[11:0] for 8MB SDRAM and MA[10:0] for 2MB SDRAM. Column addresses use MA[7:0]. Note that MA[10] is a control signal during column address strobing and precharging. • For 8MB SDRAM, bank select pins *ba0* and *ba1* should be connected to MA[12] and MA[13], respectively. • For 2MB SDRAM, *ba* should be connected to MA[12] only.
MCAS	49	O	Column address strobe (8mA). Latches column addresses on the positive edge of MCLK when low.
MCLK	51	O	Memory clock (8mA).
MCLKFB	47	I	Memory clock feedback (5V-tol). For latching in read data.
MD[15:0]	54–68	I/O	Memory data bus (8mA).
MRAS	48	O	Row address strobe (8mA). Latches row addresses on the positive edge of MCLK when low.
MWE	50	O	Memory write enable (8mA). Enables write operation and row precharge. Latches data in starting from casN and mwrN low.

2.2.6 Output Interface Pins

Table 2-6 provides detailed pin descriptions for the Output Interface.

Table 2-6 Output Interface Pin Descriptions

Name	Pin(s)	Type	Function
DCLK	136	O	Display clock for all digital outputs (4mA).
DVS	137	O	Vertical sync output for all output configurations (5V-tol, 4mA).
DHS	138	O	Horizontal sync output for all output configurations (5V-tol, 4mA).
DEN	73	I	Output enable for DCLK, DHS, and DVS (5V-to1, pull-up). Active low.
CGMS	74	I	CGMS enable (5V-to1, pull-down). Active high.
MACRO	81	I	Macrovision enable (5V-to1, pull-down). Active high.

2.2.7 Analog Back End Pins

Table 2-7 provides detailed pin descriptions for the Analog Back End.

Table 2-7 Analog Back End Pin Descriptions

Name	Pin(s)	Type	Function
ADG	18	O	Analog component video Y or G data.
ADB	15	O	Analog component video U or B data.

Table 2-7 Analog Back End Pin Descriptions (continued)

Name	Pin(s)	Type	Function
ADR	21	O	Analog component video V or R data.
ADSVM	12	O	Analog component video SVM data (alternative Y data).
COMP	25	I/O	Compensation pin. Connected through a 0.01 µF ceramic capacitor and a 10 µF tantalum capacitor to +3.3V externally.
VREFIN	26	I	Reference voltage input. Connected through a 0.01 µF ceramic capacitor to ground externally.
VREFOUT	27	O	Band-gap reference voltage output. Delivers a 1.292 V reference voltage. Does not source/sink any output current.
RSET	24	I/O	Full-scale adjust resistor. Connected through a resistor to ground. Controls the magnitude of the full-scale video signal: IO(max)=qvrefin x 2.558 / qres
ADDVSS	11	GND	Digital core ground pin for 4-channel DAC.
ADDVDD	10	P	Digital core power pin for 4-channel DAC.
ADAVSS	29	GND	Analog core ground pin for 4-channel DAC.
ADAVDD	28	P	Analog core power pin for 4-channel DAC.
AVS33SVM	14	GND	Analog I/O ground pin for Y/G channel.
AVS33R	23	GND	Analog I/O ground pin for Y/G channel.
AVS33G	20	GND	Analog I/O ground pin for U/B channel.
AVS33B	17	GND	Analog I/O ground pin for V/R channel.
AVD33SVM	13	P	Analog I/O power pin for Y/G channel.
AVD33R	22	P	Analog I/O power pin for Y/G channel.
AVD33G	19	P	Analog I/O power pin for U/B channel.
AVD33B	16	P	Analog I/O power pin for V/R channel.
ADGVDD	31	P	Analog I/O power pin for +2.5 guard ring.
ADGVSS	32	GND	Analog I/O power pin for ground guard ring.

2.2.8 Digital Power and Ground Pins

Table 2-8 provides detailed pin descriptions for Digital Power and Ground.

Table 2-8 Digital Power and Ground Pin Descriptions

Name	Pin(s)	Type	Function
VSS	8, 71, 104, 134	GND	Core ground pin.
PVSS	1, 9, 91, 53, 79, 122, 147	GND	I/O ground pin.
VDD	7, 70, 103, 133	P	Core power pin.
PVDD	30, 52, 80, 90, 121, 146, 160	P	I/O power pin.

2.3 Pin Out by Pin Number

Table 2-9 lists pin numbers and their associated pin names.

Table 2-9 Pin Outs by Pin Number

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	PVSS	41	MA8	81	MACRO	121	PVDD
2	RESERVED	42	MA10	82	VB0	122	PVSS
3	RESERVED	43	MA9	83	VB1	123	MPDVSS
4	RESERVED	44	MA13	84	VB2	124	MPAVDD
5	RESERVED	45	MA11	85	VB3	125	SCL
6	RESERVED	46	MA12	86	VB4	126	SDA
7	VDD	47	MCLKFB	87	VB5	127	TDO
8	VSS	48	MRAS	88	VB6	128	TCK
9	PVSS	49	MCAS	89	VB7	129	TDI
10	ADDVDD	50	MWE	90	PVDD	130	TMS
11	ADDVSS	51	MCLK	91	PVSS	131	TRSTN
12	ADSVM	52	PVDD	92	SVHS	132	RESETn
13	AVD33SVM	53	PVSS	93	SVVS	133	VDD
14	AVS33SVM	54	MD8	94	SVCLK	134	VSS
15	ADB	55	MD7	95	VG0	135	TEST
16	AVD33B	56	MD9	96	VG1	136	DCLK
17	AVS33B	57	MD6	97	VG2	137	DVS
18	ADG	58	MD10	98	VG3	138	DHS
19	AVD33G	59	MD5	99	VG4	139	RESERVED
20	AVS33G	60	MD11	100	VG5	140	RESERVED
21	ADR	61	MD4	101	VG6	141	RESERVED
22	AVD33R	62	MD12	102	VG7	142	RESERVED
23	AVS33R	63	MD3	103	VDD	143	RESERVED
24	RSET	64	MD13	104	VSS	144	RESERVED
25	COMP	65	MD2	105	PVCLK	145	RESERVED
26	VREFIN	66	MD14	106	CREF	146	PVDD
27	VREFOUT	67	MD1	107	PVVS	147	PVSS
28	ADAVDD	68	MD15	108	PVHS	148	RESERVED
29	ADAVSS	69	MD0	109	VR0	149	RESERVED
30	PVDD	70	VDD	110	VR1	150	RESERVED
31	ADGVDD	71	VSS	111	VR2	151	RESERVED
32	ADGVSS	72	TESTCLK	112	VR3	152	RESERVED
33	MA4	73	DEN	113	VR4	153	RESERVED
34	MA3	74	CGMS	114	VR5	154	RESERVED

Table 2-9 Pin Outs by Pin Number (continued)

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
35	MA5	75	DPDVDD	115	VR6	155	RESERVED
36	MA2	76	DPDVSS	116	VR7	156	RESERVED
37	MA6	77	DPAVDD	117	XTALI	157	RESERVED
38	MA1	78	DPAVSS	118	XTALO	158	RESERVED
39	MA7	79	PVSS	119	2W_A1	159	RESERVED
40	MA0	80	PVDD	120	2W_A2	160	PVDD

3

Electrical Specifications

This chapter describes the electrical specifications for the PW1225 Video SignalProcessor.

3.1 Absolute Maximum Ratings

Table 3-1 lists the absolute maximum ratings for the PW1225 SignalProcessor.

Table 3-1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Conditions
3.3V Digital Supply Voltage	V_{33}	-0.3	4.5	V	
2.5V Digital Supply Voltage	V_{25}	-0.3	3.6	V	
Voltage on any input	V_I	-0.3	V_{33}+0.3	V	
Storage Temperature	T_S	-40 C	125 C	C	
Soldering Temperature (30 seconds)	TSOL		230	C	

3.2 DC Specifications

Table 3-2 lists the DC electrical specifications for the SignalProcessor.

Table 3-2 DC Specifications

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Digital Inputs						
Input High Voltage	V_{IH}	2.0		V_{33}+0.3	V	
Input Low Voltage	V_{IL}	-0.3		0.8	V	
Input Low Leakage Current 1	I_{IL1}		40	$\pm$ 100	µA	Internal pull-up, V_{IL}=0
Input High Leakage Current 1	I_{IH1}		$\pm$ 0.1	$\pm$ 1	µA	Internal pull-up, V_{IH}=V_{33}
Input Low Leakage Current 2	I_{IL2}		$\pm$ 0.1	$\pm$ 1	µA	Internal pull-down, V_{IL}=0
Input High Leakage Current 2	I_{IH2}		40	$\pm$ 100	µA	Internal pull-down, V_{IH}=V_{33}
Input Capacitance	C_{IN}			8	pF	
Digital Outputs						
Output High Voltage	V_{OH}	2.4			V	
Output Low Voltage	V_{OL}			0.4	V	
Power Requirements						
3.3V Digital Power Supply	V_{33}	3.135	3.3	3.465	V	
2.5V Digital Power Supply	V_{25}	2.375	2.5	2.625	V	
3.3V Digital Supply Current	I_{33a}		0.1	0.2	A	Typical numbers are with no scaling turned on.

Table 3-2 DC Specifications (continued)

Parameter	Symbol	Min	Typ	Max	Units	Conditions
2.5V Digital Supply Current	I_{25a}		0.2	0.6	A	Typical numbers are with no scaling turned on.
Operating Temperature						
Ambient Temperature	T_A	0		70	C	
Junction Temperature	T_J	0		105	C	

3.3 Primary Video (PV) Port AC Timing Characteristics

Figure 3-1 illustrates the AC timing characteristics for the Primary Video (PV) Port on the SignalProcessor:

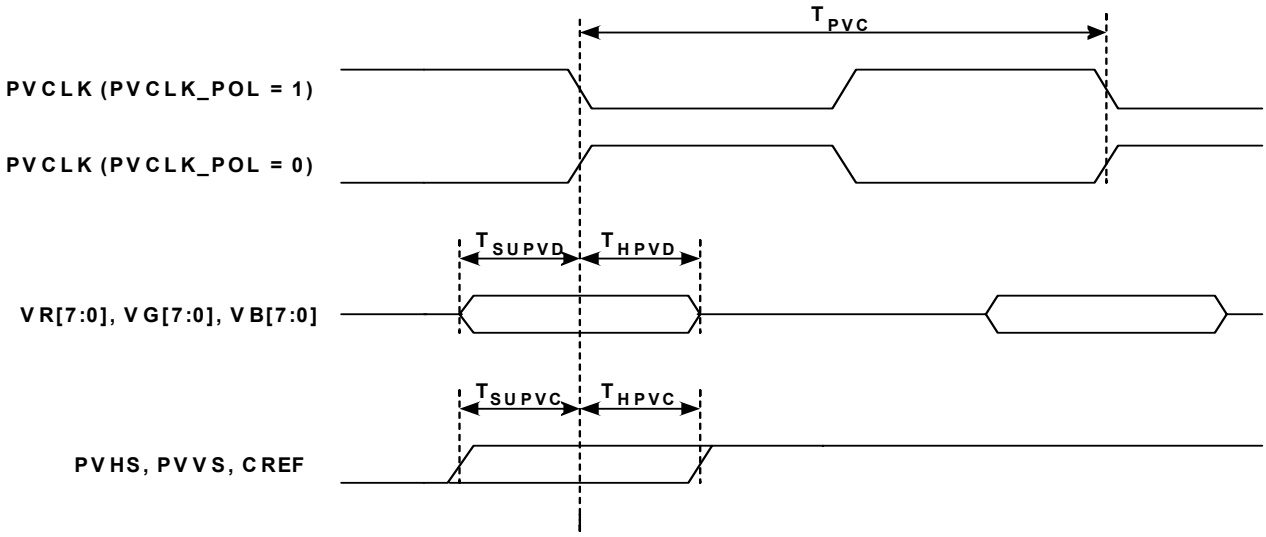


Figure 3-1 Primary Video (PV) Port Timing

Table 3-3 lists the electrical specifications for the Primary Video (PV) Port:

Table 3-3 Primary Video (PV) Port Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Units	Conditions
PVHS, PVVS Setup Time to PVCLK	T_{SUPVC}	5			ns	V_{33} = ± 5% C_L = 20 pF, V_{25} = ± 5%
VR[7:0], VG[7:0], VB[7:0] Setup Time to PVCLK	T_{SUPVD}	5			ns	V_{33} = ± 5% C_L = 20 pF, V_{25} = ± 5%
PVHS, PVVS Hold Time to PVCLK	T_{HPVC}	1			ns	V_{33} = ± 5% C_L = 20 pF, V_{25} = ± 5%
VR[7:0], VG[7:0], VB[7:0] Hold Time to PVCLK	T_{HPVD}	1			ns	V_{33} = ± 5% C_L = 20 pF, V_{25} = ± 5%
PVCLK Frequency	$1/T_{PVC}$	10	13.5	27	MHz	
PVCLK Duty Cycle		45		55	%	

3.4 Secondary Video (SV) Port AC Timing Characteristics

Figure 3-2 illustrates the AC timing characteristics for the Secondary Video (SV) Port on the SignalProcessor:

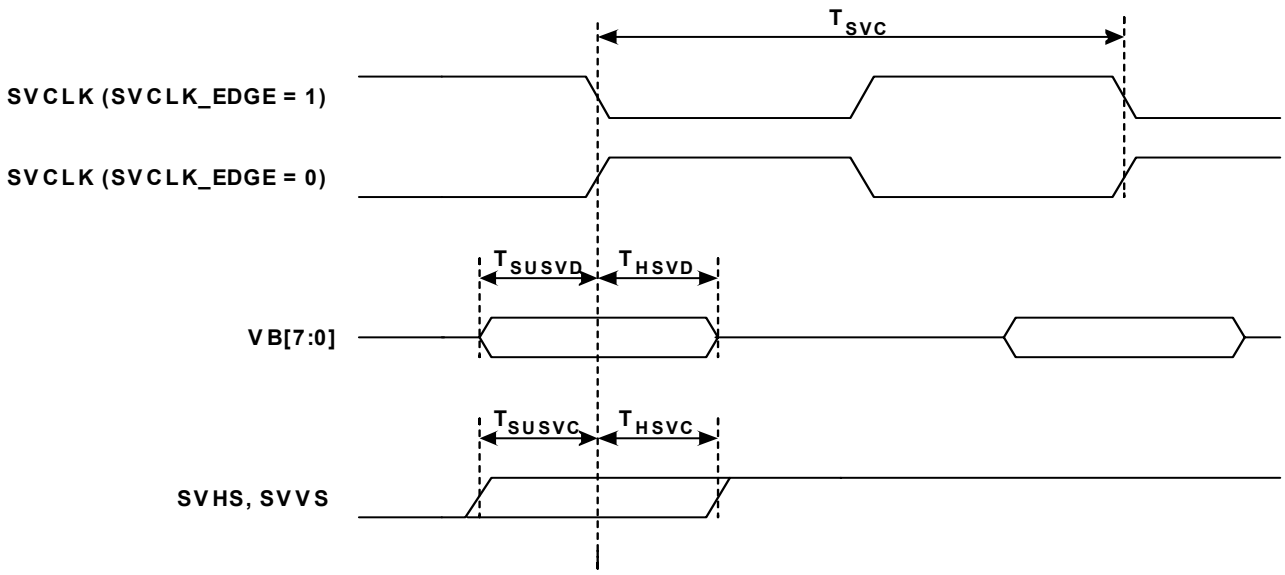


Figure 3-2 Secondary Video (SV) Port Timing

Table 3-4 lists the electrical specifications for the Secondary Video (SV) Port:

Table 3-4 Secondary Video (SV) Port Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Units	Conditions
SVHS, SVVS Setup Time to SVCLK	T_{SUSVC}	5			ns	V_{33} = ± 5% C_L = 20 pF, V_{25} = ± 5%
VB[7:0] Setup Time to SVCLK	T_{SUSVD}	5			ns	V_{33} = ± 5% C_L = 20 pF, V_{25} = ± 5%
SVHS, SVVS Hold Time to SVCLK	T_{HSVC}	2			ns	V_{33} = ± 5% C_L = 20 pF, V_{25} = ± 5%
VB[7:0] Hold Time to SVCLK	T_{HSVD}	2			ns	V_{33} = ± 5% C_L = 20 pF, V_{25} = ± 5%
SVCLK Frequency	$1/T_{SVC}$	10	27	54	MHz	
SVCLK Duty Cycle		45		55	%	

3.5 Memory Interface Input AC Timing Characteristics

Figure 3-3 illustrates the AC timing characteristics for the Memory Interface Input on the SignalProcessor:

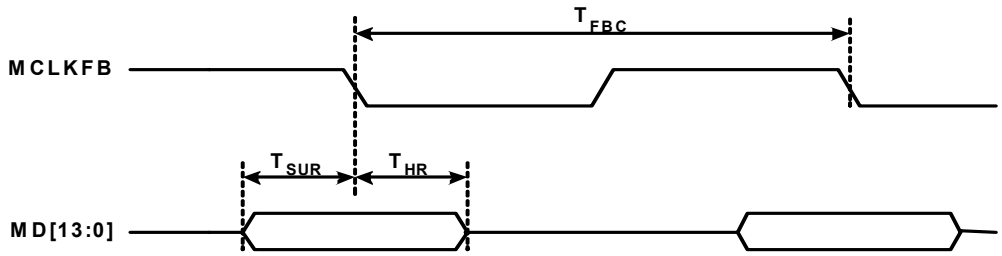


Figure 3-3 Memory Interface Input Timing

Table 3-5 lists the electrical specifications for the Memory Interface Input Port:

Table 3-5 Memory Interface Input Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Units	Conditions
MD[13:0] setup time to MCLKFB	T_{SUR}	2			ns	V_{33} = ± 5% C_L = 20 pF, V_{25} = ± 5%
MD[13:0] hold time to MCLKFB	T_{HR}	1			ns	V_{33} = ± 5% C_L = 20 pF, V_{25} = ± 5%

3.6 Memory Interface Output AC Timing Characteristics

Figure 3-4 illustrates the AC timing characteristics for the Memory Interface Output on the SignalProcessor:

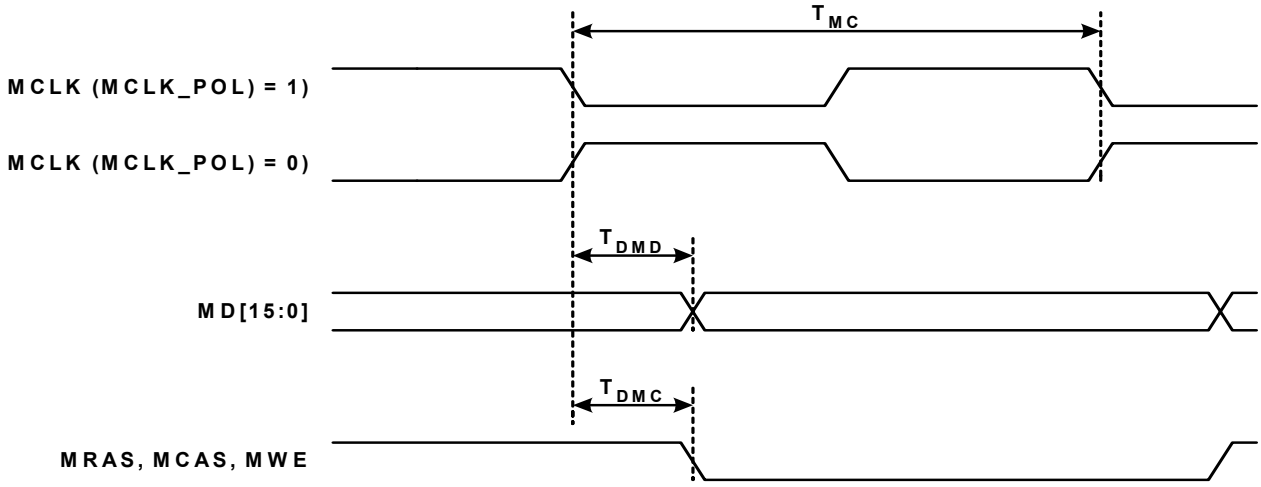


Figure 3-4 Memory Interface Output Timing

Table 3-6 lists the electrical specifications for the Memory Interface Output Port:

Table 3-6 Memory Interface Output Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Units	Conditions
MRAS, MCAS, MWE delay time from MCLK	T_{DMC}	0.8		6	ns	V_{33} = ± 5% C_L = 20 pF, V_{25} = ± 5%
MD[15:0] delay time from MCLK	T_{DMD}	0.8		6	ns	V_{33} = ± 5% C_L = 20 pF, V_{25} = ± 5%
MA[13:0] delay time from MCLK		N/A		N/A	ns	Address asserted and held one clock before/after RAS/CAS/WE assertion.
MCLK Frequency	$1/T_{MC}$	12		105	MHz	330ohm pull-up to V_{33}

4

Theory of Operations

This chapter provides the Theory of Operations for the PW1225 Video SignalProcessor.

4.1 Input Ports

Figure 4-1 shows the input ports for the PW1225 SignalProcessor.

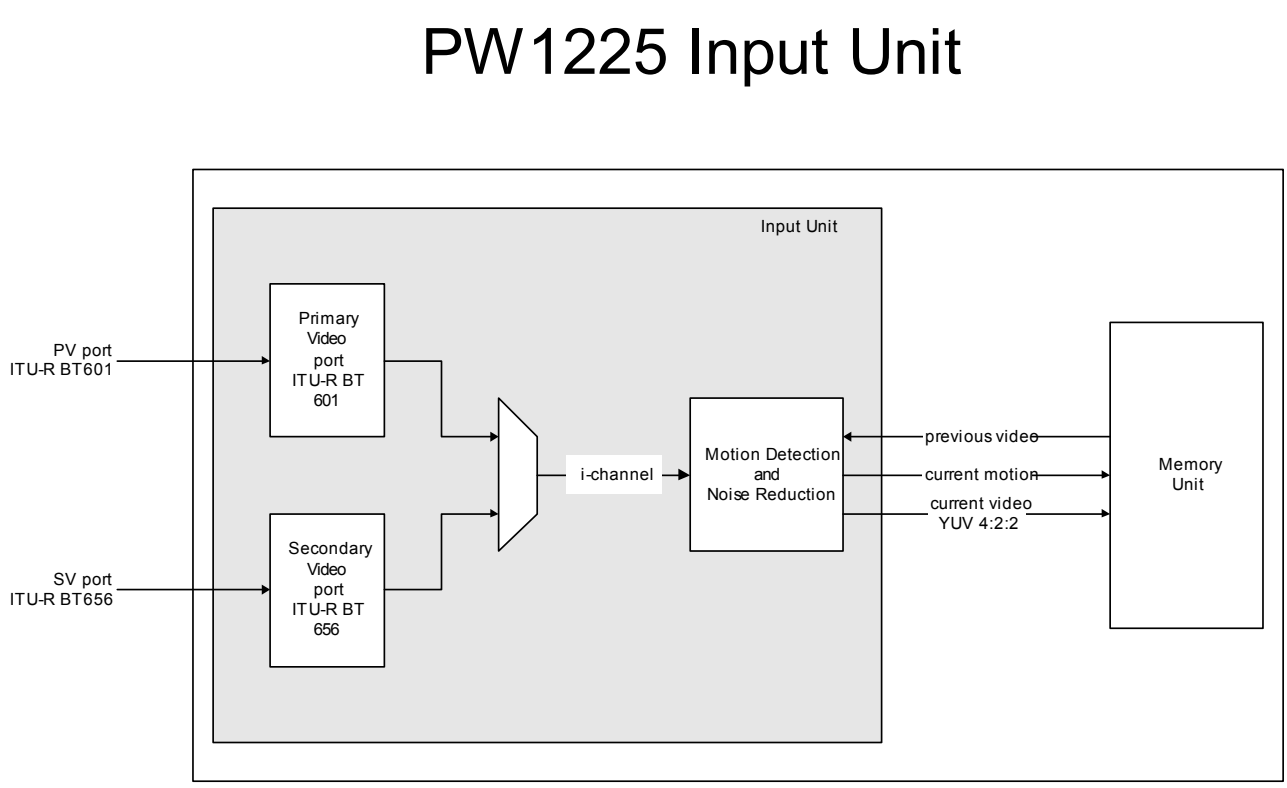


Figure 4-1 Input Ports

Both the Primary Video (PV) Port and Secondary Video (SV) Port are input interfaces for video data. The Primary Video (PV) Port accepts incoming data in the ITU-R BT601 (4:1:1, 4:2:2 and 4:4:4 YUV) formats. The Secondary Video (SV) Port accepts incoming data in the ITU-R BT656 (4:2:2 YUV) format.

The two video ports share a 24-bit video data bus and can be used to capture video inputs simultaneously. When both video ports are used, however, the Primary Video (PV) Port can accept incoming data only in the 4:1:1 or 4:2:2 YUV format.

4.1.1 Sync Decoder

The Sync Decoder determines whether the input format is programmed by an external CPU or automatically detected by the PW1225 SignalProcessor.

When DETECT_FORM = 1, the Sync Decoder is able to automatically detect the input format according to the total number of lines sampled between vertical syncs. The total includes both blanking and active lines. The Sync Decoder reports the detected input format in the INPUT_FORMAT field. The PW1225 accepts NTSC, and PAL video signals.

When the format is known, the framing of the input signal may begin. The framing parameters consist of width, height, vertical offset and horizontal offset. The vertical and horizontal offset refer to the vertical and horizontal blanking intervals and is specific to each input format. The resolution refers to the active region dimensions of the input video signal.

Table 4-1 shows the various default resolutions and offsets for NTSC and PAL.

Table 4-1 Default Resolutions and Offsets of the Active Screen Area

Video Format	cv_capw	cv_caph	cv_odd_capt	cv_even_capt	cv_capl
NTSC	720	240	16	16	122
PAL	720	288	22	22	132

The height of the even field is given in the case of interlaced modes; the height of the odd field is always assumed to be one line larger. The default vertical offset is identical for both the odd and even fields.

When DETECT_FORM = 0, the Sync Decoder is programmed with a specific resolution to capture video or graphics data, as shown in Figure 4-2. CAPL(8:0), CAPT(6:0), CAPW(7:0) and CAPH(7:0) registers define the active region of the incoming data. Data is ignored for the first CAPT(8:0) active lines, then ((CAPH(7:0)+1) x 2) lines are captured for the interlaced video input and ((CAPH(7:0)+1) x 4) lines are captured for the graphics input. For each line, CAPL(8:0) valid pixels are ignored before starting image capture, then ((CAPW(7:0) + 1) x 8) valid pixels are captured.

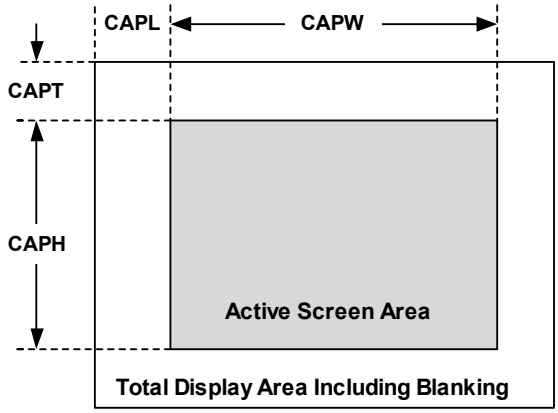


Figure 4-2 Image Capture Window

4.1.2 Secondary Video (SV) Port (ITU-R BT656 Mode 2, Slave Option)

The PW1225 accepts horizontal and vertical sync signals. A coincident low transition (within 30 clocks) of both SVHS and SVVS inputs indicates the start of an odd field. A SVVS low transition when SVHS is high indicates the start of an even field.

Figure 4-3 shows Timing Mode 2 for NTSC formats.

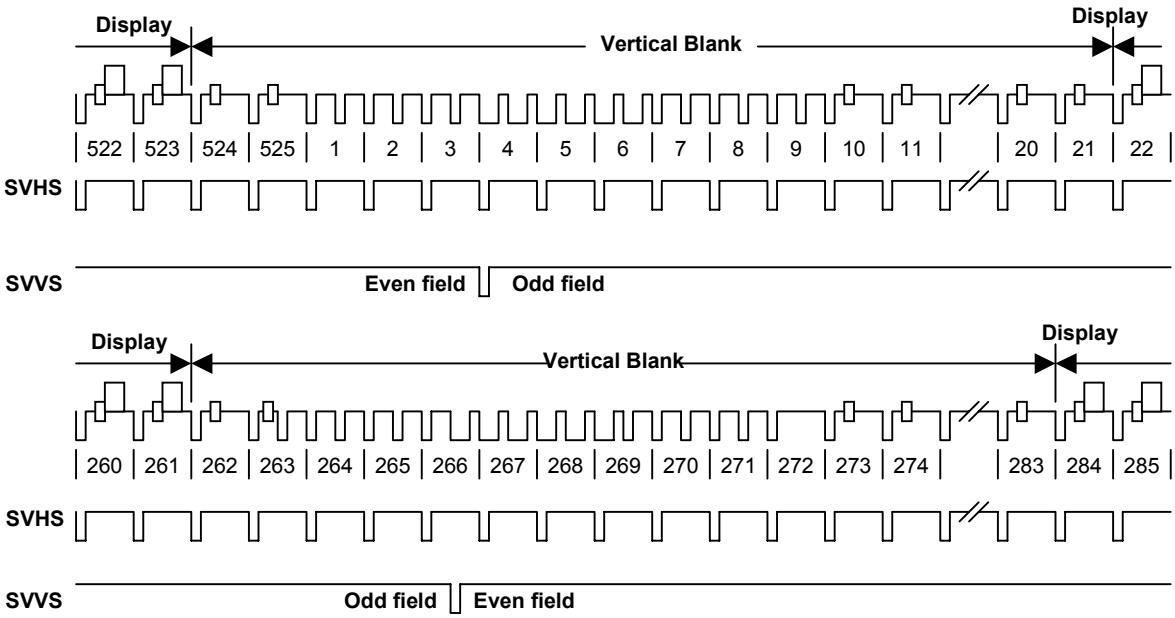


Figure 4-3 Timing Mode 2 (NTSC)

Figure 4-4 shows Timing Mode 2 for PAL formats.

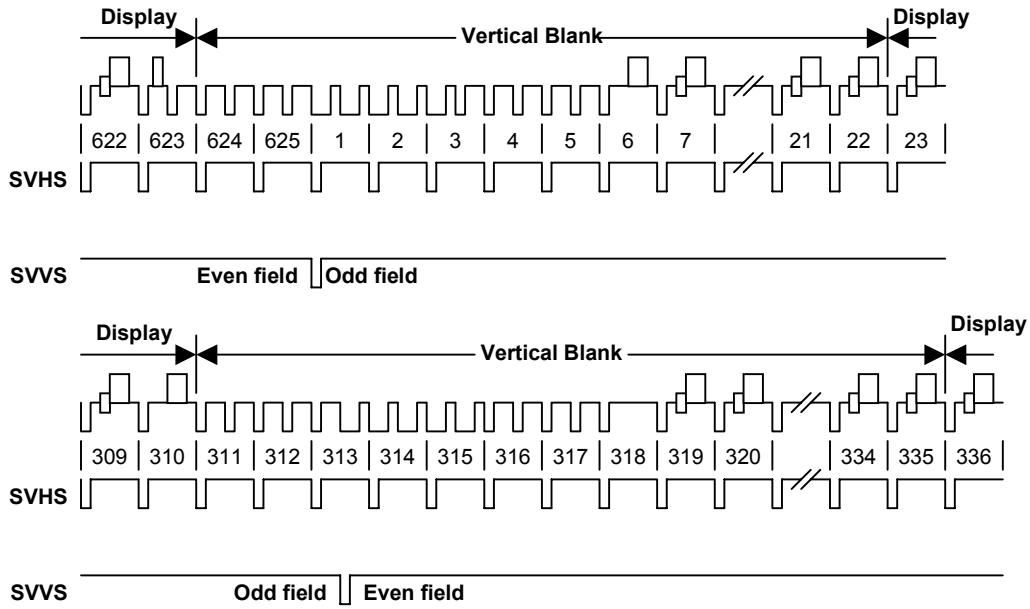


Figure 4-4 Timing Mode 2 (PAL)

4.1.3 Noise Reduction

Figure 4-5 shows a block diagram of the motion adaptive noise reduction.

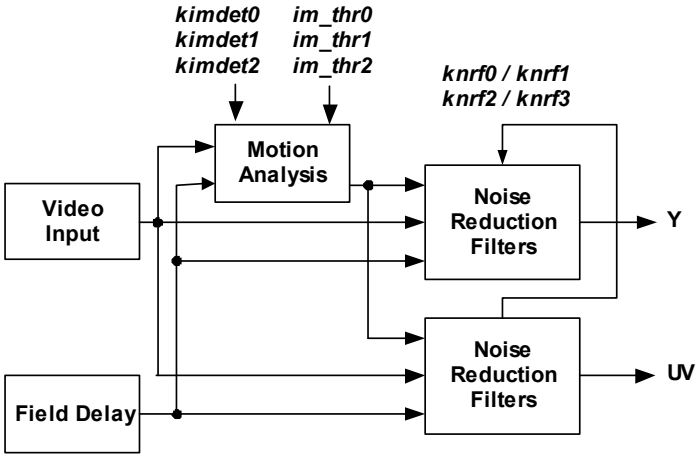


Figure 4-5 Motion Adaptive Noise Reduction Filters

The structure of the motion adaptive noise reduction is identical for the luminance signal and chrominance signals. The motion detector generates motion levels from input video data and field memory data. The input video data may be low-pass filtered with a FIR filter before being analyzed by the motion detector.

Table 4-2 defines the parameters of registers for the Noise Reduction Filters.

Table 4-2 Parameters for Noise Reduction Filter

Registers	Description	Value Range	Default Values
kimdet0, kimdet1, kimdet2	Parameters of the motion detection low-pass filter. Properties: [kimdet2, kimdet1, kimdet0, kimdet1, kimdet2] For example, setting kimdet2=0, kimdet1=0, and kimdet0=16 disables the low pass filter.	0…31	kimdet0 = 6 kimdet1 = 4 kimdet2 = 1
im_thr0, im_thr1, im_thr2	Set thresholds on the motion level. These registers divide the range of motion (from no motion to maximum motion) into four zones. Based on the level of motion present, one of four noise reduction filters is selected. Properties: $0 \le im\_thr0 < im\_thr1 < im\_thr2 \le 255$	0…255	im_thr0 = 3 im_thr1 = 6 im_thr2 = 10
knrf0, knrf1, knrf2, knrf3	Program parameters controlling these motion adaptive noise reduction filters. These parameters control the amount of noise filtering used in each motion zone. Properties: $0 \le knrf0 < knrf1 < knrf2 < knrf3 \le 128$	0…128	knrf0 = 64 knrf1 = 84 knrf2 = 104 knrf3 = 128

4.2 Memory Controller

The integrated memory controller takes care of addressing and control of the external SDRAM. The SDRAM should have LVTTL-compatible inputs and outputs.

The SDRAM types used with the PW1225 should be organized as 1Mx16, each bank having 4096 pages of 256 words of 16 bits. A typical configuration uses one 16Mb (1Mx16) or 64Mb (4Mx16) SDRAM with a 16-bit data bus, allowing for 2MB or 8MB of storage. Examples of SDRAMs that are supported include the Hyundai HY57V161610D (2MB), the Micron MT48LC4m16A2 or Hyundai HY57V641620HGT (8MB), or other compatible devices.

4.2.1 Frame Buffer Operations

The memory controller controls the flow of data between the PW1225 and either 2 or 8 MB of external 16-bit SDRAM. The essential function is to operate the SDRAM as a frame buffer between the input and display units.

Figure 4-6 shows the flow of the frame buffering operations.

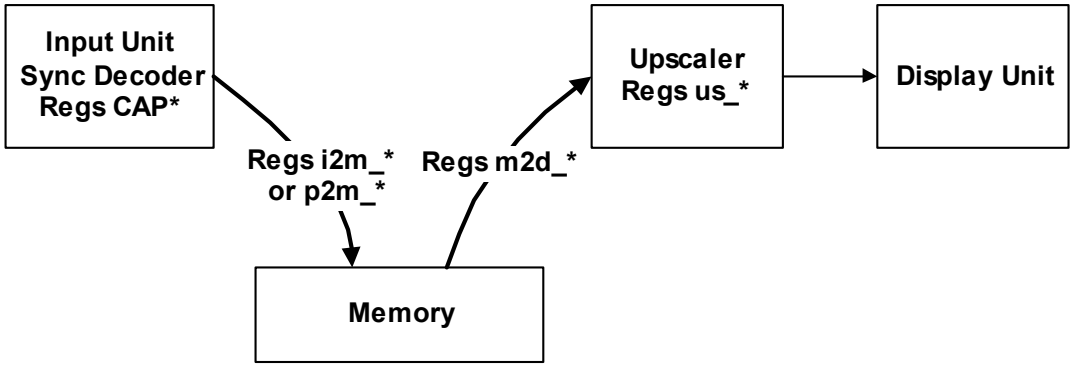


Figure 4-6 Frame Buffering

Data arrives at the frame buffer either in *video* or *motion* formats from the input unit or in raw form from the host interface via the two-wire bus. Interlaced data arrives as separate 16-bit 4:2:2 video and 4-bit motion components stored in different regions of the SDRAM. Similarly, data exits the memory unit either in video or motion formats to the display unit or in raw form to the host interface. The video data is also fed back to the input unit.

On the input side, the most recent four fields – two odd and two even – are stored in the frame buffer.

Freeze and *step* functions may be employed for the rejection of all or a fixed ratio of incoming fields. When in freeze mode, the entire frame buffer or a portion thereof may be *painted* a solid background color or, for diagnostics, a two-dimensional color bar pattern.

The active input region stored in the frame buffer is defined by the coordinates of its width *i2m_hlen* 0x40[6:0] and height *i2m_vlen* 0x41[7:0] and its top left corner *i2m_left* 0x44[6:0] and *i2m_top* 0x45[7:0]. When *i2m_siz* 0x40[7] = 0 and *i2m_offset* 0x44[7] = 0, there is no offset from the upper left origin and the size of the active input region follows Table 4-1.

On the output side, a set of line buffers is presented to the display unit from the merging of the most recently stored odd and even fields. The line buffers of 16-bit 4:2:2 video plus 4-bit motion are used. The merging of the odd and even fields can be either straight deinterlaced or inverse 3:2 or inverse 2:2 pulldown, depending on whether *film mode* has been detected.

The active display region is defined by the coordinates of its width *m2d_hlen* 0x5C[6:0] and height *m2d_vlen* 0x5D[7:0] and its top left corner *m2d_left* 0x58[6:0] and *m2d_top* 0x59[7:0]. When *m2d_siz* 0x5C[7] = 0 and *m2d_offset* 0x58[7] = 0, there is no offset from the upper left origin and the size of the active display region follows Table 4-1.

4.2.2 SDRAM Interface

The data output from the SDRAM may be clocked into the PW1225 using the external MCLKFB.

Figure 4-7 shows a block diagram of the SDRAM interface.

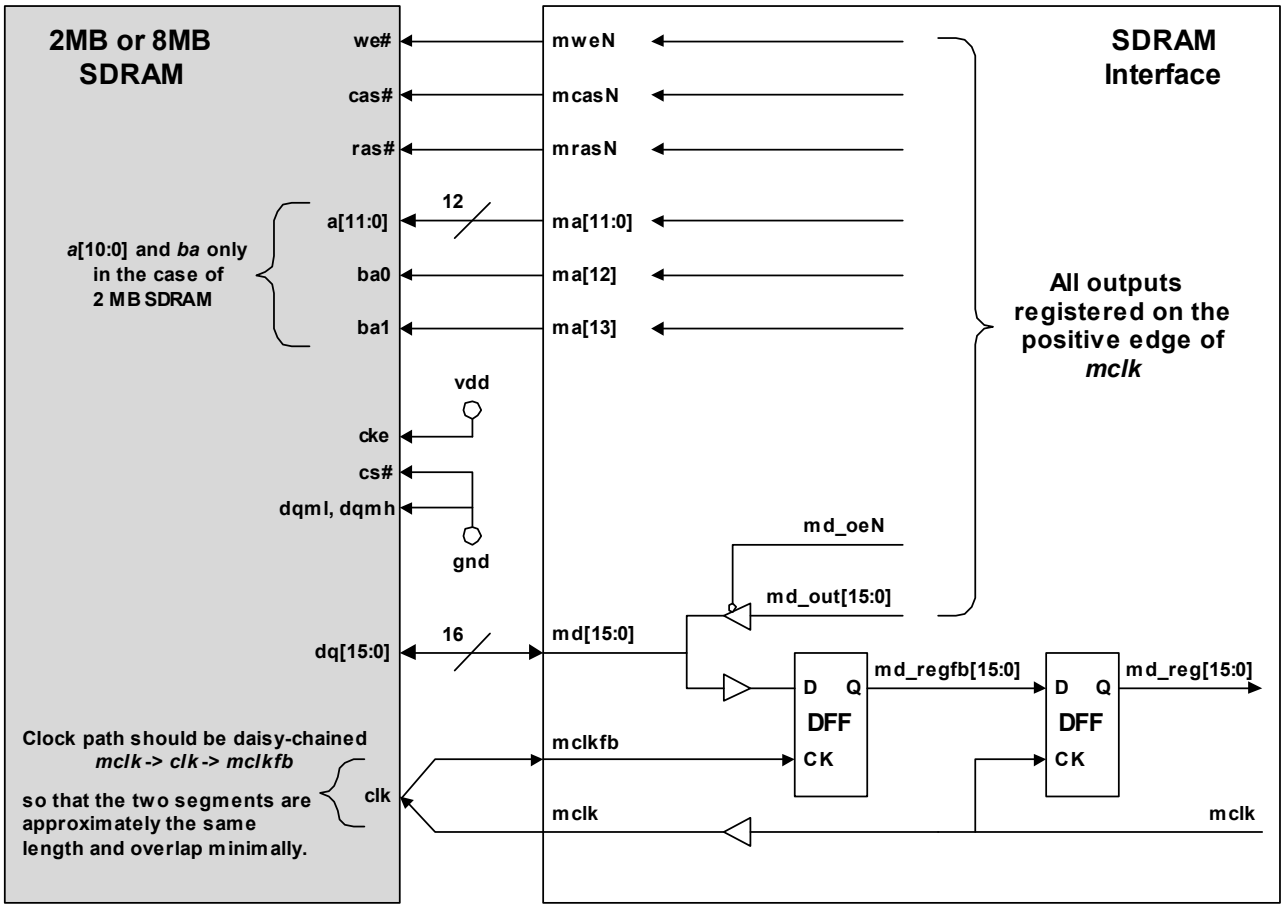


Figure 4-7 SDRAM Interface Block Diagram

All outputs from the SDRAM interface are registered on the positive edge of *mclk*. The clock path should be connected in this order:

mclk-> clk -> mclkfb

This ensures that the two segments are approximately the same length and overlap minimally. In the case of 2MB SDRAM, only memory address bus *ma*[10:0] and *ma*[12] bits are used to interface with the SDRAM address inputs a[10:0] and bank address input ba. For the 8MB SDRAM usage, *ma*[11:0] should be connected to *a*[11:0]; *ma*[12] and ma[13] should be tied to ba0 and ba1, respectively.

4.2.3 Memory Refresh

Typically an SDRAM part requires refreshing at an average interval of every 15.625 µs. In general, it is good to set the refresh interval *ref_len* 0x57[1:0] to as large a number as possible to optimize bandwidth. However, a certain maximum setting is required depending on the speed of the memory clock *mclk*. Table 4-3 lists the optimal (maximum) setting. The minimum *mclk* frequency supported is 10 MHz.

Table 4-3 Maximum Refresh Interval Settings

Frequency Range *mclk*	Maximum Refresh Interval *ref_len*
10 – 50 MHz	0
51 – 80 MHz	1
81 – 110 MHz	2
> 110 MHz	3

4.3 Deinterlace Processor

The Deinterlace Processor automatically determines the type of incoming video content – film, static interlaced video and moving interlaced video. Different algorithms are applied for each of the content types.

The PW1225 incorporates a per-pixel, motion compensated architecture to produce artifact-free progressive scan video signals. Video content is analyzed on a single pixel granularity to detect presence or absence of noise and compute the amount of motion. When DI_BYPASS = 0, the motion video is processed using a highly intelligent algorithm that *simultaneously* eliminates noise and interpolates pixels along any angle to produce a noise-free picture without jagged-edge artifacts.

4.3.1 Film Mode

The Deinterlace Processor detects film-originated content by analyzing consecutive images and detecting a 3:2 or 2:2 pull down pattern. Film-originated content is deinterlaced by merging the two fields from the original frame. Either 32pd_film_mode or 22pd_film_mode bit is normally set to 1 to enable automatic film mode detection.

- In the NTSC mode, the PW1225 detects 3:2 pull-down sequences and merges the fields into 60Hz progressive frames.
- In the PAL mode, the Deinterlace Processor detects 2:2 pull-down sequences and rearranges the fields into 50Hz progressive frames.

A block diagram of Film Mode is shown in Figure 4-8.

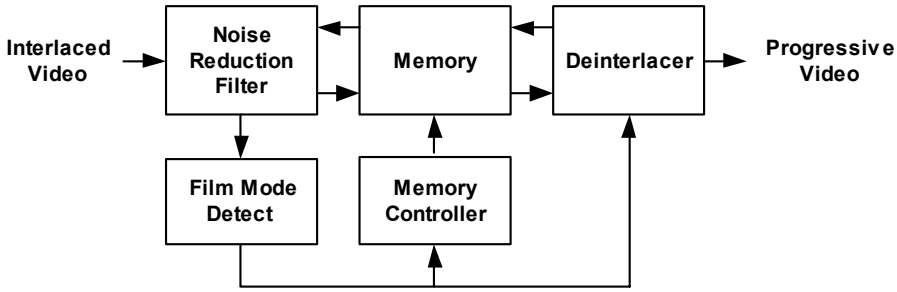


Figure 4-8 Film Mode Block Diagram

The Film Mode Detect module detects film originated content sequences by examining the interlaced video inputs. The Memory Controller receives appropriate command to map the fields to support 60Hz progressive video in Memory, prior to deinterlacing. If no film-originated content is detected, the video stream is stored in Memory without further processing. 32pd_film_sens(1:0) and 22pd_film_sens(1:0) registers define the number of fields the PW1225PW1231 requires to detect film-originated content and enter film mode.

The sequence is continuously monitored and any break in the sequence caused by “bad cuts” is quickly spotted and compensated for if bad cut processing is enabled (register 0x33). Bad Cut can occur in three scenarios:

- TV commercials sandwiched between film materials In this case, the source materials jump in and out of the film mode very abruptly.
- Movie preview in a DVD title. In this case, the movie preview usually consists of many improperly formatted 3:2 film materials.
- Shot on film, transferred to video, and edited on video.

4.4 Video Scalers

Figure 4-10 shows the Video Up Scaler. The upscaler remaps an incoming *m*-column by *n*-row frame into an outgoing *p* by *q* frame.

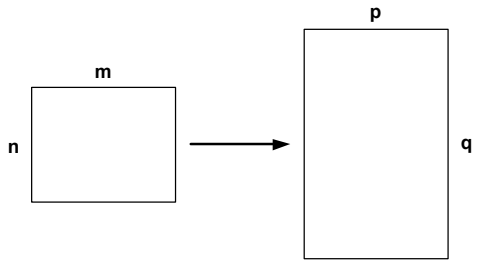


Figure 4-9 nm Frame to pq Frame

The incoming horizontal length *m* is determined according to *m2d_siz* 0x5C[7] and *m2d_hlen* 0x5C[6:0] fields. Similarly, the upscaler determines the incoming vertical length n is by examining the *m2d_siz* and *m2d_vlen* 0x5D[7:0] fields.

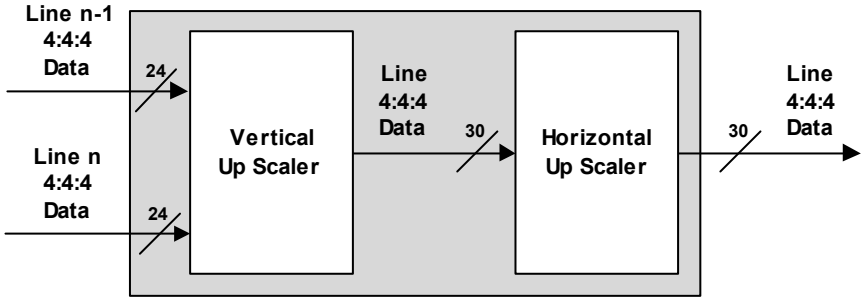


Figure 4-10 Video Up Scaler

The outgoing horizontal and vertical lengths, p and q, are also programmable. Table 4-4 shows the default output resolutions, which can be programmed by setting *us_remap* 0x71[0] to 1 and selecting the output resolutions using *us_mode* 0x71[3:1]. Alternatively, the upscaler can resize the picture to any arbitrary size *(us_hlen* by *us_vlen)* when *us_size* is set to 1. The upscaler can be turned off by setting *us_size* and *us_remap* to 0.

Table 4-4 Default Output Resolutions by Display Mode

us_mode	Format	Width (*hlen*)	Height (*vlen*)
0	NTSC/480i/480p	720	480
1	PAL	720	576

4.4.1 Vertical Scaler

The vertical scaler scales data provided by the deinterlacer. Vertical scaling allows a downscale ratio of up to 2 to 1. The upscale ratio is limited by the resolution of the control registers.

4.4.2 Horizontal Scaler

The horizontal scaler takes 1 line of data provided by the vertical scaler and outputs 1 line. The horizontal scaler only supports upscaling. The upscale ration is limited by the resolution of the control registers.

4.5 Video Enhancer

The Video Enhancer block contains these key functions: Luminance Peaking, DLTI, DCTI, Brightness and Contrast, Hue and Saturation, and Black Level Expansion. Figure 4-11 illustrates the Video Enhancer.

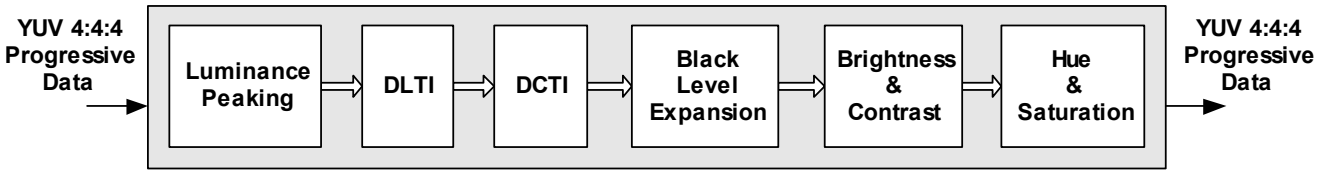


Figure 4-11 Video Enhancer

Coring is a noise reduction technique used in may areas of the PW1225. If a signal is less than a certain threshold value, it is assumed to be noise and is set to zero.

Figure 4-12 shows an example of output with and without coring.

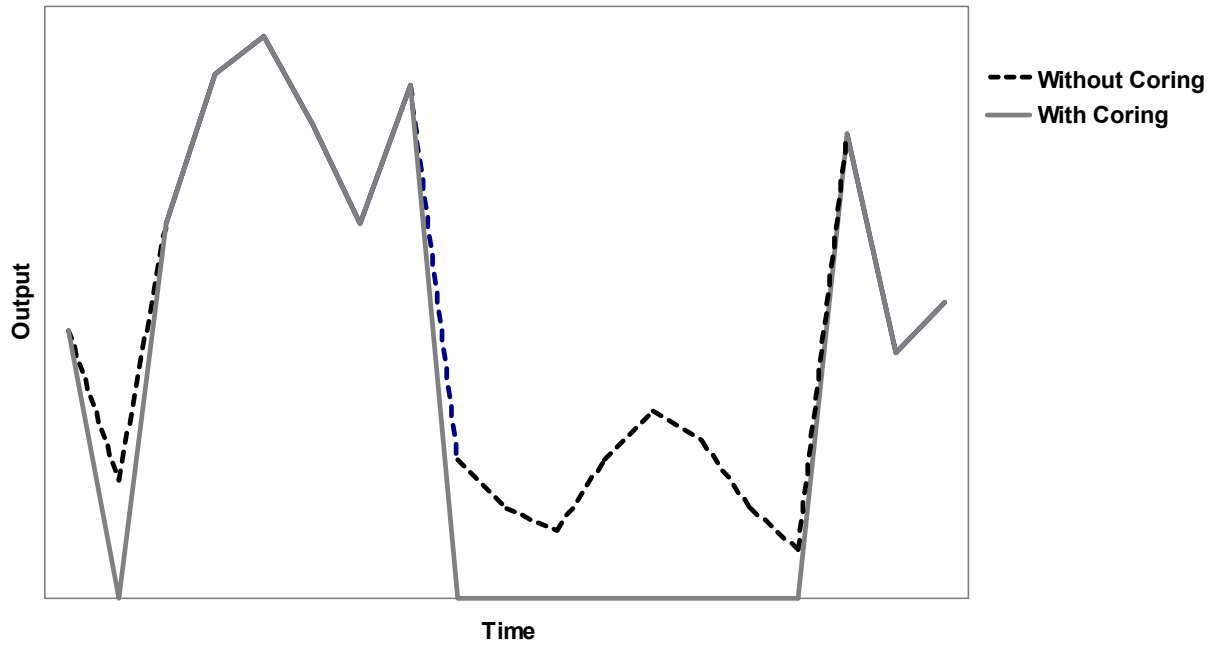


Figure 4-12 Coring Example

4.5.1 Luminance Peaking Filter

The Luminance Peaking Filter improves the overall frequency response of the luminance by increasing the peak-to-peak signal thus creating blacker blacks and whiter whites. There are three filters applied to the luminance:

- High-pass filter
- Band-pass filter
- Low-pass filter

The outputs of these filters are weighted by gain factors and summed together. The gain factors are programmable through registers *khpw* 0xD0[4:0], *kbpw* 0xD1[4:0] and *klp* 0xD2[2:0]. Coring is used to remove low amplitudes in the (high-pass + band-pass) signal, which are considered to be noise. Coring levels can be programmed via the *peak_coring* 0xD3 register.

4.5.2 DLTI & DCTI

The Digital Luminance Transient Improvement (DLTI) and Digital Color Transient Improvement (DCTI) are intended to enhance video by replacing the edges of the video with edges that have steeper rise and fall times. DLTI and DCTI are different from peaking in that they do not increase the peak-to-peak video at its output; rather it turns

sloped or sinusoidal waveforms into rectangular or square waveforms with the same duty cycles and peak-to-peak amplitude. DCTI is especially useful for 4:1:1 video sources.

The PW1225 can perform coring in conjunction with DCTI and DLTI, in which it forces all values below a programmed threshold level to be 0. This is useful to enhance immunity against nose. Via the configuration registers (0xD4 and 0xD5) it is possible to control: DLTI gain width, DLTI coring threshold, DCTI gain width, DCTI coring threshold, and selection of simple, or improved first differentiating DCTI filter.

4.5.3 Black Level Expansion

Black level expansion (BLE) enhances the contrast of the picture. The dark regions of the picture are made darker, while bright areas remain unchanged. The advantage of this black-level expansion is that the black expansion is performed only if it will be noticeable to the viewer.

Figure 4-13 shows an example of the BLE transfer function.

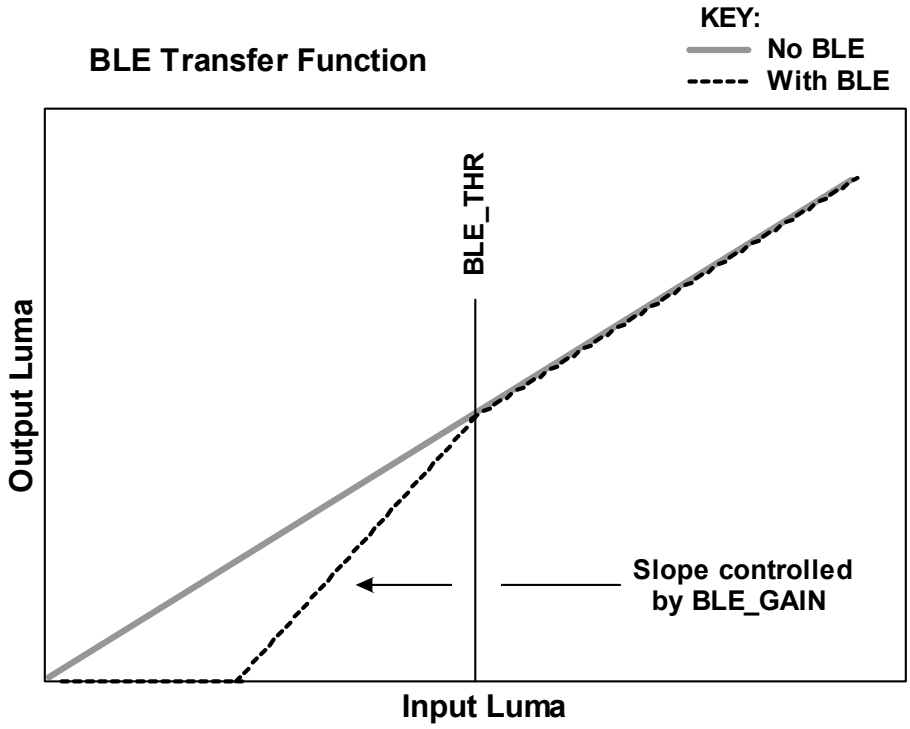


Figure 4-13 BLE Transfer Function Example

4.5.4 Brightness and Contrast

Programmable brightness and contrast are used to adjust the offset and gain of the video signal. Contrast is adjusted by multiplying the luminance (after sync and blank information have been removed) by a constant, *contrast* 0xD6[5:0]. The video enhancement module can also adjust brightness by adding or subtracting a constant, *brightness* 0xD7[7:0], from the luminance value. The brightness adjustment is done after the contrast adjustment to avoid introducing a varying DC offset due to adjusting the contrast.

4.5.5 Hue and Saturation

Hue refers to the wavelength of the color and is used to describe base color- red, green, yellow, etc. Saturation is the amount of color present. For example, a lightly saturated red looks pink. The hue and saturation algorithm uses the *hue* 0xD8[7:0] and *saturation* 0xD9[7:0] fields.

4.6 Video Overlay

Video Overlay adjusts video into the proper color space with required blanking for the active region; blue screen adjustment is optional. Figure 4-14 illustrates Video Overlay for the PW1225:

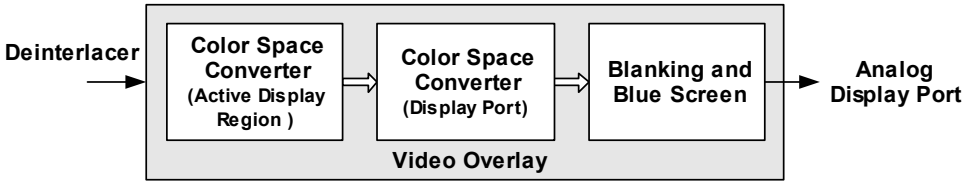


Figure 4-14 Video Overlay

4.6.1 Color Space Converters

The PW1225 has two Color Space Converters. The first converter is located in front of the video select block and performs color space conversion on the active display region. The converter ensures that both video channels share a common color space before the video select. The second converter is located behind the video select block and converts the video select output to the display color space.

Table 4-5 lists the settings for the Active Display Region Color Space Converter.

Table 4-5 Active Display Region Color Space Converter

prim_cs	Input	Output
00	ITU-R BT601YPbPr	ITU-R BT601YPbPr
01	ITU-R BT709 YPbPr	
10	PC RGB (0 ... 255 range)	
11	TV RGB (16 ... 235 range)	

Table 4-6 lists the settings for the Display Port Color Space Converter.

Table 4-6 Display Port Color Space Converter

common_cs	Input	Output
000	ITU-R BT601YPbPr	ITU-R BT601YPbPr
001		YPbPr
010		ITU-R BT709 YPbPr
100		PC RGB (0 ... 255 range)
101		TV RGB (16 ... 235 range)

4.6.2 Blanking

Blanking sets YPbPr or RGB to fixed values during vertical and horizontal blanking. The blank value for Y can be selected to be either 0 or 64 using the *y_blank* 0x79[6] field. U and V are fixed to 512 in either case. In the case of RGB, blanking switches all three signals to 0. There is no bypass of the blanking algorithm.

4.6.3 Blue Screen

Blue screen sets active YUV or RGB to programmable values when the *blue_screen* 0x78[6] bit = 1. Configuration registers *blue_screen*, *y_blue* (0x79), *u_blue* (0x7A), and *v_blue* (0x7B) are used to specify the values according to the following. The blue screen algorithm is turned off when *blue_screen* = 0.

$$Y' = \{y\_blue, y\_blue[7:6]\}$$

U’ = {*u_blue, u_blue[7:6]}*

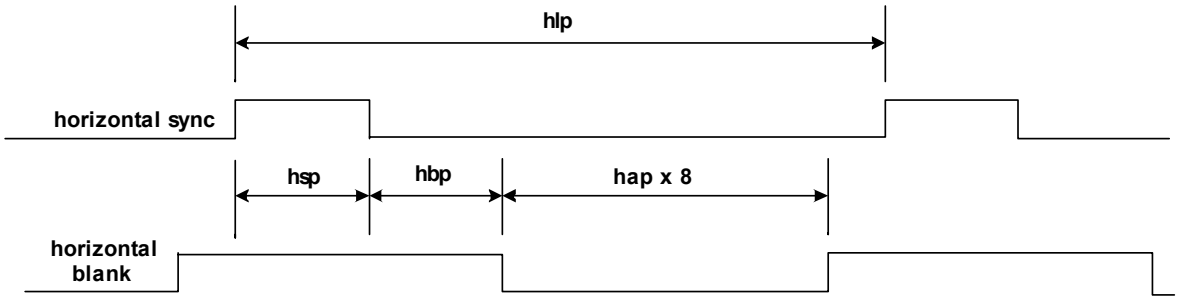
V’ ={*v_blue, v_blue[7:6]}*

4.7 Display Timing Generator

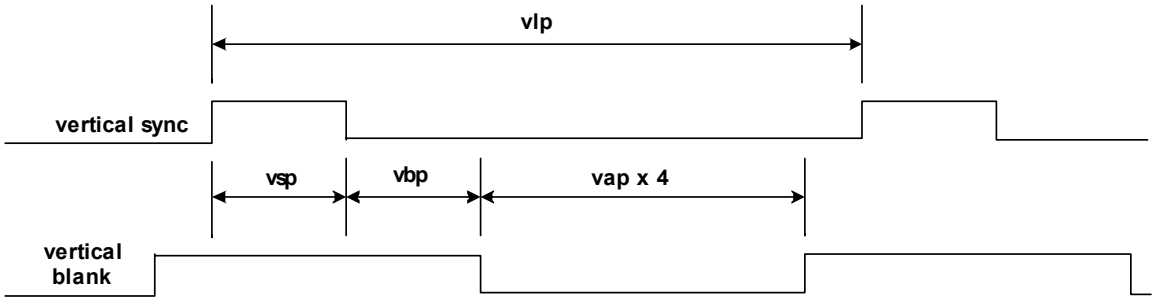
The display timing generator creates the vertical and horizontal timing signals for the display device. When dsp_sync = 0 (0x60[1]) 480p timing is generated for NTSC input data, and 576p is generated for PAL data. When dsp_sync = 1 (0x60[1]) timing is generated based on the registers 0x60 – 0x6f. When dsp_sync = 0 (0x60[1]) progressive timing is generated. When dsp_sync = 1 (0x60[1]) interlaced timing is generated.

The relationship of the register values to the timing generated is shown in Figure 4-15:

Horizontal Timing



Vertical Timing (Progressive)



Vertical Timing (Interlaced)

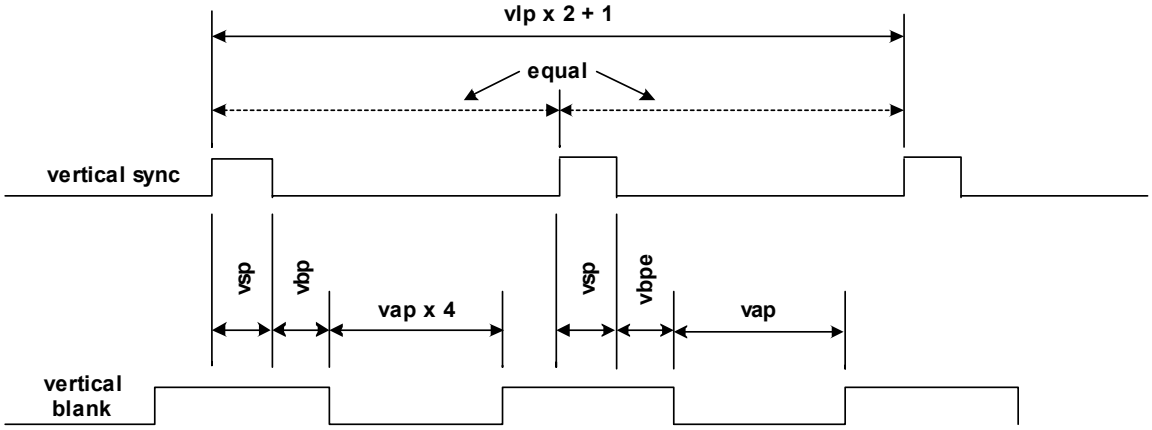


Figure 4-15 DSP Timing

4.8 Analog Display Port

The Analog Display Port generates analog RGB, YUV or YPbPr with triple 10-bit digital-to-analog converters (DACs). The analog RGB or YUV output is generated in synchronization with timing signals.

Conversion from digital to analog is separate for Y, U and V. Each converter uses an external resistor of approximately 75 ohms, connected between output and ground, to interface with low impedance output buffers.

Each digital-to-analog converter has its own supply and ground pins which are used for decoupling. An internal reference voltage of 1.23V is generated for each DAC. A compensation capacitor is connected to the COMP pin. A resistor is connected to the RSET pin to set the magnitude of the full-scale DAC output.

4.8.1 Copy Protection

The anticopy process is implemented according to the Macrovision version 7.1L1 specification developed by Macrovision Corporation, Sunnyvale, California. All luminance and chrominance signals include the Macrovision Anticopy Process. The PW1225 incorporates an anticopy process technology that is protected by U.S. patents and other intellectual property rights.

The anticopy process is licensed for noncommercial, home use only. Reverse engineering or disassembly is prohibited. Pixelworks can only ship PW1225 to customers licensed by Macrovision. A PW1225 Macrovision supplement may be obtained, by Macrovision licensees, by contacting Pixelworks Corporation.

The component video interface with Macrovision (CVIM) is designed to meet standards of EIA-770.2-A and Specification of the Macrovision AGC copy protection waveforms for DVD applications with 525p (480p) progressive outputs. The copy protection module also supports placing the CGMS (Copy Generation Management System) into the Y channel of the output data stream.

The copy protection module accepts progressive scan video inputs and generates outputs to meet the EIA-770.2 standard. The inputs are 30-bit YPbPr 4:4:4 data, Vsync, and Hsync. The output format is progressive scan 30-bit YPbPr 4:4:4 data with the embedded sync. Copy protection is supported only for the 480p display format using a 27 MHz pixel clock.

Copy protection is enabled by external pins and register bits. Both the external pin and the register must be in the enabled state to engage the copy protection feature. Pin 74 and register bits 0xE0[0] are for CGMS; Pin 81 and register bits 0xEA[1:0] are for Macrovision.

4.8.2 Sync Signal Insertion

The sync signal is inserted into the digital video signal (Y channel) prior to digital to analog conversion allowing ease of use. Prior to the sync insertion, the active video data is shifted from 0 to Blanking Level (306). The mapped video data will then swing between the Y Blanking Level and 1023, while the range from 0 to Blanking will be used for sync insertion only. The sync insertion conforms to the timing requirement of EIA-770-2A. Figure 4-17 shows the insertion of the sync signal. The video data mapping uses the following gain control formula.

Multiplier = (Output Max - Output Blank)/Input Max.

Adder = Output Blank

Sync signal insertion is only supported for the 480p display format using a 27MHz pixel clock.

4.8.3 CGMS

The PW1225 places the CGMS (Copy Generation Management System) into the Y channel of the output data stream. The CGMS generator is programmable and supports different standards. Both the American Standard EIA-805 and the Japanese Standard EIAJ CPR-1204 are supported.

CGMS is only supported for the 480p display format using a 27MHz pixel clock.

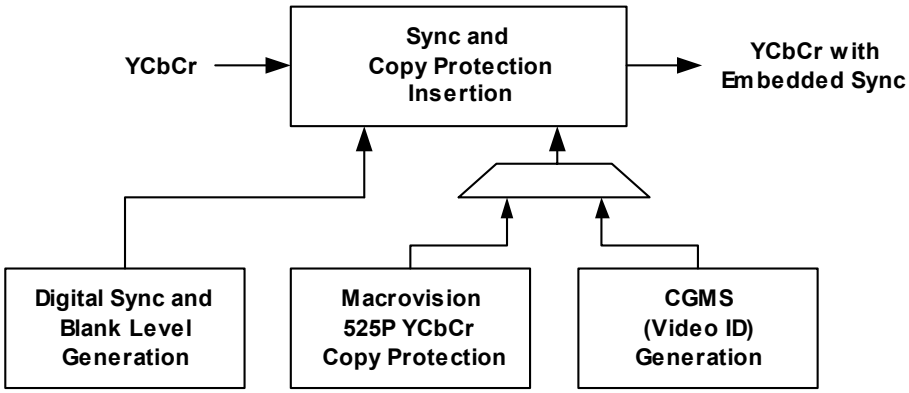


Figure 4-16 Copy Protection Block Diagram

Figure 4-17 illustrates mapping and sync insertion.

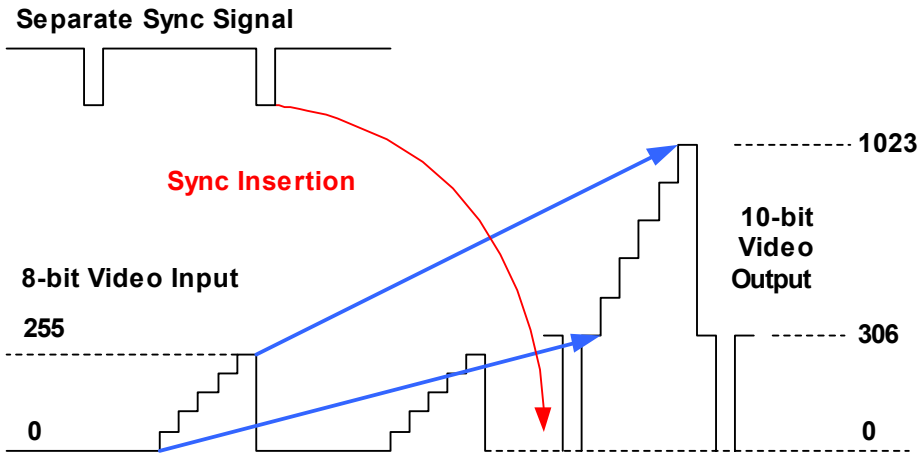


Figure 4-17 Mapping and Sync Insertion

4.9 2-Wire Serial Bus Description

The host interface provides programmable control capability to allow adjustment, calibration, and intelligent control of each subsystem. The PW1225 provides this capability via the 2-wire serial bus. The 2-wire serial bus is a bi-directional, two-wire serial bus, consisting of a serial data line (SDA) and a serial clock line (SCL). The 2-wire serial bus interface is used in slave receive and transmit mode for communication with a system microprocessor. The standardized bus frequencies of both 100 kHz and 400 kHz are supported. The 400 kHz (Fast Mode) requires 50ns glitch filters for both positive and negative glitches.

4.9.1 2-Wire Serial Bus Protocol

Four device addresses (0x60, 0x64, 0x68 and 0x6C) are reserved for accessing the PW1225 via the 2-wire serial bus. The least significant bit of the device addresses is fixed to zero. The next two least significant bits are configurable and can be defined by the level tied at their input pins 2WA1 and 2WA2.

The 2-wire Serial Bus protocol is shown in Figure 4-18. All communications are initiated with a start condition (S) from the 2-wire bus master, which is followed by the desired device address and read/write bit.

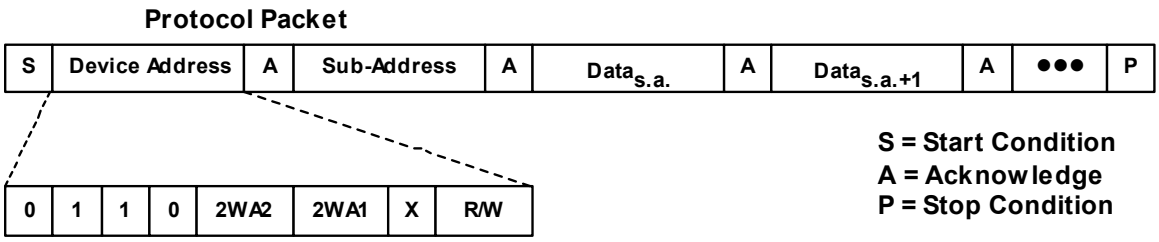


Figure 4-18 2-Wire Serial Bus Device Address

Figure 4-19 illustrates the 2-wire serial bus WRITE mode.

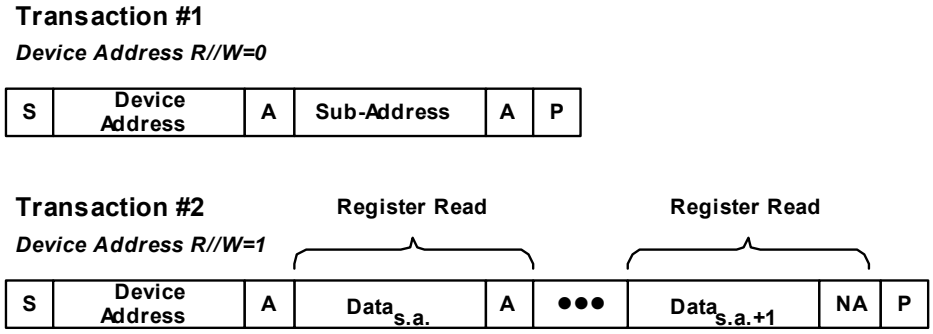


Figure 4-19 2-Wire Serial Bus WRITE Mode

In the WRITE mode (indicated by setting the read/write bit LOW), one sub-address follows the device address acknowledgement. After the sub-address, a series of data bytes may follow. After the last data byte has been acknowledged, the 2-wire serial bus master issues a stop condition (P).

Figure 4-20 illustrates the 2-wire serial bus READ mode.

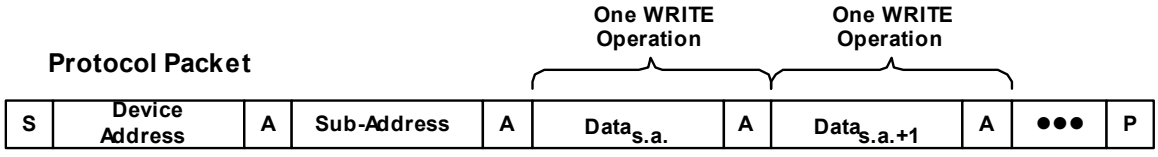


Figure 4-20 2-Wire Serial Bus READ Mode

In the READ mode (indicated by setting the read/write bit LOW), two transactions are required on the 2-wire serial control bus. The first transaction resembles a write operation with no data transfer. This step will write the desired sub-address into the internal address pointer. The next transaction reads one or more bytes from the PW1225 starting from the sub-address set in the first transaction. The first byte of this transaction is the IC address with the read bit set. The second and subsequent bytes, if any, are read data from the PW1225. The last byte is signaled by the 2-wire control master when it returns a “not acknowledge” for a data byte transmitted by the PW1225.

5

Register Maps

This chapter describes the Register Maps for the PW1225 Video SignalProcessor. The sections for each register block in this chapter include two tables. The first lists the registers with bit names, and the second provides detailed bit descriptions.

5.1 Register Map Overview

The sub-address assignment for each subsystem is listed in Table 5-1. The last column in this table provides a link to the sections in this chapter for each register block.

Note
All unlisted sub-addresses are Reserved.

Table 5-1 PW1225 Register Block Address Map

Block Name		Byte Offset	Link to Register Definition Table
Clock Generator and Programming Unit		0x10 — 0x17	Table 5-3, on page 5-3
Input Unit		0x18 — 0x3F	
	PV Interface	0x17 — 0x1F	Table 5-5, on page 5-5
	SV Interface	0x18 — 0x3F	Table 5-7, on page 5-9
	Input Channel	0x30 — 0x33	Table 5-9, on page 5-13
Input to Memory		0x40 — 0x43	Table 5-11, on page 5-15
Memory Unit		0x44 — 0x5B	
	Input FIFO Unit	0x44 — 0x47	Table 5-13, on page 5-16
	Memory Controller	0x4C — 0x57	Table 5-15, on page 5-17
	Display FIFO	0x58 — 0x59	Table 5-17, on page 5-19
Memory to Display		0x5C — 0x5D	Table 5-21, on page 5-21
Display Unit		0x60 — 0x7F	
	Display Timing	0x60 — 0x6C	Table 5-23, on page 5-22
	Deinterlace Control	0x70	Table 5-25, on page 5-24
	Upscaling	0x71 — 0x73	Table 5-27, on page 5-25
	Video Overlay	0x78 — 0x7B	Table 5-29, on page 5-26
Additional Programming Unit		0x90 — 0x9F	
	Scan Velocity Modulation (SVM)	0x80 — 0x83	Table 5-31, on page 5-27

Table 5-1 PW1225 Register Block Address Map (continued)

Block Name		Byte Offset	Link to Register Definition Table
	2:2 Pull-Down (22pd) Control	0x87	Table 5-33, on page 5-28
	2:2 Pull-Down (22pd) Global Motion Detection	0x88 — 0x8F	Table 5-35, on page 5-29
	Two-Wire Slave	0x90 — 0x93	Table 5-37, on page 5-30
	Direct SDRAM Access	0x94 — 0x97	Table 5-39, on page 5-31
Additional Display Unit		0xD0 — 0xEF	
	Video Enhance	0xD0 — 0xDF	Table 5-41, on page 5-32
	CMGS	0xE0 — 0xEA	Table 5-43, on page 5-34

5.2 Control Register Definitions

The following sections describe the function of the registers used for control and status.

Note
Unless otherwise stated in the bit description, all registers bits are reset to zero by the RESET input pin.

The following abbreviations are used in the Register Type column of the register tables.

- r = Read Only
- rw = Read/Write

5.3 Clock Generator and Programming Unit

Table 5-2 lists the Clock Generator and Programming Unit Registers.

Table 5-2 Clock Generator and Programming Unit Register Map

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x10	rw	mpll_bp	dpll_bp	0	0	dpll_source	dpll_source	dpll_von	mpll_von
0x11	rw	mpll_nf7	mpll_nf6	mpll_nf5	mpll_nf4	mpll_nf3	mpll_nf2	mpll_nf1	mpll_nf0
0x12	rw	mpll_nf8	mpll_od1	mpll_od0	mpll_r4	mpll_r3	mpll_r2	mpll_r1	mpll_r0
0x13	rw	mpll_pd	mpll_oe	dpll_pd	dpll_oe	0	0	mclk_bypass	dclk_bypass
0x14	rw	0	0	0	0	0	0	0	buffer_2W_wr
0x15	rw	dpll_nf7	dpll_nf6	dpll_nf6	dpll_nf4	dpll_nf3	dpll_nf2	dpll_nf1	dpll_nf0
0x16	rw	dpll_nf8	dpll_od1	dpll_od0	dpll_r4	dpll_r3	dpll_r2	dpll_r1	dpll_r0

Table 5-3 provides detailed descriptions of the Clock Generator and Programming Unit Registers.

Table 5-3 Clock Generator and Programming Unit Registers

<table>
<tr><th>Sub Address</th><th>Bits</th><th>Default</th><th>Name</th><th>Description</th></tr>
<tr><td rowspan="6">0x10</td><td>7</td><td>1</td><td>MPLL_BP</td><td>MPLL_BP
• When MPLL_BP=0, set for normal MCLK operation.
• When MPLL_BP=1, set for internal PLL bypass.</td></tr>
<tr><td>6</td><td>1</td><td>DPLL_BP</td><td>DPLL_BP
• When DPLL_BP=0, set for DCLK operation.
• When DPLL_BP= 1, set for internal PLL bypass.</td></tr>
<tr><td>5-4</td><td>-</td><td>—</td><td>Reserved.</td></tr>
<tr><td>3-2</td><td>0</td><td>DPLL_SOURCE[1:0]</td><td>Source of display clock.<table><tr><th>DPLL_OD</th><th>Set for</th></tr><tr><td>0</td><td>DCLK PLL</td></tr><tr><td>1</td><td>SV_CLK</td></tr><tr><td>2</td><td>PV_CLK</td></tr><tr><td>3</td><td>TESTCLK</td></tr></table></td></tr>
<tr><td>1</td><td>1</td><td>DPLL_VON</td><td>Reprogram enable for DCLK PLL. The DCLK PLL is reprogrammed using DCLK_MULT (0x12) on a rising edge of this bit.</td></tr>
<tr><td>0</td><td>1</td><td>MPLL_VON</td><td>Reprogram enable for MCLK PLL. The MCLK PLL is reprogrammed using MCLK_NUM (0x11:5-0) and MCLK_DEN (0x11:7-6) on a rising edge of this bit.</td></tr>
<tr><td>0x11</td><td>7-0</td><td>4e</td><td>MPLL_NF[7:0]</td><td>Numerator of MPLL driver (low).</td></tr>
<tr><td rowspan="3">0x12</td><td>7</td><td>0</td><td>MPLL_NF[8]</td><td>Numerator of MPLL driver (high).</td></tr>
<tr><td>6-5</td><td>1</td><td>MPLL_OD[1:0]</td><td>Output divide for MPLL.<table><tr><th>MPLL_OD</th><th>Description</th></tr><tr><td>00</td><td>Divide by 1</td></tr><tr><td>01</td><td>Divide by 2</td></tr><tr><td>10</td><td>Divide by 2</td></tr><tr><td>11</td><td>Divide by 4</td></tr></table></td></tr>
<tr><td>4-0</td><td>2</td><td>MPLL_R[4:0]</td><td>Denominator of MPLL divider.</td></tr>
</table>

Table 5-3 Clock Generator and Programming Unit Registers (continued)

Sub Address	Bits	Default	Name	Description
0x13	7	0	MPLL_PD	Power Down MPLL. • When MPLL_PD=0, set for normal PLL operation. • When MPLL_PD=1, set for power down mode.
	6	0	MPLL_OE	Output Enable MPLL. • When MPLL_OE=0, set for normal PLL operation. • When MPLL_OE=1, set for output disable.
	5	0	DPLL_PD	Power Down DPLL. • When DPLL_PD=0, set for normal PLL operation. • When DPLL_PD=1, set for power down mode.
	4	0	DPLL_OE	Output Enable DPLL. • When DPLL_OE=0, set for normal PLL operation. • When DPLL_OE=1, set for output disable.
	3-2	-	—	Reserved.
	1	1	MCLK_BYPASS	Bypass enable for MCLK PLL. • When MCLK_BYPASS=0, output from MCLK PLL. • When MCLK_BYPASS=1, MCLK=FCLK.
	0	1	DCLK_BYPASS	Bypass enable for DCLK PLL. • When DCLK_BYPASS=0, output from DCLK PLL. • When DCLK_BYPASS=1, DCLK=clock selected by DPLL_SOURCE.
0x14	0	0	BUFFER_2W_WR	Two-Wire Buffer bit. • When BUFFER_2W_WR=1, buffer subsequent 2-Wire writes. • When BUFFER_2W_WR=0, allow the data of all previous and subsequent 2-Wire writes to be passed through to the rest of the PW1225.
0x15	7-0	6a	DPLL_NF[7:0]	Numerator of DPLL divider (low).
0x16	7	0	DPLL_NF[8]	Numerator of DPLL divider (high).
	6-5	3	DPLL_OD[1:0]	Output divide for DPLL. DPLL_OD / Description 00 Divide by 1 01 Divide by 2 10 Divide by 2 11 Divide by 4
	4-0	3	DPLL_R[4:0]	Denominator of DPLL divider.

5.4 PV Interface Registers

Table 5-4 lists the PV Interface Registers.

Table 5-4 PV Interface Registers

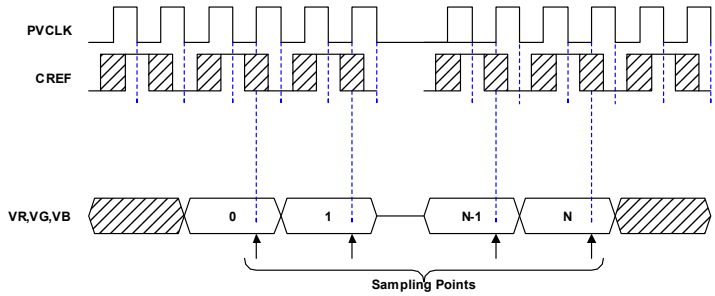
Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x20	r or rw	0	pv_clk_edge	pv_video_err	pv_inp_ format2	pv_inp_ format1	pv_inp_ format0	pv_type1	pv_type0
0x21	rw	cref_mode	cref_ena	pv_data_ format1	pv_data_ format0	pv_uv_ encode1	pv_uv_ encode0	pv_y_adj1	pv_y_adj0
0x22	rw	cref_pol	hspv_pol	vspv_pol	pv_422_ conv	pv_detect_ form	pv_prog_il	pv_prog_siz	pv_offset
0x23	rw	pv_hsta7	pv_hsta6	pv_hsta6	pv_hsta4	pv_hsta3	pv_hsta2	pv_hsta1	pv_hsta0
0x24	rw	pv_odd_vsta7	pv_odd_vsta6	pv_odd_vsta5	pv_odd_vsta4	pv_odd_vsta3	pv_odd_vsta2	pv_odd_vsta1	pv_hsta8
0x25	rw	0	pv_even_ vsta6	pv_even_ vsta5	pv_even_ vsta4	pv_even_ vsta3	pv_even_ vsta2	pv_even_ vsta1	pv_even_ vsta0
0x26	rw	pv_prog_ hlen7	pv_prog_ hlen6	pv_prog_ hlen5	pv_prog_ hlen4	pv_prog_ hlen3	pv_prog_ hlen2	pv_prog_ hlen1	pv_prog_ hlen0
0x27	rw	pv_prog_ vlen7	pv_prog_ vlen6	pv_prog_ vlen6	pv_prog_ vlen4	pv_prog_ vlen3	pv_prog_ vlen2	pv_prog_ vlen1	pv_prog_ vlen0

Table 5-5 provides detailed descriptions of the PV Interface Registers.

Table 5-5 PV Interface Configuration Details

<table>
<tr><th>Sub Address</th><th>Bits</th><th>Default</th><th>Name</th><th>Description</th></tr>
<tr><td rowspan="3">0x20</td><td>6</td><td>0</td><td>PV_CLK_EDGE</td><td>Clock edge adjustment.
• When PV_CLK_EDGE=0, sample data on the rising edge of PV_CLK.
• When PV_CLK_EDGE=1, sample data on the falling edge.</td></tr>
<tr><td>5</td><td>0</td><td>PV_VIDEO_ERR</td><td>Video error at the PV interface. Can be cleared only by a hard or soft reset. Read only.
• When PV_VIDEO_ERR=0, set for normal operation.
• When PV_VIDEO_ERR=1, indicates improperly framed video data.</td></tr>
<tr><td>4-2</td><td>0</td><td>PV_INP_FORMAT [2:0]</td><td>Input format at the PV interface appropriate to PV_TYPE. Specifies either the format or reports the format detected, according to the value of PV_DETECT_FORM. Read only when PV_DETECT_FORM=1.
<table>
<tr><th>PV_INP_FORMAT</th><th>Description</th></tr>
<tr><td>0</td><td>NTSC or 480i</td></tr>
<tr><td>2</td><td>PAL</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>0</td><td>PV_TYPE[1:0]</td><td>Input type at the PV interface.
<table>
<tr><th>PV_TYPE</th><th>Description</th></tr>
<tr><td>0</td><td>NTSC / PAL</td></tr>
<tr><td>1</td><td>480i</td></tr>
</table></td></tr>
</table>

Table 5-5 PV Interface Configuration Details (continued)

<table>
<tr><th>Sub Address</th><th>Bits</th><th>Default</th><th>Name</th><th>Description</th></tr>
<tr><td rowspan="4">0x21</td><td>7</td><td>0</td><td>CREF_MODE</td><td>Mode for CREF (clock reference) timing. Valid only when CREF_ENA=1.
• When CREF_MODE=0, set to positive edge enable.
• When CREF_MODE=1, set to negative edge enable.
When CREF_MOD =0:
 

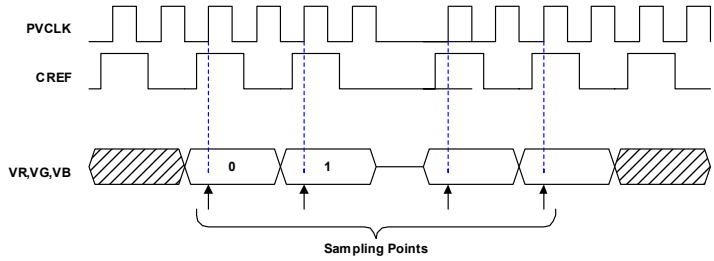
When CREF_MODE=1:
 
</td></tr>
<tr><td>6</td><td>0</td><td>CREF_ENA</td><td>Active high enable for CREF pin.</td></tr>
<tr><td>5-4</td><td>3</td><td>PV_DATA_ FORMAT[1:0]</td><td>Data format at the PV interface.
<table><tr><th>PV_DATA_FORMAT</th><th>Format</th></tr><tr><td>1</td><td>4:1:1</td></tr><tr><td>2</td><td>4:2:2</td></tr><tr><td>3</td><td>4:4:4</td></tr></table></td></tr>
<tr><td>3-2</td><td>2</td><td>PV_UV_ENCODE [1:0]</td><td>Encoding for UV components at the PV interface.
<table><tr><th>PV_UV_ENCODE</th><th>Description</th></tr><tr><td>00</td><td>1’s complement numbers</td></tr><tr><td>01</td><td>2’s complement numbers</td></tr><tr><td>10</td><td>Positive binary numbers</td></tr><tr><td>11</td><td>Reserved.</td></tr></table></td></tr>
<tr><td>1-0</td><td>0</td><td>PV_Y_ADJ[1:0]</td><td>Y Component adjust at the PV interface.
• When PV_Y_ADJ=1, delay the adjustment.
• When PV_Y_ADJ=2, advance the Y component one pixel (cycle) relative to the UV components. Otherwise, no adjustment.</td></tr>
</table>

Table 5-5 PV Interface Configuration Details (continued)

<table>
<tr><th>Sub Address</th><th>Bits</th><th>Default</th><th>Name</th><th>Description</th></tr>
<tr><td rowspan="8">0x22</td><td>7</td><td>0</td><td>CREF_POL</td><td>Polarity of CREF pin.
• When CREF_POL=0, polarity is active high.
• When CREF_POL=1, polarity is active low.</td></tr>
<tr><td>6</td><td>0</td><td>HSPV_POL</td><td>Polarity of HSPV pin.
• When HSPV_POL=0, polarity is active high.
• When HSPV_POL=1, polarity is active low.</td></tr>
<tr><td>5</td><td>0</td><td>VSPV_POL</td><td>Polarity of VSPV pin.
• When VSPV_POL=0, polarity is active high.
• When VSPV_POL=1, polarity is active low.</td></tr>
<tr><td>4</td><td>1</td><td>PV_422_CONV</td><td>Method for converting from 4:1:1 to 4:2:2 or from 4:2:2 to 4:4:4 formats at the PV interface.
• When PV_422_CONV=0, simply copy the UV sample.
• When PV_422_CONV=1, use bilinear interpolation.</td></tr>
<tr><td>3</td><td>1</td><td>PV_DETECT_ FORM</td><td>Format detection enable on video data at the PV interface. Active high.
• When PV_DETECT_FORM =0, the input format is specified via the PV_FORMAT (0x20:4-2) field.
• When PV_DETECT_FORM =1, use auto detection.</td></tr>
<tr><td>2</td><td>0</td><td>PV_PROG_IL</td><td>Program enable for interlaced format. Valid only when PV_PROG_SIZ (0x22:1)=1.
• When PV_PROG_IL=1, specifies the input mode as interlaced.
• When PV_PROG_IL is other than 1, the input data is treated as progressive.</td></tr>
<tr><td>1</td><td>0</td><td>PV_PROG_SIZ</td><td>Program enable for the resolution of the active region at the PV interface using the PV_PROG_HLEN (0x26) and PV_PROG_VLEN (0x27) fields.
• When PV_PROG_SIZ=0, assumes the values follow the defaults:
<table>
<tr><th>Video Format</th><th>Width</th><th>Height</th><th>Scan Format</th></tr>
<tr><td>NTSC / 480i</td><td>720</td><td>240</td><td rowspan="2">Interlaced</td></tr>
<tr><td>PAL</td><td>720</td><td>288</td></tr>
</table>
• When PV_PROG_SIZ=1, use PV_PROG_HLEN and PV_PROG_VLEN.</td></tr>
<tr><td>0</td><td>0</td><td>PV_OFFSET</td><td>Program enable for the top left corner of the active region at the PV interface using the PV_HSTA (0x23, 0x24:0), PV_ODD_VSTA (0x24:7-1), and PV_EVEN_VSTA (0x25) fields.
• When PV_OFFSET=0, assumes the offset values follow the defaults:
<table>
<tr><th>Video Format</th><th>pv_odd_vsta</th><th>pv_even_vsta</th><th>pv_hsta</th></tr>
<tr><td>NTSC</td><td>16</td><td>16</td><td>122</td></tr>
<tr><td>PAL</td><td>22</td><td>22</td><td>132</td></tr>
<tr><td>480i</td><td>17</td><td>16</td><td>124</td></tr>
</table>
• When PV_OFFSET=1, use values from Registers 0x23, 0x24, and 0x25.</td></tr>
<tr><td>0x23</td><td>7-0</td><td>7A</td><td>PV_HSTA[7:0]</td><td>Lower 8 bits of the starting pixel, relative to the horizontal sync for active video at the PV interface. Valid only when PV_OFFSET (0x22:0)=1.
Enter ‘0’ for 0, ‘1’ for 1, ‘2’ for 2 pixels, etc.</td></tr>
</table>

Table 5-5 PV Interface Configuration Details (continued)

Sub Address	Bits	Default	Name	Description
0x24	7-1	10	PV_ODD_VSTA [6:0]	Starting line relative to the vertical sync for an active odd video field at the PV interface. Valid only when PV_OFFSET (0x22:0)=1. Enter ‘0’ for 0, ‘1’ for 1, ‘2’ for 2 lines, etc.
	0	0	PV_HSTA[8]	Most significant bit of starting pixel relative to the horizontal sync for active video at the PV interface. See 0x23.
0x25	6-0	10	PV_EVEN_VSTA [6:0]	Starting line relative to the vertical sync for an active even video field at the PV interface. Alternately, starting line for an active video frame in the case of progressive input data. Valid only when PV_OFFSET (0x22:0)=1. Enter ‘0’ for 0, ‘1’ for 1, ‘2’ for 2 lines, etc.
0x26	7-0	59	PV_PROG_HLEN [7:0]	Number of pixels in the active horizontal region at the PV interface. Valid only when PV_PROG_SIZ (0x22:1)=1. Enter ‘0’ for 8, ‘1’ for 16, ‘2’ for 24 pixels, etc.
0x27	7-0	77	PV_PROG_VLEN [7:0	Number of lines in the active vertical region at the PV interface. Valid only when PV_PROG_SIZ (0x22:1)=1. • For interlaced data, enter ‘0’ for 2, ‘1’ for 4, ‘2’ for 6 lines, etc. The odd field is assumed to include one additional line. • For progressive data, enter ‘0’ for 4, ‘1’ for 8, ‘2’ for 12 lines, etc.

5.5 SV Interface Registers

Table 5-6 lists the SV Interface Registers.

Table 5-6 SV Interface Registers

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x28	r or rw	0	0	sv_video_err	sv_inp_ format2	sv_inp_ format1	sv_inp_ format0	sv_type1	sv_type0
0x29	rw	0	0	sv_data_ format1	sv_data_ format0	sv_uv_ encodet1	sv_uv_ encodet0	sv_clk_del	sv_clk_edge
0x2A	rw	0	hssv_pol	vssv_pol	sv_422_ conv	sv_detect_ form	sv_prog_il	sv_prog_siz	sv_offset
0x2B	rw	sv_hsta7	sv_hsta6	sv_hsta5	sv_hsta4	sv_hsta3	sv_hsta2	sv_hsta1	sv_hsta0
0x2C	rw	sv_odd_vsta6	sv_odd_vsta5	sv_odd_vsta4	sv_odd_vsta3	sv_odd_vsta2	sv_odd_vsta1	sv_odd_vsta0	sv_hsta8
0x2D	rw	0	sv_even_ vsta6	sv_even_ vsta5	sv_even_ vsta4	sv_even_ vsta3	sv_even_ vsta2	sv_even_ vsta1	sv_even_ vsta0
0x2E	rw	sv_prog_ hlen7	sv_prog_ hlen6	sv_prog_ hlen5	sv_prog_ hlen4	sv_prog_ hlen3	sv_prog_ hlen2	sv_prog_ hlen1	sv_prog_ hlen0
0x2F	rw	sv_prog_ vlen7	sv_prog_ vlen6	sv_prog_ vlen5	sv_prog_ vlen4	sv_prog_ vlen3	sv_prog_ vlen2	sv_prog_ vlen1	sv_prog_ vlen0

Table 5-7 provides detailed descriptions of the SV Interface Registers.

Table 5-7 SV Interface Register Details

<table>
<tr><th>Sub Address</th><th>Bits</th><th>Default</th><th>Name</th><th>Description</th></tr>
<tr><td rowspan="2">0x28</td><td>5</td><td>0</td><td>SV_VIDEO_ERR</td><td>Video error at the SV interface. Can be cleared only by a hard or soft reset. Read only.
• When SV_VIDEO_ERR=0, set for normal operation.
• When SV_VIDEO_ERR=1, indicates improperly framed video data.</td></tr>
<tr><td>4-2</td><td>0</td><td>SV_INP_FORMAT [2:0]</td><td>Input format at the SV interface appropriate to the SV_TYPE (0x28:1-0). Specifies either the format or reports the format detected, according to the value of SV_DETECT_FORM (0x2A:3).
<table>
<tr><th>SV_TYPE</th><th>SV_INP_FORMAT</th><th>Video Format</th></tr>
<tr><td rowspan="2">00</td><td>000</td><td>NTSC</td></tr>
<tr><td>010</td><td>PAL</td></tr>
<tr><td>01</td><td>—</td><td>Reserved.</td></tr>
<tr><td>10</td><td>—</td><td>Reserved.</td></tr>
<tr><td>11</td><td>—</td><td>Reserved.</td></tr>
</table>
When SV_DETECT_FORM=1, this is Read Only.</td></tr>
<tr><td>1-0</td><td>0</td><td>SV_TYPE[1:0]</td><td>Input type at the SV interface.
<table>
<tr><th>SV_TYPE</th><th>Description</th></tr>
<tr><td>0</td><td>NTSC / PAL</td></tr>
</table></td></tr>
</table>

Table 5-7 SV Interface Register Details (continued)

<table>
<tr><th>Sub Address</th><th>Bits</th><th>Default</th><th>Name</th><th>Description</th></tr>
<tr><td rowspan="4">0x29</td><td>5-4</td><td>2</td><td>SV_DATA_ FORMAT[1:0]</td><td>Data format at the SV interface. Enter:
<table><tr><th>SV_DATA_FORMAT</th><th>Description</th></tr><tr><td>0</td><td>SV mode 0.</td></tr><tr><td>2</td><td>Slave side of SV mode 2.</td></tr><tr><td>3</td><td>Master side of SV mode 2.</td></tr></table></td></tr>
<tr><td>3-2</td><td>2</td><td>SV_UV_ENCODE [1:0]</td><td>Encoding for UV components at the SV interface.
<table><tr><th>SV_UV_ENCODE</th><th>Description</th></tr><tr><td>00</td><td>1’s complement numbers.</td></tr><tr><td>01</td><td>2’s complement numbers.</td></tr><tr><td>10</td><td>Positive binary numbers.</td></tr><tr><td>11</td><td>Reserved.</td></tr></table></td></tr>
<tr><td>1</td><td>0</td><td>SV_CLK_DEL</td><td>Clock delay adjustment.
• When SV_CLK_DEL=0, set for normal operation.
• When SV_CLK_DEL=1, sample data with a one clock cycle delay, effectively reversing the luma and chroma values.</td></tr>
<tr><td>0</td><td>0</td><td>SV_CLK_EDGE</td><td>Clock edge adjustment.
• When SV_CLK_EDGE=0, sample data on the rising edge of SV_CLK.
• When SV_CLK_EDGE=1, sample data on the falling edge.</td></tr>
</table>

Table 5-7 SV Interface Register Details (continued)

<table>
<tr><th>Sub Address</th><th>Bits</th><th>Default</th><th>Name</th><th>Description</th></tr>
<tr><td rowspan="8">0x2A</td><td>6</td><td>0</td><td>HSSV_POL</td><td>Polarity of HSSV_POL pin.
• When HSSV_POL=0, polarity is active high.
• When HSSV_POL=1, polarity is active low.</td></tr>
<tr><td>5</td><td>0</td><td>VSSV_POL</td><td>Polarity of VSSV_POL pin.
• When VSSV_POL=0, polarity is active high.
• When VSSV_POL=1, polarity is active low.</td></tr>
<tr><td>4</td><td>1</td><td>SV_422_CONV</td><td>Convert from 4:1:1 to 4:2:2 or from 4:2:2 to 4:4:4.
• When SV_422_CONV=0, copy the UV sample.
• When SV_422_CONV=1, interpolate the new UV value.</td></tr>
<tr><td>3</td><td>1</td><td>SV_DETECT_ FORM</td><td>Format detection enable on video data at the SV interface. Active high. Valid only when SV_PROG_SIZ (0x2A:1)=0.
• When SV_DETECT_FORM=0, the input format is specified via the SV_FORMAT (0x28:4-2) field.
• When SV_DETECT_FORM=1, the input format is detected.</td></tr>
<tr><td>2</td><td>0</td><td>SV_PROG_IL</td><td>Program enable for interlaced format. Valid only when SV_PROG_SIZ (0x2A:1)=1.
• When SV_PROG_IL=1, specifies the input mode as interlaced.
• Otherwise, the input data is treated as progressive.</td></tr>
<tr><td>1</td><td>0</td><td>SV_PROG_SIZ</td><td>Program enable for the resolution of the active region at the SV interface via the SV_PROG_HLEN (0x2E) and SV_PROG_VLEN (0x2F) fields.
• When SV_PROG_SIZ=0, assumes the values follow the defaults in this table:
<table>
<tr><th>Video Format</th><th>Width</th><th>Height</th><th>Scan Format</th></tr>
<tr><td>NTSC / 480i</td><td>720</td><td>240</td><td rowspan="2">Interlaced</td></tr>
<tr><td>PAL</td><td>720</td><td>288</td></tr>
</table>
• When SV_PROG_SIZ=1, use the values in Registers 0x2E and 0x2F.</td></tr>
<tr><td>0</td><td>0</td><td>SV_OFFSET</td><td>Program enable for the top left corner of the active region at the SV interface via the sv_hsta (0x2B, 0x2C:0), sv_odd_vsta (0x2C:7-1), and sv_even_vsta (0x2D) fields.
• When SV_OFFSET=0, the offset values follow the defaults.
<table>
<tr><th>Video Format</th><th>SV_ODD_VSTA</th><th>SV_EVEN_VSTA</th><th>SV_HSTA</th></tr>
<tr><td>NTSC</td><td>16</td><td>16</td><td>122</td></tr>
<tr><td>PAL</td><td>22</td><td>22</td><td>132</td></tr>
<tr><td>480i</td><td>17</td><td>16</td><td>124</td></tr>
</table>
• When SV_OFFSET=1, use the values in registers 0x2B, 0x2C, and 0x2D.</td></tr>
<tr><td>0x2B</td><td>7-0</td><td>7A</td><td>SV_HSTA[7:0]</td><td>Lower 8 bits of starting pixel relative to the horizontal sync for active video at the SV interface. Valid only when SV_OFFSET (0x2A:0)=1.
Enter ‘0’ for 0, ‘1’ for 1, ‘2’ for 2 pixels, etc.</td></tr>
</table>

Table 5-7 SV Interface Register Details (continued)

Sub Address	Bits	Default	Name	Description
0x2C	7-1	10	SV_ODD_VSTA [6:0]	Starting line relative to the vertical sync for an active odd video field at the SV interface. Valid only when SV_OFFSET (0x2A:0)=1. Enter ‘0’ for 0, ‘1’ for 1, ‘2’ for 2 lines, etc.
	0	0	SV_HSTA[8]	Most significant bit (MSB) of the starting pixel relative to horizontal sync for active video at the SV interface. See 0x2B.
0x2D	6-0	10	SV_EVEN_VSTA [6:0]	Starting line relative to the vertical sync for an active even video field at the SV interface. Alternately, starting line for an active video frame in the case of progressive input data. Valid only when SV_OFFSET (0x2A:0) =1. Enter ‘0’ for 0, ‘1’ for 1, ‘2’ for 2 lines, etc.
0x2E	7-0	59	SV_PROG_HLEN [7:0]	Number of pixels in the active horizontal region at the SV interface. Valid only when SV_PROG_SIZ (0x2A:1) =1. Enter ‘0’ for 8, ‘1’ for 16, ‘2’ for 24 pixels, etc.
0x2F	7-0	77	SV_PROG_VLEN [7:0]	Number of lines in the active vertical region at the SV interface. Valid only when SV_PROG_SIZ (0x2A:1)=1. • For interlaced data, enter ‘0’ for 2, ‘1’ for 4, ‘2’ for 6 lines, etc. The odd field is assumed to include one additional line. • For progressive data, enter ‘0’ for 4, ‘1’ for 8, ‘2’ for 12 lines, etc.

5.6 Input Channel Registers

Table 5-8 lists the Input Channel Registers.

Table 5-8 Input Channel Registers

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x30	r or rw	0	0	0	0	0	0	il_srstN_fb	srstN
0x31	rw	0	0	0	0	odd_det_byp	non_std_det	il_if_num1	il_if_num0
0x32	rw	odd_win_siz7	odd_win_siz6	odd_win_siz5	odd_win_siz4	odd_win_siz3	odd_win_siz2	odd_win_siz1	odd_win_siz0
0x33	rw	0	0	bad_cut_ factor	bad_cut_enab	0	mn_testN	mn_chroma	mn_bypass

Table 5-9 provides detailed descriptions of the Input Channel Registers.

Table 5-9 Input Channel Register Details

Sub Address	Bits	Default	Name	Description
0x30	1	1	IL_SRSTN_FB	Software reset echo (*feedback*) for the interlaced channel. Can be used to detect the absence of a clock in the interlaced channel. Read only.
	0	1	SRSTN	Software reset. • When SRSTN=0, reset the video input block. • When SRSTN=1, resume operation.
0x31	3	0	ODD_DET_BYP	Odd Detection Bypass. This bit must be 0 if NON_STD_DET is set to 1. • When ODD_DET_BYP=0, set odd generation. • When ODD_DET_BYP=1, bypass odd generation.
	2	0	NON_STD_ DET	Non-Standard Detection. • When NON_STD_DET=0, use standard field polarity detection. • When NON_STD_DET=1, use non-standard detection.
	1-0	2	IL_IF_NUM[1:0]	Input interface for the interlaced channel. IL_IF_NUM / Description 0 – None 1 – PV 2 – SV 3 – None
0x32	7-0	20	ODD_WIN_SIZ[7:0]	Define window size for odd sync detection on all interfaces.
0x33	5	0	BAD_CUT_FACTOR	Bad cut factor. • When BAD_CUT_FACTOR=0, detection is stringent (more sensitive). • When BAD_CUT_FACTOR=1, detection is relaxed (less sensitive).
	4	0	BAD_CUT_ENAB	Bad cut enable. • When BAD_CUT_ENAB=0, disable. • When BAD_CUT_ENAB=1, enable.
	3	—	—	Reserved.
	2	1	MN_TESTN	Motion and noise test enable. Active low.

Table 5-9 Input Channel Register Details (continued)

Sub Address	Bits	Default	Name	Description
0x33 (cont'd)	1	1	MN_CHROMA	Chroma enable. • When MN_CHROMA=0, use luma values only. • When MN_CHROMA=1, include chroma in the calculation of motion detection and noise reduction.
	0	0	MN_BYPASS	Motion and noise bypass enable. Enter '1' to "bypass" the motion and noise function on the interlaced channel.

5.7 Input to Memory Registers

Table 5-10 lists the Input to Memory Registers.

Table 5-10 Input to Memory Registers

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x40	rw	i2m_siz	i2m_hlen6	i2m_hlen5	i2m_hlen4	i2m_hlen3	i2m_hlen2	i2m_hlen1	i2m_hlen0
0x41	rw	i2m_vlen7	i2m_vlen6	i2m_vlen5	i2m_vlen4	i2m_vlen3	i2m_vlen2	i2m_vlen1	i2m_vlen0

Table 5-11 provides detailed descriptions of the Input to Memory Registers.

Table 5-11 Input to Memory Register Details

<table>
<tr><th>Sub Address</th><th>Bits</th><th>Default</th><th>Name</th><th>Description</th></tr>
<tr><td rowspan="2">0x40</td><td>7</td><td>0</td><td>I2M_SIZ</td><td>Program enable for the size of the region transferred from the interlaced channel.
• When I2M_SIZ=0, assumes the region size information to be passed directly from the input unit through the I2M_MODE bus. The I-channel image written into the frame buffer has one of the following preset resolutions:
<table>
<tr><th>Input Format</th><th>Width</th><th>Height</th><th>Notes</th></tr>
<tr><td>NTSC</td><td rowspan="3">720</td><td rowspan="2">240</td><td rowspan="3">Interlaced</td></tr>
<tr><td>480i</td></tr>
<tr><td>PAL</td><td>288</td></tr>
</table>
• When I2M_SIZ=1, allows the programming of the region size through the I2M_HLEN (0x40:6-0) and I2M_VLEN (0x41) fields. When I2M_SIZ =1, the I-channel image written into memory is defined by the I2M_HLEN and I2M_VLEN registers.
<table>
<tr><th>Input Format</th><th>Width</th><th>Height</th></tr>
<tr><td>Non-standard</td><td>(i2m_hlen+1)x8</td><td>(i2m_vlen+1)x2</td></tr>
</table></td></tr>
<tr><td>6-0</td><td>59</td><td>I2M_HLEN[6:0]</td><td>Width of the region transferred from the interlaced channel. Valid only when I2M_SIZ (0x40:7)=1.
Enter ‘0’ for 8, ‘1’ for 16, ‘2’ for 24 pixels, etc.</td></tr>
<tr><td>0x41</td><td>7-0</td><td>77</td><td>I2M_VLEN[7:0]</td><td>Height of the region transferred from the interlaced channel. Valid only when I2M_SIZ (0x40:7)=1.
• For interlaced data, enter ‘0’ for 2, ‘1’ for 4, ‘2’ for 6 rows, etc. The odd field is assumed to include one additional row.
• For progressive data, enter ‘0’ for 4, ‘1’ for 8, ‘2’ for 12 rows, etc.</td></tr>
</table>

5.8 Input FIFO Registers

Table 5-12 lists the Input FIFO Registers.

Table 5-12 Input FIFO Registers

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x44	rw	i2m_offset	i2m_left6	i2m_left5	i2m_left4	i2m_left3	i2m_left2	i2m_left1	i2m_left0
0x45	rw	i2m_top7	i2m_top6	i2m_top6	i2m_top4	i2m_top3	i2m_top2	i2m_top1	i2m_top0
0x46	rw	0	0	0	0	0	0	i2m_step	i2m_freeze
0x47	rw	i2m_step_siz7	i2m_step_siz6	i2m_step_siz5	i2m_step_siz4	i2m_step_siz3	i2m_step_siz2	i2m_step_siz1	i2m_step_siz0

Table 5-13 provides detailed descriptions of the Input FIFO Registers.

Table 5-13 Input FIFO Register Details

Sub Address	Bits	Default	Name	Description
0x44	7	0	I2M_OFFSET	Destination offset enable for data transferred from the interlaced channel. • When I2M_OFFSET=0, assumes the top left corner to be at coordinate (0,0). • When I2M_OFFSET=1, allows the programming of the top left corner through the I2M_LEFT (0x44:6-0) and I2M_TOP (0x45) fields.
	6-0	0	I2M_LEFT[6:0]	Column coordinate for the top left corner for data transferred from the interlaced channel. Valid only when I2M_OFFSET (0x44:7)=1. Enter ‘0’ for column 0, ‘1’ for column 8, ‘2’ for column 16, etc.
0x45	7-0	0	I2M_TOP[7:0]	Row coordinate for the top left corner for data transferred from the interlaced channel. Valid only when I2M_OFFSET (0x44:7)=1. • For interlaced data, enter ‘0’ for row 0, ‘1’ for row 2, ‘2’ for row 4, etc. • For progressive data, enter ‘0’ for row 0, ‘1’ for row 4, ‘2’ for row 8, etc.
0x46	1	0	I2M_STEP	Step enable for data transferred from the interlaced channel. Valid only when I2M_FREEZE (0x46:0)=0. When ‘1’, allows the skipping of I2M_STEP_SIZ (0x47) field pairs (interlaced) or frames (progressive) between updates from the interlaced channel.
	0	0	I2M_FREEZE	Freeze enable for data transferred from the interlaced channel. • When I2M_FREEZE=0, set to normal operation. • When I2M_FREEZE=1, prevents the primary picture from being updated by the interlaced channel.
0x47	7-0	3	I2M_STEP_SIZ[7:0]	Step size for data transferred from the interlaced channel. Specifies the number of field pairs (interlaced) or frames (progressive) to skip between updates. Valid only when I2M_STEP (0x46:1)=1 and I2M_FREEZE (0x46:0)=0.

5.9 Memory Controller Registers

Table 5-14 lists the Memory Controller Registers.

Table 5-14 Memory Controller Registers

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x4C	r or rw	0	0	0	0	0	bg_status	bg_pattern	bg_ena
0x4D	rw	bg_color7	bg_color6	bg_color5	bg_color4	bg_color3	bg_color2	bg_color1	bg_color0
0x4E	rw	bg_color15	bg_color14	bg_color13	bg_color12	bg_color11	bg_color10	bg_color9	bg_color8
0x4F	rw	bg_color23	bg_color22	bg_color21	bg_color20	bg_color19	bg_color18	bg_color17	bg_color16
0x50	rw	0	0	0	0	0	pack720	row_len1	row_len0
0x51	rw	0	0	motion_siz	video_siz3	video_siz2	video_siz1	video_siz0	primary_siz
:		0	0	0	0	0	0	0	0
0x56	r or rw	m2d_vact	i2m_odd	i2m_vact	film_phase	film_mode	film_ctl	0	0
0x57	rw	0	0	mem_enaN	ntsc2pal	latency1	latency0	ref_len1	ref_len0

Table 5-15 provides detailed descriptions of the Memory Controller Registers.

Table 5-15 Memory Controller Register Details

Sub Address	Bits	Default	Name	Description
0x4C	2	0	BG_STATUS	Background paint status. Read only. • High when painting the background. • Low otherwise.
	1	0	BG_PATTERN	Background pattern control. • When BG_PATTERN=0, background pattern is a solid color. • When BG_PATTERN=1, directs a checkerboard pattern to be painted.
	0	0	BG_ENA	Background paint enable. Background paint is initiated by a rising edge on this bit.
0x4D	7-0	3A	BG_COLOR[7:0]	Lower order 8 bits of the background color. Used for ‘V’ data of YUV and ‘R’ data of RGB fields.
0x4E	7-0	48	BG_COLOR[15:8]	Middle order 8 bits of the background color. Used for ‘U’ data of YUV and ‘B’ data of RGB fields.
0x4F	7-0	70	BG_COLOR[23:16]	Higher order 8 bits of the background color. Used for ‘Y’ data of YUV and ‘G’ data of RGB fields.
0x50	2	0	PACK720	Enable packing of video and motion fields in memory to occupy exactly 720 pixels per line.
	1-0	2	ROW_LEN[1:0]	Length of a primary picture row in units of 512 bytes. The default default value corresponds to 768 video pixels. Enter ‘0’ for 1 unit, ‘1’ for 2 units, etc.

Table 5-15 Memory Controller Register Details (continued)

<table>
<tr><th>Sub Address</th><th>Bits</th><th>Default</th><th>Name</th><th>Description</th></tr>
<tr><td rowspan="3">0x51</td><td>5</td><td>0</td><td>MOTION_SIZ</td><td>Size of a primary picture motion field in units of 128 kB. The default is sufficient for NTSC/480i. Valid only when primary_siz (0x51:0)=1 or when not in NTSC/480i or PAL modes.</td></tr>
<tr><td>4-1</td><td>2</td><td>VIDEO_SIZ[3:0]</td><td>Size of a primary picture video field in units of 128 kB. Corresponds to bits [20:17] of the SDRAM byte address. The default is sufficient for NTSC/480i. Valid only when PRIMARY_SIZ (0x51:0)=1 or when not in NTSC/480i or PAL modes.
Enter ‘0’ for 128 kB, ‘1’ for 256 kB, '2' for 384 kB, and so on.</td></tr>
<tr><td>0</td><td>0</td><td>PRIMARY_SIZ</td><td>Program enable for the memory layout of the primary picture.
• When PRIMARY_SIZ=0, set NTSC/480i or PAL modes.
• When PRIMARY_SIZ=other, the VIDEO_SIZ (0x51:4-1) and MOTION_SIZ (0x51:5) fields apply.</td></tr>
<tr><td rowspan="7">0x56</td><td>7</td><td>—</td><td>M2D_VACT</td><td>Vertical active period for the display unit. Read only.</td></tr>
<tr><td>6</td><td>—</td><td>I2M_ODD</td><td>Polarity of the incoming interlaced field. Read only.
• When I2M_ODD=0, field is even.
• When I2M_ODD=1, field is odd.</td></tr>
<tr><td>5</td><td>—</td><td>I2M_VACT</td><td>Vertical active period for the incoming field. Read only.</td></tr>
<tr><td>4</td><td>0</td><td>film_phase</td><td>Phase used in film mode merging when under external control. Valid only when film_ctl (0x56:2)=1.</td></tr>
<tr><td>3</td><td>0</td><td>FILM_MODE</td><td>Enables film mode merging of fields instead of standard merging of fields when film data is detected under internal control. Active high.Valid only when film_ctl (0x56:2)=0.
Permits standard merging only when ‘0’.</td></tr>
<tr><td>2</td><td>0</td><td>FILM_CTL</td><td>Film mode control.
• When FILM_CTL=0 for internal control, FILM_MODE (0x56:3) applies.
• When FILM_CTL=1 for external control, FILM_MODE (0x56:4) applies.</td></tr>
<tr><td>1-0</td><td>0</td><td>FILM_SENS[1:0]</td><td>Film mode sensitivity. Set to 0 least sensitive, 3 for most rigorous requirements for detecting film.
<table>
<tr><th>#</th><th>Description</th></tr>
<tr><td>00</td><td>20 fields (least sensitive)</td></tr>
<tr><td>01</td><td>40 fields</td></tr>
<tr><td>10</td><td>60 fields</td></tr>
<tr><td>11</td><td>80 fields (most rigorous)</td></tr>
</table></td></tr>
</table>

Table 5-15 Memory Controller Register Details (continued)

Sub Address	Bits	Default	Name	Description
0x57	5	0	MEM_ENA_N	Memory controller enable. Active low. Toggle high and then low to reinitialize the memory controller, including the external SDRAM, without having to reset the chip.
	4	0	NTSC2PAL	Down-rate conversion enable, especially for: • NTSC (60 Hz) to PAL (50 Hz), or • 480p (60 Hz) to 576p (50 Hz).
	3-2	0	LATENCY[1:0]	Read latency. Enter '0' for 3 cycles, '1' for 4 cycles, etc.
	1-0	0	REF_LEN[1:0]	Maximum Refresh Interval. Refresh length. REF_LEN / Frequency Range MCLK 00 – 10 – 50 MHz 01 – 51 – 80 MHz 10 – 81 – 110 MHz 11 – > 110 MHz

5.10 Display FIFO Registers

Table 5-16 lists the Display FIFO Registers.

Table 5-16 Display FIFO Registers

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x58	rw	m2d_offset	m2d_left6	m2d_left5	m2d_left4	m2d_left3	m2d_left2	m2d_left1	m2d_left0
0x59	rw	m2d_top7	m2d_top6	m2d_top5	m2d_top4	m2d_top3	m2d_top2	m2d_top1	m2d_top0

Table 5-17 provides detailed descriptions of the Display FIFO Registers.

Table 5-17 Display FIFO Register Details

Sub Address	Bits	Default	Name	Description
0x58	7	0	M2D_OFFSET	Source offset enable for data transferred from the primary picture. • When M2D_OFFSET=0, assumes the top left corner is at coordinate (0,0). • When M2D_OFFSET =1, allows the programming of the top left corner through the M2D_LEFT (0x58:6-0) and M2D_TOP (0x59) fields.
	6-0	0	M2D_LEFT[6:0]	Column coordinate for the top left corner of the primary picture. Valid only when M2D_OFFSET (0x58:7)=1. Enter '0' for column 0, '1' for column 8, '2' for column 16, etc.
0x59	7-0	0	M2D_TOP[7:0]	Row coordinate for the top left corner of the primary picture. Valid only when M2D_OFFSET (0x58:7)=1. • For interlaced data, enter '0' for row 0, '1' for row 2, '2' for row 4, etc. • For progressive data, enter '0' for row 0, '1' for row 4, '2' for row 8, etc.

5.11 Film Mode Status Registers

Table 5-20 lists the Film Mode Status Registers.

Table 5-18 Film Mode Status Registers

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x5A	rw	0	0	0	dsp_odd	32_film_mode	22_film_mode	odd_field_id	even_field_id
0x5B	rw	32_film_phase 3	32_film_phase 2	32_film_phase 1	32_film_phase 0	22_film_phas e 3	22_film_phase 2	22_film_phase 1	22_film_phase 0

Table 5-17 provides detailed descriptions of the Display FIFO Registers.

Table 5-19 Display FIFO Register Details

Sub Address	Bits	Default	Name	Description
0x5A	4	-	DSP_ODD	DSP_ODD status, read only.
	3	-	32_FILM_MODE	3:2 pull-down film mode status, read only.
	2	-	22_FILM_MODE	2:2 pull-down film mode status, read only.
	1	-	ODD_FIELD_ID	Odd field ID for merge, read only.
	0	-	EVEN_FIELD_ID	Even field ID for merge, read only.
0x5B	7-4	-	32_FILM_PHASE [3:0]	3:2 pull-down film phase status, read only.
	3-0	-	22_FILM_PHASE [3:0]	2:2 pull-down film phase status, read only.

5.12 Memory-to-Display Registers

Table 5-20 lists the Memory-to-Display Registers.

Table 5-20 Memory-to-Display Registers

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x5C	rw	m2d_siz	m2d_hlen6	m2d_hlen5	m2d_hlen4	m2d_hlen3	m2d_hlen2	m2d_hlen1	m2d_hlen0
0x5D	rw	m2d_vlen7	m2d_vlen6	m2d_vlen6	m2d_vlen4	m2d_vlen3	m2d_vlen2	m2d_vlen1	m2d_vlen0

Table 5-21 provides detailed descriptions of the Memory-to-Display Registers.

Table 5-21 Memory-to-Display Register Details

<table>
<tr><th>Sub Address</th><th>Bits</th><th>Default</th><th>Name</th><th>Description</th></tr>
<tr><td rowspan="2">0x5C</td><td>7</td><td>0</td><td>M2D_SIZ</td><td>Program enable for the size of the region transferred from the primary picture.
• When M2D_SIZ=0, assumes the region size information to be passed directly from the input unit through the I2M_MODE bus, according to. The source image is an identical copy of I-channel data.
<table>
<tr><th>Input Format</th><th>Width</th><th>Height</th><th>Notes</th></tr>
<tr><td>NTSC</td><td rowspan="3">720</td><td rowspan="2">240</td><td rowspan="3">Interlaced data</td></tr>
<tr><td>480i</td></tr>
<tr><td>PAL</td><td>288</td></tr>
</table>
• When M2D_SIZ=1, allows the programming of the region size. The source image read from memory is defined by the M2D_HLEN (0x5C:6-0) and M2D_VLEN (0x5D) registers.
<table>
<tr><th>Input Format</th><th>Width</th><th>Height</th></tr>
<tr><td>Non-standard</td><td>(m2d_hlen+1)x8</td><td>(m2d_vlen+1)x2</td></tr>
</table></td></tr>
<tr><td>6-0</td><td>59</td><td>M2D_HLEN[6:0]</td><td>Width of the region transferred from the primary picture. Valid only when M2D_SIZ (0x5C:7)=1.
Enter ‘0’ for 8, ‘1’ for 16, ‘2’ for 24 pixels, etc.</td></tr>
<tr><td>0x5D</td><td>7-0</td><td>77</td><td>M2D_VLEN[7:0]</td><td>Height of the region transferred from the primary picture. Valid only when M2D_SIZ (0x5C:7)=1.
• For interlaced data, enter ‘0’ for 2, ‘1’ for 4, ‘2’ for 6 rows, etc. The odd field is assumed to include one additional row.
• For progressive data, enter ‘0’ for 4, ‘1’ for 8, ‘2’ for 12 rows, etc.</td></tr>
</table>

5.13 Display Timing Registers

Table 5-22 lists the Display Timing Registers.

Table 5-22 Display Timing Registers

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x60	rw	0	0	0	0	0	il_output	dsp_sync	dsp_ena
0x61	rw	0	0	0	il_60i	dvq_polN	oeq_polN	vsq_polN	hsq_polN
0x62	rw	hsp7	hsp6	hsp5	hsp4	hsp3	hsp2	hsp1	hsp0
0x63	rw	hbp7	hbp6	hbp5	hbp4	hbp3	hbp2	hbp1	hbp0
0x64	rw	hap7	hap6	hap5	hap4	hap3	hap2	hap1	hap0
0x65	rw	hlp7	hlp6	hlp5	hlp4	hlp3	hlp2	hlp1	hlp0
0x66	rw	0	0	0	0	hlp11	hlp10	hlp9	hlp8
0x67	rw	vsp7	vsp6	vsp5	vsp4	vsp3	vsp2	vsp1	vsp0
0x68	rw	vbp7	vbp6	vbp5	vbp4	vbp3	vbp2	vbp1	vbp0
0x69	rw	vap7	vap6	vap5	vap4	vap3	vap2	vap1	vap0
0x6A	rw	vlp7	vlp6	vlp5	vlp4	vlp3	vlp2	vlp1	vlp0
0x6B	rw	0	0	0	0	vlp11	vlp10	vlp9	vlp8
0x6C	rw	vbp_e7	vbp_e6	vbp_e5	vbp_e4	vbp_e3	vbp_e2	vbp_e1	vbp_e0

Table 5-23 provides detailed descriptions of the Display Timing Registers.

Table 5-23 Display Timing Register Details

Sub Address	Bits	Default	Name	Description
0x60	3	0	—	Reserved. Write only a “0” to this bit position.
	2	0	IL_OUTPUT	Interlaced output format enable. • When IL_OUTPUT=1, enables interlaced output. • When IL_OUTPUT=0, enables progressive output.
	1	0	DSP_SYNC	Program enable for output syncs. Normally set DSP_SYNC=1; fields {0x61... 6A} apply.
	0	1	DSP_ENA	Enable bit for the entire display unit. Display unit operation is started when a rising edge is detected on this bit, stopped on a falling edge.
0x61	5	0	—	Reserved.
	4	0	IL_601i	Frame rate adjust. • When IL_601i=0, set for a double frame rate. • When IL_601i=1, set for a single frame rate.
	3	0	DQ_POL_N	Pad DVQ polarity. • When DQ_POL_N=0, polarity is set for active high. • When DQ_POL_N=1, polarity is set for active low.
	2	0	OEQ_POL_N	Pad OEQ polarity. • When OEQ_POL_N=0, polarity is set for active high. • When OEQ_POL_N=1, polarity is set for active low.
	1	0	VSQ_POL_N	Pad VSQ polarity. • When VSQ_POL_N=0, polarity is set for active high. • When VSQ_POL_N=1, polarity is set for active low.
	0	0	HSQ_POL_N	Pad HSQ polarity. • When HSQ_POL_N=0, polarity is set for active high. • When HSQ_POL_N=1, polarity is set for active low.
0x62	7-0	40	HSP[7:0]	Horizontal sync pulse length in pixels. Valid only when DSP_SYNC (0x60:1)=1.

Table 5-23 Display Timing Register Details (continued)

Sub Address	Bits	Default	Name	Description
0x63	7-0	48	HBP[7:0]	Horizontal blanking pulse length in pixels. Valid only when DSP_SYNC (0x60:1)=1.
0x64	7-0	5A	HAP[7:0]	Horizontal active-video pulse length. Valid only when DSP_SYNC (0x60:1)=1 Enter ‘0’ for 0 pixels, ‘1’ for 8 pixels, ‘2’ for 16 pixels, etc.
0x65	7-0	5A	HLP[7:0]	Lower 8 bits of horizontal total line length in pixels. Valid only when DSP_SYNC (0x60:1)=1.
0x66	3-0	3	HLP[11:8]	Upper 4 bits of horizontal total line length in pixels. Valid only when DSP_SYNC (0x60:1)=1.
0x67	7-0	2	VSP[7:0]	Vertical sync pulse length in lines. Valid only when DSP_SYNC (0x60:1)=1.
0x68	7-0	1A	VBP[7:0]	Vertical blanking pulse length in lines. Valid only when DSP_SYNC (0x60:1)=1.
0x69	7-0	78	VAP[7:0]	Vertical active-video pulse length. Valid only when DSP_SYNC (0x60:1)=1. Enter ‘0’ for 0 lines, ‘1’ for 4 lines, ‘2’ for 8 lines, etc.
0x6A	7-0	0D	VLP[7:0]	Lower 8 bits of total vertical length in lines. Valid only when DSP_SYNC (0x60:1)=1.
0x6B	3-0	2	VLP[11:8]	Upper 4 bits of total vertical length in lines. Valid only when DSP_SYNC (0x60:1=1.
0x6C	7-0	1A	VBP_E[7:0]	Vertical blanking pulse length for even field of interlaced output. In lines. Valid only when DSP_SYNC (0x60:1)=1.

5.14 Deinterlace Control Registers

Table 5-24 lists the Deinterlace Control Registers.

Table 5-24 Deinterlace Control Registers

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x70	rw	0	regular_ motion	vof_glb_enab	vof_local_ enab	0	di_bypass	vert_interp	dsp_422_ conv

Table 5-25 provides detailed descriptions of the Deinterlace Control Registers.

Table 5-25 Deinterlace Control Register Details

Sub Address	Bits	Default	Name	Description
0x70	6	0	REGULAR_MOTION	Deinterlace motion source. • When REGULAR_MOTION=0, set for saw-tooth motion. • When REGULAR_MOTION=1, set for regular motion.
	5	1	VOF_GLB_ENAB	Video on film global detection enable.
	4	1	VOF_LOCAL_ENAB	Video on film local detection enable.
	3	0	—	Reserved. Write only a “0” to this bit position.
	2	1	DI_BYPASS	Deinterlace bypass. • When DI_BYPASS=0, • When DI_BYPASS=1, interlaced data is de-interlaced without vertical or angle interpolation or motion compensation.
	1	0	VERT_INTERP	Vertical linear interpolation enable. • When VERT_INTERP=0, use angle interpolation. • When VERT_INTERP=1, set for normal operation.
	0	1	DSP_422_CONV	Method for converting from 4:1:1 to 4:2:2 or from 4:2:2 to 4:4:4 formats in the display unit. • When DSP_422_CONV=0, simply copy the UV sample • When DSP_422_CONV=1, use interpolation.

5.15 Upscaling Registers

Table 5-26 lists the Upscaling Registers.

Table 5-26 Upscaling Registers

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x71	rw	0	0	0	us_siz	us_mode2	us_mode1	us_mod0	us_remap
0x72	rw	us_hlen7	us_hlen6	us_hlen5	us_hlen4	us_hlen3	us_hlen2	us_hlen1	us_hlen0
0x73	rw	us_vlen7	us_vlen6	us_vlen6	us_vlen4	us_vlen3	us_vlen2	us_vlen1	us_vlen0

Table 5-27 provides detailed descriptions of the Upscaling Registers.

Table 5-27 Upscaling Register Details

<table>
<tr><th>Sub Address</th><th>Bits</th><th>Default</th><th>Name</th><th>Description</th></tr>
<tr><td rowspan="3">0x71</td><td>4</td><td>0</td><td>US_SIZ</td><td>Output scaling region size enable.
• When US_SIZ=0, normal operation.
• When US_SIZ=1, the size is given by the US_HLEN (0x73) and US_VLEN (0x72) fields, regardless of the value of the US_REMAP (0x71:0) field.</td></tr>
<tr><td>3-1</td><td>0</td><td>US_MODE[2:0]</td><td>Output resolution mode. Valid only when US_REMAP (0x71:0)=1.
<table>
<tr><th>US_MODE</th><th>US_REMAP</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>No up-scaling.</td></tr>
<tr><td>0</td><td>1</td><td>Reserved.</td></tr>
<tr><td>1</td><td>X</td><td>Scaled the active display region using resolution US_HLEN and US_VLEN.</td></tr>
</table></td></tr>
<tr><td>0</td><td>0</td><td>US_REMAP</td><td>Program enable for the output resolution mode. Up-scaling enable.
• When US_REMAP=0, set for normal operation.
• When US_REMAP=1, allows the remapping of the output mode through the US_MODE (0x71:3-1) field.</td></tr>
<tr><td>0x72</td><td>7-0</td><td>59</td><td>US_HLEN[7:0]</td><td>Width of the output display device. Valid only when US_SIZ (0x71:4)=1.
Enter ‘0’ for 8, ‘1’ for 16, ‘2’ for 24 pixels, etc.</td></tr>
<tr><td>0x73</td><td>7-0</td><td>77</td><td>US_VLEN[7:0]</td><td>Height of the output display device. Valid only when US_SIZ (0x71:4)=1.
Enter ‘0’ for 4, ‘1’ for 8, ‘2’ for 12 rows, etc.</td></tr>
</table>

5.16 Video Overlay Registers

Table 5-28 lists the Video Overlay Registers.

Table 5-28 Video Overlay Registers

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x78	rw	blue_screen	y_blank	0	prim_cs	prim_cs	common_cs2	common_cs1	common_cs0
0x79	rw	y_blue7	y_blue6	y_blue5	y_blue4	y_blue3	y_blue2	y_blue1	y_blue0
0x7A	rw	u_blue7	u_blue6	u_blue5	u_blue4	u_blue3	u_blue2	u_blue1	u_blue0
0x7B	rw	v_blue7	v_blue6	v_blue5	v_blue4	v_blue3	v_blue2	v_blue1	v_blue0

Table 5-29 provides detailed descriptions of the Video Overlay Registers.

Table 5-29 Video Overlay Register Details

<table>
<tr><th>Sub Address</th><th>Bits</th><th>Default</th><th>Name</th><th>Description</th></tr>
<tr><td rowspan="5">0x78</td><td>7</td><td>1</td><td>BLUE_SCREEN</td><td>Blue screen enable. Active high.</td></tr>
<tr><td>6</td><td>0</td><td>Y_BLANK</td><td>Blanking value for Y when fixing the blanking values for YUV. Enter ‘0’ for 64 or ‘1’ for 0.</td></tr>
<tr><td>5</td><td>—</td><td>—</td><td>Reserved.</td></tr>
<tr><td>4-3</td><td>0</td><td>PRIM_CS[1:0]</td><td>Color space for input primary channel.
<table>
<tr><th>PRIM_CS</th><th>Description</th></tr>
<tr><td>00</td><td>ITU-R BT601 YCbCr (for SDTV)</td></tr>
<tr><td>01</td><td>ITU-R BT709 YCbCr (for HDTV)</td></tr>
<tr><td>10</td><td>RGB (for PC)</td></tr>
<tr><td>11</td><td>RGB (for TV)</td></tr>
</table></td></tr>
<tr><td>2-0</td><td>0</td><td>COMMON_CS[2:0]</td><td>Common output color space.
<table>
<tr><th>COMMON_CS</th><th>Description</th></tr>
<tr><td>000</td><td>ITU-R BT601 YCbCr (for SDTV)</td></tr>
<tr><td>001</td><td>Y-Cb-Cr</td></tr>
<tr><td>010</td><td>ITU-R BT709 YCbCr (for HDTV)</td></tr>
<tr><td>011</td><td>Reserved</td></tr>
<tr><td>100</td><td>RGB (for TV)</td></tr>
<tr><td>101</td><td>RGB (for PC)</td></tr>
<tr><td>110</td><td>Reserved</td></tr>
<tr><td>111</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>0x79</td><td>7-0</td><td>10</td><td>Y_BLUE[7:0]</td><td>Blue screen value of Y (G) component. Valid only when BLUE_SCREEN (0x78:6)=1.</td></tr>
<tr><td>0x7A</td><td>7-0</td><td>80</td><td>U_BLUE[7:0]</td><td>Blue screen value of U (B) component. Valid only when BLUE_SCREEN (0x78:6)=1.</td></tr>
<tr><td>0x7B</td><td>7-0</td><td>80</td><td>V_BLUE[7:0]</td><td>Blue screen value of V (R) component. Valid only when BLUE_SCREEN (0x78:6)=1.</td></tr>
</table>

5.17 Scan Velocity Modulation (SVM) Registers

Table 5-30 lists the Scan Velocity Modulation (SVM) Registers.

Table 5-30 Scan Velocity Modulation (SVM) Registers

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x80	rw	full_cyc_svm_clk	SVM_plrt	SVM_lpf	SVM_en	SVM_coring3	SVM_coring2	SVM_coring1	SVM_coring0
0x81	rw	SVM_diff2	SVM_diff1	SVM_diff0	SVM_dctrl	SVM_delay3	SVM_delay2	SVM_delay1	SVM_delay0
0x82	rw	SVM_gain5	SVM_gain4	SVM_gain3	SVM_gain2	SVM_gain1	SVM_gain0	SVM_ctrl1	SVM_ctrl0
0x83	rw	SVM_limit7	SVM_limit6	SVM_limit5	SVM_limit4	SVM_limit3	SVM_limit2	SVM_limit1	SVM_limit0

Table 5-31 provides detailed descriptions of the Scan Velocity Modulation (SVM) Registers.

Table 5-31 Scan Velocity Modulation (SVM) Register Details

Sub Address	Bits	Default	Name	Description
0x80	7	1	FULL_CYC_SVM_CLK	Full cycle SVM Clock. • When FULL_CYC_SVM_CLK=0, set delay in half clock cycle (2x display clock). • When FULL_CYC_SVM_CLK=1, set delay in one clock cycle
	6	0	SVM_PLRT	Polarity control.
	5	0	SVM_LPF	Low pass filter control. • When SVM_LPF=0, disable low pass filter control. • When SVM_LPF=1, enable low pass filter control.

	4	0	SVM_EN	Enable data active signal
				• When SVM_EN=0, bypass
				• When SVM_EN=1:
				  • If data active=high, bypass.
				  • If data active=low, disable SVM.

	3-0	0	SVM_CORING[3:0]	Coring value.
0x81	7-5	1	SVM_DIFF[2:0]	Differentiator steps. • First order range=1~6. • Second order range=1~3.
	4	0	SVM_DCTRL	Delay control. • When SVM_DCTRL=0, delay control [0...15]. • When SVM_DCTRL=1, delay control [-15...0].
	3-0	0	SVM_DELAY[3:0]	Delay range.
0x82	7-2	1	SVM_GAIN[5:0]	Gain control.
	1-0	1	SVM_CTRL[1:0]	Control transfer function
0x83	7-0	0	SVM_LIMIT[7:0]	Limiter.

5.18 2:2 Pull-Down (22pd) Control Registers

Table 5-32 lists the 2:2 Pull-Down (22pd) Control Registers.

Table 5-32 2:2 Pull-Down Control Registers

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x87	rw	0	gm_frame_based	22pd_gmdata_sel	22pd_film_phase	22pd_film_mode	22pd_film_ctl	0	0

Table 5-33 provides detailed descriptions of the 2:2 Pull-Down (22pd) Control Registers.

Table 5-33 2:2 Pull-Down Control Register Details

Sub Address	Bits	Default	Name	Description
0x87	6	0	GM_FRAME_BASED	Global Motion frame-based. • When GM_FRAME_BASED=0, global motion is line-based. • When GM_FRAME_BASED=1, global motion is frame-based.
	5	0	22PD_GMDATA_SEL	Global Motion data select. • When 22PD_GMDATA_SEL=0, use 3:2 pull-down global motion data. • When 22PD_GMDATA_SEL=1, use 2:2 pull-down global motion data Note: This bit has an effect on 3:2 pulldown.
	4	0	22PD_FILM_PHASE	Phase used in film mode merging when under external control. Valid only when FILM_CTL (0x87:2)=1.
	3	0	22PD_FILM_MODE	Enables film mode merging of fields instead of standard merging of fields when 2:2 pull-down film data is detected under internal control. Valid only when FILM_CTL (0x87:2)=0. • When 22PD_FILM_MODE=0, use standard merging. • When 22PD_FILM_MODE=1, use 2:2 pull-down film merging
	2	0	22PD_FILM_CTL	Film mode control. • When 22PD_FILM_CTL=0, use internal control; 22PD_FILM_MODE (0x87:3) applies. • When 22PD_FILM_CTL=0, use external control; 22PD_FILM_PHASE (0x87:4) applies.
	1-0	0	Reserved	Film mode sensitivity.

5.19 2:2 Pull-Down (22pd) Global Motion Detection Registers

Table 5-34 lists the 2:2 Pull-Down (22pd) Global Motion Detection Registers.

Table 5-34 2:2 Pull-Down Global Motion Detection Registers

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x88	rw	gmd22_left7	gmd22_left6	gmd22_left5	gmd22_left4	gmd22_left3	gmd22_left2	gmd22_left1	gmd22_left0
0x89	rw	gmd22_top7	gmd22_top6	gmd22_top5	gmd22_top4	gmd22_top3	gmd22_top2	gmd22_top1	gmd22_top0
0x8A	rw	gmd22_hlen7	gmd22_hlen6	gmd22_hlen5	gmd22_hlen4	gmd22_hlen3	gmd22_hlen2	gmd22_hlen1	gmd22_hlen0
0x8B	rw	gmd22_vlen7	gmd22_vlen6	gmd22_vlen5	gmd22_vlen4	gmd22_vlen3	gmd22_vlen2	gmd22_vlen1	gmd22_vlen0
0x8C	rw	vof_thr1_7	vof_thr1_6	vof_thr1_5	vof_thr1_4	vof_thr1_3	vof_thr1_2	vof_thr1_1	vof_thr1_0
0x8D	rw	vof_thr2_7	vof_thr2_6	vof_thr2_5	vof_thr2_4	vof_thr2_3	vof_thr2_2	vof_thr2_1	vof_thr2_0
0x8E	rw	vof_thrC7	vof_thrC6	vof_thrC5	vof_thrC4	vof_thrC3	vof_thrC2	vof_thrC1	vof_thrC0
0x8F	rw	vof_thrC15	vof_thrC14	vof_thrC13	vof_thrC12	vof_thrC11	vof_thrC10	vof_thrC9	vof_thrC8

Note:
1. The registers used to set the global motion detection region for 2:2 pulldown are:
   0x88–gmd22_left
   0x89–gmd22_top
   0x8a–gmd22_hlen
   0x8b–gmd22_vlen
2. Complete global motion register sets exist for both 2:2 and 3:2 motion. Both are read from registers 0xb4–0xbf and are switched using register 0x87 bit 5.

Table 5-35 provides detailed descriptions of the 2:2 Pull-Down (22pd) Global Motion Detection Registers.

Table 5-35 2:2 Pull-Down Global Motion Detection Register Details

Sub Address	Bits	Default	Name	Description
0x88	7-0	0	GMD22_LEFT[7:0]	Column coordinate for the top left corner of the global motion detection region. Enter ‘0’ for column 0, ‘1’ for column 8, ‘2’ for column 16, etc.
0x89	7-0	0	GMD22_TOP[7:0]	Row coordinate for the top left corner of the global motion detection region. Enter ‘0’ for row 0, ‘1’ for row 4, ‘2’ for row 8, etc.
0x8A	7-0	5A	GMD22_HLEN[7:0]	Number of pixels horizontally in the global motion detection region. Enter ‘0’ for 8, ‘1’ for 16, ‘2’ for 24 pixels, etc.
0x8B	7-0	32	GMD22_VLEN[7:0]	Number of lines vertically in the global motion detection region. Enter ‘0’ for 4, ‘1’ for 8, ‘2’ for 12 lines, etc.
0x8C	7:0	A0	VOF_THR1[7:0]	Video-on-Film threshold 1.
0x8E	7-0	64	VOF_THR2[7:0]	Video-on-Film threshold 2.
0x8E	7-0	0	VOF_THRC[7:0]	Low byte of Video-on-Film threshold C.
0x8F	7-0	1	VOF_THRC[15:8]	High byte of Video-on-Film threshold C.

5.20 Two-Wire Slave Registers

Table 5-36 lists the Two-Wire Slave Registers.

Table 5-36 Two-Wire Slave Registers

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x90	r or rw	device_ address5	device_ address4	device_ address3	device_ address2	device_ address1	device_ address0	word_address 8	rwN
0x91	ro	word_address 7	word_address 6	word_address 5	word_address 4	word_address 3	word_address 2	word_address 1	word_address 0
0x92	rw	bta7	bta6	bta5	bta4	bta3	bta2	bta1	bta0
0x93	rw	0	0	0	0	0	0	2W_filter	bta8

Table 5-37 provides detailed descriptions of the Two-Wire Slave Registers.

Table 5-37 Two-Wire Slave Register Details

Sub Address	Bits	Default	Name	Description
0x90	7-4	6	DEVICE_ADDRESS [5:2]	Base device address.
	3-2	0	DEVICE_ADDRESS [1:0]	Configurable lower 2 bits of the base device address. Bit 3 is determined by pin *2W_a2* and bit 2 by *2W_a1*. Read only.
	1	0	WORD_ADDRESS[8]	Upper bit of word address of the next byte access. In conjunction with the lower 8 bits (0x91:7-0), automatically increments after each access. Read only.
	0	1	2W_RWN	2-Wire read-write N Bit. Writing to it has no effect. Always returns ‘1’ on a read.
0x91	7-0	0	WORD_ADDRESS [7:0]	Lower 8 bits of word address of the next byte access. In conjunction with the upper 3 bits (0x90:3-1), automatically increments after each access. Read only.
0x92	7-0	24	BTA[7:0]	Lower 8 bits of bus turn around time. Enter ‘0’ for 1 cycle, ‘1’ for 2 cycles, etc. Reset value is correct for 100 kb/s 2-Wire operation.
0x93	1	1	2W_FILTER	Enables one-clock buffering of incoming 2-Wire signals to filter out noise.
	0	0	BTA[8]	Upper bit of bus turnaround time.

5.21 Direct SDRAM Access Registers

Table 5-38 lists the Direct SDRAM Access Registers.

Table 5-38 Direct SDRAM Access Registers

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x94	rw	ram_addr7	ram_addr6	ram_addr5	ram_addr4	ram_addr3	ram_addr2	ram_addr1	ram_addr0
0x95	rw	ram_addr15	ram_addr14	ram_addr13	ram_addr12	ram_addr11	ram_addr10	ram_addr9	ram_addr8
0x96	rw	ram_addr23	ram_addr22	ram_addr21	ram_addr20	ram_addr19	ram_addr18	ram_addr17	ram_addr16
0x97	rw	ram_dat7	ram_dat6	ram_dat5	ram_dat4	ram_dat3	ram_dat2	ram_dat1	ram_dat0

Table 5-39 provides detailed descriptions of the Direct SDRAM Access Registers.

Table 5-39 Direct SDRAM Access Register Details

Sub Address	Bits	Default	Name	Description
0x94	7-0	0	RAM_ADDR[7:0]	Least significant 8 bits of the SDRAM address.
0x95	7-0	0	RAM_ADDR[15:8]	Second-order 8 bits of the SDRAM address.
0x96	6-0	0	RAM_ADDR[22:16]	Most significant 7 bits of the SDRAM address.
0x97	7-0	0	RAM_DAT	Data to or from the SDRAM. The value of RAM_ADDR is incremented at the conclusion of a write or read at this address. • When written, writes the value RAM_DAT to the location RAM_ADDR (0x94 – 0x96). • When read, returns the value stored at the same location.

5.22 Video Enhance Registers

Table 5-40 lists the Video Enhance Registers.

Table 5-40 Video Enhance Registers

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xD0	rw	0	0	0	khpw4	khpw3	khpw2	khpw1	khpw0
0xD1	rw	0	0	0	kbpw4	kbpw3	kbpw2	kbpw1	kbpw0
0xD2	rw	0	0	0	0	0	klp2	klp1	klp0
0xD3	rw	0	0	peak_coring5	peak_coring4	peak_coring3	peak_coring2	peak_coring1	peak_coring0
0xD4	rw	dlti_coring4	dlti_coring3	dlti_coring2	dlti_coring1	dlti_coring0	dlti_gain2	dlti_gain1	dlti_gain0
0xD5	rw	dcti_coring3	dcti_coring2	dcti_coring1	dcti_coring0	dcti_slow	dcti_gain2	dcti_gain1	dcti_gain0
0xD6	rw	0	06	contrast5	contrast4	contrast3	contrast2	contrast1	contrast0
0xD7	rw	brightness7	brightness	brightness5	brightness4	brightness3	brightness2	brightness1	brightness0
0xD8	rw	hue7	hue6	hue5	hue4	hue3	hue2	hue1	hue0
0xD9	rw	saturation7	saturation6	saturation5	saturation4	saturation3	saturation2	saturation1	saturation0
0xDA	ro	hue_sin7	hue_sin6	hue_sin5	hue_sin4	hue_sin3	hue_sin2	hue_sin1	hue_sin0
0xDB	ro	0	0	0	0	0	0	hue_sin9	hue_sin8
0xDC	ro	hue_cos7	hue_cos6	hue_cos5	hue_cos4	hue_cos3	hue_cos2	hue_cos1	hue_cos0
0xDD	ro	0	0	0	0	0	0	hue_cos9	hue_cos8
0xDE	rw	0	0	0	ble_gain4	ble_gain3	ble_gain2	ble_gain1	ble_gain0
0xDF	rw	ble_thr7	ble_thr6	ble_thr5	ble_thr4	ble_thr3	ble_thr2	ble_thr1	ble_thr0

Table 5-41 provides detailed descriptions of the Video Enhance Registers.

Table 5-41 Video Enhance Register Details

Sub Address	Bits	Default	Name	Description
0xD0	4-0	2	KHPW[4:0]	High-pass peaking filter weighting.
0xD1	4-0	2	KBPW[4:0]	Band-pass peaking filter weighting.
0xD2	2-0	1	KLP[2:0]	Low-pass peaking filter gain.
0xD3	5-0	8	PEAK_CORING[5:0]	Coring threshold for peaking. Enter ‘0’ for 0, ‘1’ for 1, ‘2’ for 2, etc.
0xD4	7-3	8	DLTI_CORING[4:0]	Coring threshold for DLTI. Enter ‘0’ for 0, ‘1’ for 1, ‘2’ for 2, etc.
	2-0	0	DLTI_GAIN[2:0]	Gain for DLTI.
0xD5	7-4	8	DCTI_CORING[3:0]	Coring threshold for DCTI. Enter ‘0’ for 0, ‘1’ for 2, ‘2’ for 4, etc.
	3	0	DCTI_SLOW	Bandwidth mode of DCTI. Enter ‘0’ for high-bandwidth or ‘1’ for low-bandwidth.
	2-0	0	DCTI_GAIN[2:0]	Gain for DCTI.
0xD6	5-0	20	CONTRAST[5:0]	Contrast adjustment.
0xD7	7-0	0	BRIGHTNESS[7:0]	Brightness adjustment, in signed notation. Note that ‘7f’ corresponds to +127, ‘80’ to –128, ‘81’ to –127, etc.
0xD8	7-0	0	HUE[7:0]	Hue adjustment.
0xD9	7-0	40	SATURATION[7:0]	Saturation adjustment.
0xDA	7-0	0	HUE_SIN[7:0]	Lower 8 bits of sin θ as used in the hue calculation, where sin θ is a signed integer –256.. .256. Read only.

Table 5-41 Video Enhance Register Details (continued)

Sub Address	Bits	Default	Name	Description
0xDB	1-0	0	HUE_SIN[9:8]	Upper 2 bits of sin θ. Read only.
0xDC	7-0	0	HUE_COS[7:0]	Lower 8 bits of cos θ as used in the hue calculation, where cos θ is a signed integer –256 ... 256. Read only.
0xDD	1-0	0	HUE_COS[9:8]	Upper 2 bits of cos θ. Read only.
0xDE	4-0	0	BLE_GAIN[4:0]	Gain for black level expansion.
0xDF	7-0	0	BLE_THR [7:0]	Threshold for black level expansion. Maximum Y value for consideration for black level expansion.

5.23 CMGS Registers

Table 5-42 lists the CMGS Registers.

Table 5-42 CMGS Registers

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xE0	rw	0	0	0	0	0	cgms_prog	cgms_standard	cgms_ena
0xE1	rw	cgms_hsta7	cgms_hsta6	cgms_hsta5	cgms_hsta4	cgms_hsta3	cgms_hsta2	cgms_hsta1	cgms_hsta0
0xE2	rw	0	0	cgms_vsta5	cgms_vsta4	cgms_vsta3	cgms_vsta2	cgms_vsta1	cgms_vsta0
0xE3	rw	0	0	cgms_width5	cgms_width4	cgms_width3	cgms_width2	cgms_width1	cgms_width0
0xE4	rw	cgms_high7	cgms_high6	cgms_high5	cgms_high4	cgms_high3	cgms_high2	cgms_high1	cgms_high0
0xE5	rw	cgms_low7	cgms_low6	cgms_low5	cgms_low4	cgms_low3	cgms_low2	cgms_low1	cgms_low0
0xE6	rw	0	0	0	0	cgms_ref3	cgms_ref2	cgms_ref1	cgms_ref0
0xE7	rw	cgms_dat1_7	cgms_dat1_6	cgms_dat1_5	cgms_dat1_4	cgms_dat1_3	cgms_dat1_2	cgms_dat1_1	cgms_dat1_0
0xE8	rw	cgms_dat2_7	cgms_dat2_6	cgms_dat2_5	cgms_dat2_4	cgms_dat2_3	cgms_dat2_2	cgms_dat2_1	cgms_dat2_0
0xE9	rw	cgms_dat3_7	cgms_dat3_6	cgms_dat3_5	cgms_dat3_4	cgms_dat3_3	cgms_dat3_2	cgms_dat3_1	cgms_dat3_0
0xEA	rw	0	0	0	0	0	0	p525_ena	macro_ena

Table 5-43 provides detailed descriptions of the CMGS Registers.

Table 5-43 CMGS Register Details

Sub Address	Bits	Default	Name	Description
0xE0	2	0	CGMS_PROG	Program enable for CGMS start, width, high level, and low level values (0xE1-4). Otherwise, the values are given in TBD according to the CGMS_STANDARD (0xE0:1).
	1	0	CGMS_STANDARD	CGMS Standard. • When CGMS_STANDARD=0, use for EIA-805. • When CGMS_STANDARD=1, use EIAJ-CPR 1204.
	0	0	CGMS_ENA	CGMS Enable.
0xE1	7-0	7B	CGMS_HSTA[7:0]	Starting pixel number from the edge of horizontal sync to the first reference bit. Valid only when CGMS_PROG (0xE0:2)=‘1’. Enter ‘0’ for 0, ‘1’ for 1, ‘2’ for 2 pixels, etc.
0xE2	5-0	29	CGMS_VSTA[5:0]	CGMS line number, counted from the edge of vertical sync edge. Valid only when CGMS_PROG (0xE0:2)=‘1’. Enter ‘0’ for 0, ‘1’ for 1, ‘2’ for 2 lines, etc.
0xE3	5-0	10	CGMS_WIDTH[5:0]	The width of a CGMS reference or data bit in pixels. Valid only when CGMS_PROG (0xE0:2)=‘1’. Enter ‘0’ for 0, ‘1’ for 1, ‘2’ for 2 pixels, etc.
0xE4	7-0	C8	CGMS_HIGH[7:0]	High level of CGMS reference and data bits. In increments of 1/256 of full range. Valid only when CGMS_PROG (0xE0:2)=‘1’.
0xE5	7-0	3C	CGMS_LOW[7:0]	Low level of CGMS reference and data bits. In increments of 1/256 of full range. Valid only when CGMS_PROG (0xE0:2)=‘1’.
0xE6	3-0	0xA	CGMS_REF[3:0]	CGMS Reference value. Only cgms_ref[3:0] are valid when CGMS_STANDARD (0xE0:1)=‘1’.
0xE7	7-0	0x0	CGMS_DAT1[7:0]	CGMS Data byte 1.
0xE8	7-0	0x0	CGMS_DAT2[7:0]	CGMS Data byte 2.
0xE9	7-0	0x0	CGMS_DAT3[7:0]	CGMS Data byte 3. Only cgms_ref[3:0] are valid when CGMS_STANDARD (0xE0:1)=‘1’.

Table 5-43 CMGS Register Details (continued)

Sub Address	Bits	Default	Name	Description
0xEA	1	0	P525_ENA	P525 Processing enable. • When P525_ENA=0, bypass P525 processing. • When P525_ENA=1, enable sync embedding and optional CGMS and Macrovision copy protection.
	0	0	MACRO_ENA	Macrovision enable.

5.24 Back End Registers

Table 5-44 lists the Back End Registers.

Table 5-44 Back End Registers

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xF0	rw	0	0	0	dac2x	svmq_down	yq_down	uq_down	vq_down
0xF1	rw	0	0	0	0	0	rgb_swap2	rgb_swap1	rgb_swap0
0xF3	rw	valid_src1	valid_src0	V_delay1	V_delay0	U_delay1	U_delay0	Y_delay1	Y_delay0
0xF4	rw	0	0	0	0	0	0	0	0

Table 5-45 provides detailed descriptions of the Analog Back End Registers.

Table 5-45 Back End Register Details

Sub Address	Bits	Default	Name	Description
0xF0	4	0	DAC2X	Double-speed DAC enable. • When DAC2X=0, set for normal operation. • When DAC2X=1, run the DAC at twice the display clock speed.
	3	0	SVMQ_DOWN	Power down for SVM channel. Active high.
	2	0	YQ_DOWN	Power down for Y channel. Active high.
	1	0	UQ_DOWN	Power down for U channel. Active high.
	0	0	VQ_DOWN	Power down for V channel. Active high.
0xF1	2-0	0	RGB_SWAP[2:0]	Color swap.

RGB_SWAP	Description
000	Y=Y, U=U, V=V
001	Y=U, U=V, V=Y
010	Y=V, U=Y, V=U
011	Y=Y, U=V, V=U
101	Y=Y, U=U, V=Y
110	Y=U, U=Y, V=V

Table 5-45 Back End Register Details (continued)

<table>
<tr><th>Sub Address</th><th>Bits</th><th>Default</th><th>Name</th><th>Description</th></tr>
<tr><td rowspan="4">0xF3</td><td>7-6</td><td>0</td><td>VALID_SRC[1:0]</td><td>Channel source for data valid.<table><tr><th>valid_src</th><th>Description</th></tr><tr><td>00</td><td>Y</td></tr><tr><td>01</td><td>U</td></tr><tr><td>10</td><td>V</td></tr></table></td></tr>
<tr><td>5-4</td><td>0</td><td>V_DELAY[1:0]</td><td>Delay Y output by 0-3 clock cycles.</td></tr>
<tr><td>3-2</td><td>0</td><td>U_DELAY[1:0]</td><td>Delay U output by 0-3 clock cycles.</td></tr>
<tr><td>1-0</td><td>0</td><td>Y_DELAY[1:0]</td><td>Delay V output by 0-3 clock cycles.</td></tr>
<tr><td>0xF4</td><td>7-0</td><td>0</td><td>—</td><td>Reserved.</td></tr>
</table>

6

Packaging

This chapter describes packaging used for the PW1225 Video SignalProcessor.

6.1 Package

The PW1225 SignalProcessor is packaged in a 160-pin PQFP package, shown in Figure 6-1.

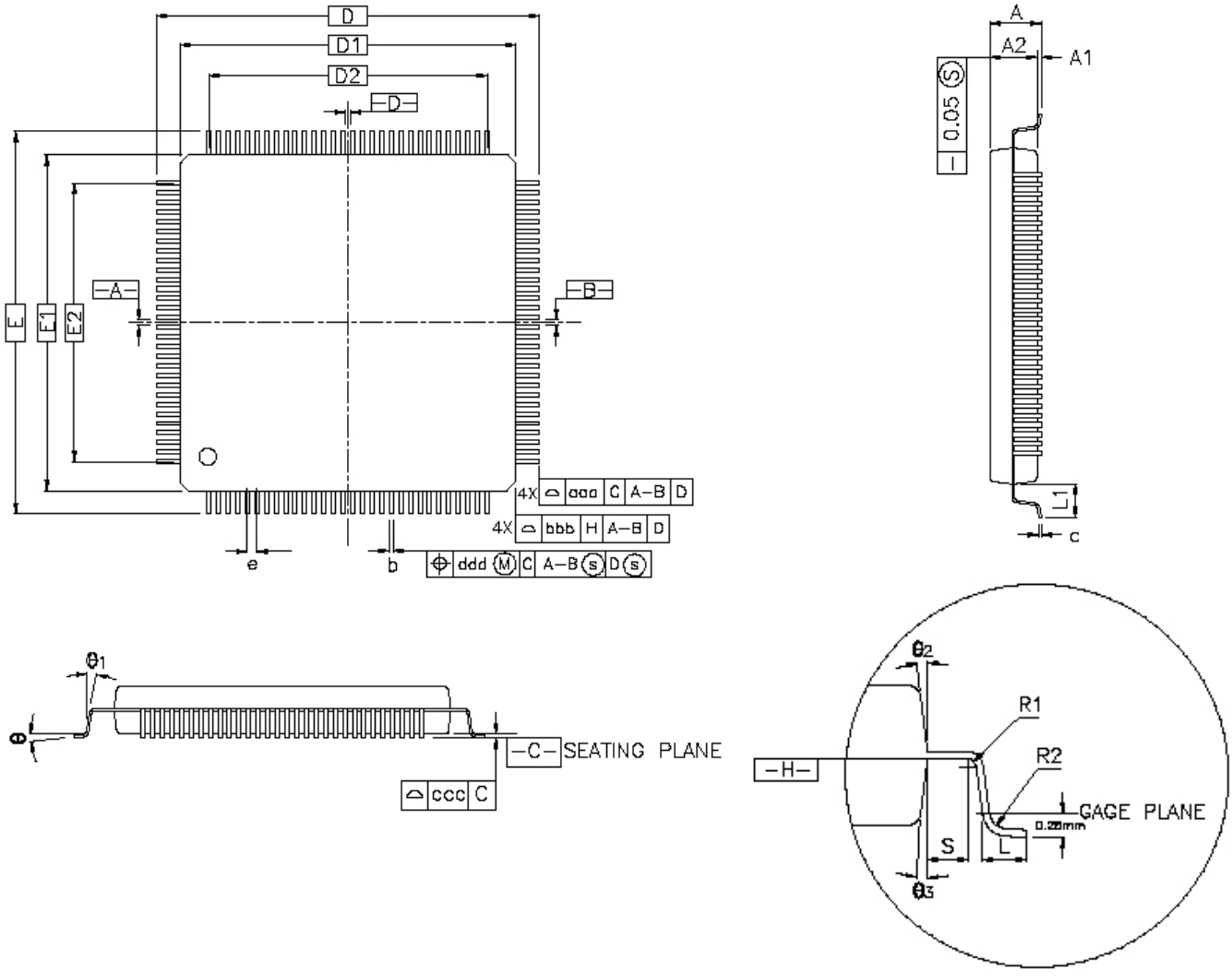


Figure 6-1 Package Diagram

6.2 Physical Dimensions

The controlling dimensions for the package are listed in Table 6-1:

Table 6-1 Controlling Dimensions

Symbol	Millimeter			Inch		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	—	—	4.07	—	—	0.160
A1	0.15	0.25	0.35	0.006	0.010	0.014
A2	3.17	3.32	3.67	0.125	0.131	0.144
D	31.90 Basic			1.256 Basic		
D1	28.00 Basic			1.102 Basic		
D2	25.35			0.998		
E	31.90 Basic			1.256 Basic		
E1	28.00 Basic			1.102 Basic		
E2	25.35			0.998		
R1	0.13	—	—	0.005	—	—
R2	0.13	—	0.30	0.005	—	0.012
Θ	0^o	3.5^o	7^o	0^o	3.5^o	7^o
Θ_1	0^o	—	—	0^o	—	—
Θ_2	8^o Ref			8^o Ref		
Θ_3	8^o Ref			8^o Ref		
b	0.22	0.30	0.38	0.009	0.012	0.015
c	0.11	0.15	0.23	0.004	0.006	0.009
e	0.65 Basic			0.26 Basic		
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.95 Ref			0.077 Ref		
S	0.40	—	—	0.016	—	—
Tolerances of Form and Position						
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	0.10			0.004		
ddd	0.12			0.005		

Notes:
1. Dimensions of D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 do not include mold mismatch and are determined at datum plane –H–.
2. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located on the lower radius or the lead foot.

6.3 Thermal Resistance

Table 6-2 lists thermal resistance of the package as measured on a JEDEC standard board (4L):

Table 6-2 Thermal Resistance

Θ_{JA}			Ψ_{JT}	Θ_{JC}
0 m/s	1 m/s	2 m/s	(C/W)	(C/W)
36.4	34.0	32.4	2.8	18.2