OpenSPARC Glossary 11/29/05

This chapter defines concepts and terminology common to all implementations of UltraSPARC Architecture.

aliased Said of each of two virtual addresses that refer to the same underlying memory location.

address space identifier (ASI) An 8-bit value that identifies an address space. For each instruction or data access, the integer unit appends an ASI to the address. *See also* **implicit ASI**.

application program A program executed with the virtual processor in nonprivileged mode. **Note:** Statements made in this specification regarding application programs may not be applicable to programs (for example, debuggers) that have access to privileged virtual processor state (for example, as stored in a memory-image dump).

ASI Address space identifier.

ASR Ancillary State register.

available (virtual processor) A virtual processor that is physically present and functional, that can be enabled and used.

big-endian An addressing convention. Within a multiple-byte integer, the byte with the smallest address is the most significant; a byte's significance decreases as its address increases.

BLD "Legacy" abbreviation for block load (now LDBLOCKF).

BST "Legacy" abbreviation for block store (now STBLOCKF).

bypass ASI An ASI that refers to memory space and for which the MMU does not perform address translation (that is, memory is accessed using a direct physical address).

byte Eight consecutive bits of data, aligned on an 8-bit boundary.

clean window A register window in which all of the registers contain 0, a valid address from the current address space, or valid data from the current address space.

CMP Chip-level multiprocessor. A processor cluster containing more than one processor core.

coherence A set of protocols guaranteeing that all memory accesses are globally visible to all caches on a shared-memory bus.

completed (memory operation) Said of a memory transaction when an idealized memory has executed the transaction with respect to all processors. A load is considered completed when no subsequent memory transaction can affect the value returned by the load. A store is considered completed when no subsequent load can return the value that was overwritten by the store.

consistency *See* **coherence**.

context A set of translations that supports a particular address space. *See also* **Memory Management Unit (MMU)**.

copyback The process of copying back a dirty ("owned") cache line present in the cache, in response to snoop request from another processor.

CPI Cycles per instruction. The number of clock cycles it takes to execute an instruction.

core In a UltraSPARC Architecture processor, the term core may be used to refer to either a virtual processor or a physical processor core.

cross-call An interprocessor call in a multiprocessor system.

CTI Abbreviation for **control-transfer instruction**.

current window The block of 24 R registers that is currently in use. The Current Window Pointer (CWP) register points to the current window.

data access (instruction) A load, store, load-store, or FLUSH instruction.

DCTI Delayed control transfer instruction.

demap To invalidate a mapping in the MMU.

denormalized number A nonzero floating-point number, the exponent of which has a value of zero. A more complete definition is provided in IEEE Standard 754-1985.

deprecated The term applied to an architectural feature (such as an instruction or register) for which a UltraSPARC Architecture implementation provides support *only* for compatibility with previous versions of the architecture. Use of a deprecated feature must generate correct results but may compromise software performance.

Deprecated features should not be used in new UltraSPARC Architecture software and may not be supported in future versions of the architecture.

disable (core) The process of removing a virtual processor from operation, which will normally complete during the next system or power-on reset.

disabled (core) A virtual processor that is out of operation (not executing instructions and not participating in cache coherency).

dispatch To send a previously fetched instruction to one or more functional units for execution. Typically, the instruction is dispatched from a reservation station or other buffer of instructions waiting to be executed. (Other conventions for this term exist, but the this specification attempts to use *dispatch* consistently as defined here. *See also* **issued**.

doublet Two bytes (16 bits) of data.

doubleword An 8-byte datum. **Note:** The definition of this term is architecture dependent and may differ from that used in other processor architectures.

enable (core) The process of preparing a virtual processor for operation, which will normally complete at the next system or power-on reset.

enabled (core) A virtual processor that is in operation (participating in cache coherency, but not executing instructions unless it is also running). *See also* **disabled** *and* **running**.

even parity The mode of parity checking in which each combination of data bits plus a parity bit contains an even number of '1' bits.

exception A condition that makes it impossible for the processor to continue executing the current instruction stream. Some exceptions (for example, floating-point exceptions; see FSR.tem) may be masked (that is, trap generation disabled) so that the decision on whether or not to apply special processing can be deferred and made by software at a later time. *See also* **trap**.

explicit ASI An ASI that that is provided by a load, store, or load-store alternate instruction (either from its imm_asi field or from the ASI register).

extended word An 8-byte datum, nominally containing integer data. **Note:** The definition of this term is architecture dependent and may differ from that used in other processor architectures.

fcc*n* One of the floating-point condition code fields fcc0, fcc1, fcc2, or fcc3.

fiber Refers to an execution pipeline. It is a loose term for the basic collection of hardware needed to execute instructions. A fiber may be used by one or more strands to execute instructions from one or more threads. *See also* **physical core**, **processor**, **strand**, **thread**, *and* **virtual processor**.

floating-point exception An exception that occurs during the execution of a floating-point operate (FPop) instruction. The exceptions are *unfinished_FPop*, *unimplemented_FPop*, *sequence_error*, *hardware_error*, *invalid_fp_register*, or *IEEE_754_exception*.

F register A floating-point register. SPARC V9 includes single-, double-, and quad-precision F registers.

IEEE 754 IEEE Standard 754-1985, the IEEE Standard for Binary Floating-Point Arithmetic.

IEEE-754 exception A floating-point exception, as specified by IEEE Std 754-1985. Listed within this specification as IEEE_754_exception.

floating-point operate (FPop) instructions Instructions that perform floating-point calculations, as defined in *Floating-Point Operate (FPop) Instructions* on page 144. FPop instructions do not include FBfcc instructions, loads and stores between memory and the F registers, or non-floating-point operations that read or write F registers.

floating-point trap type The specific type of a floating-point exception, encoded in the FSR.ftt field.

floating-point unit A processing unit that contains the floating-point registers and performs floating-point operations, as defined by this specification.

FPop *See* floating-point operate (FPop) instructions.

FPRS Floating-Point Register State register.

FSR Floating-Point Status register.

GL Global Level register.

GSR General Status register.

FPU Floating-point unit.

halfword A 2-byte datum. **Note:** The definition of this term is architecture dependent and may differ from that used in other processor architectures.

hyperprivileged (software) Software executing while the processor is in hyperprivileged state.

hyperprivileged (state) The highest processor privilege state (defined by HPSTATE.hpriv = 1), in which all processor features are accessible.

hypervisor (software) A layer of software that executes in hyperprivileged processor state. One purpose of hypervisor software (also referred to as "the hypervisor") is to provide greater isolation between operating system ("supervisor") software and the underlying processor implementation.

implementation Hardware or software that conforms to all of the specifications of an instruction set architecture (ISA).

implementation dependent An aspect of the UltraSPARC Architecture architecture that can legitimately vary among implementations. In many cases, the permitted range of variation is specified. When a range is specified, compliant implementations must not deviate from that range.

implicit ASI An address space identifier that is implicitly supplied by the virtual processor on all instruction accesses and on data accesses that do not explicitly provide an ASI value (from either an imm_asi instruction field or the ASI register).

informative appendix An appendix containing information that is useful but not required to create an implementation that conforms to the UltraSPARC Architecture specification. *See also* **normative appendix**.

initiated *Synonym*: **issued**.

instruction field A bit field within an instruction word.

instruction group One or more independent instructions that can be dispatched for simultaneous execution.

instruction set architecture A set that defines instructions, registers, instruction and data memory, the effect of executed instructions on the registers and memory, and an algorithm for controlling instruction execution. Does not define clock cycle times, cycles per instruction, data paths, etc. This specification defines the UltraSPARC Architecture instruction set architecture.

integer unit A processing unit that performs integer and control-flow operations and contains general-purpose integer registers and virtual processor state registers, as defined by this specification.

interrupt request A request for service presented to a virtual processor by an external device.

inter-strand Describes an operation that crosses virtual processor (strand) boundaries.

intra-strand Describes an operation that occurs entirely within one virtual processor (strand).

invalid (ASI or address) Undefined, reserved, or illegal.

ISA Instruction set architecture.

issued (1) A memory transaction (load, store, or atomic load-store) is said to be "issued" when a virtual processor has sent the transaction to the memory subsystem and the completion of the request is out of the virtual processor's control.
Synonym: **initiated**.

(2) An instruction (or sequence of instructions) is said to be *issued* when released from the virtual processor's instruction fetch unit. Typically, instructions are issued to a reservation station or other buffer of instructions waiting to be executed. (Other conventions for this term exist, but this specification attempts to use "issued" consistently as defined here.)
See also **dispatched**.

IU Integer Unit.

little-endian An addressing convention. Within a multiple-byte integer, the byte with the smallest address is the least significant; a byte's significance increases as its address increases.

load An instruction that reads (but does not write) memory or reads (but does not write) location(s) in an alternate address space. Some examples of *Load* includes loads into integer or floating-point registers, block loads, and alternate address space variants of those instructions. *See also* **load-store** *and* **store**, the definitions of which are mutually exclusive with *load*.

load-store An instruction that explicitly both reads and writes memory or explicitly reads and writes location(s) in an alternate address space. *Load-store* includes instructions such as CASA, CASXA, LDSTUB, and the deprecated SWAP instruction. *See also* **load** *and* **store**, the definitions of which are mutually exclusive with *load-store*.

may A keyword indicating flexibility of choice with no implied preference. **Note:** "May" indicates that an action or operation is allowed; "can" indicates that it is possible.

Memory Management Unit (MMU) The address translation hardware in a UltraSPARC Architecture implementation that translates 64-bit virtual address into physical addresses. The MMU is composed of the TLBs, ASRs, and ASI registers used to manage address translation. *See also* **context**, **physical address**, *and* **virtual address**.

multiprocessor system A system containing more than one virtual processor, which share some resources (notably, memory).

must *Synonym*: **shall**.

next program counter (NPC) A register that contains the address of the instruction to be executed next if a trap does not occur.

NFO Nonfault access only.

nonfaulting load A load operation that behaves identically to a normal load operation, except when supplied an invalid effective address by software. In that case, a regular load triggers an exception whereas a nonfaulting load appears to ignore the exception and loads its destination register with a value of zero (on a UltraSPARC Architecture processor, hardware treats regular and nonfaulting loads identically; the distinction is made in trap handler software). *Contrast with* **speculative load**.

nonprivileged An adjective that describes
(1) the state of the virtual processor when PSTATE.priv = 0, that is, nonprivileged mode;
(2) virtual processor state information that is accessible to software while the virtual processor is in either privileged mode or nonprivileged mode; for example, nonprivileged registers, nonprivileged ASRs, or, in general, nonprivileged state;
(3) an instruction that can be executed when the virtual processor is in either privileged mode or nonprivileged mode.

nonprivileged mode The mode in which a virtual processor is operating when executing application software (at the lowest privilege level). Nonprivileged mode is defined by PSTATE.priv = 0 and HSTATE.hpriv = 0. *See also* **privileged**.

normative appendix An appendix containing specifications that must be met by an implementation conforming to the this specification. *See also* **informative appendix**.

nontranslating ASI An ASI that does not refer to memory (for example, refers to control/status register(s)) and for which the MMU does not perform address translation.

normal trap A trap processed in `execute_state` (or equivalently, a non-`RED_state` trap). *Contrast with* **`RED_state` trap**.

NPC Next program counter.

npt Nonprivileged trap.

NUMA Nonuniform memory access.

N_REG_WINDOWS The number of register windows present in a particular implementation.

octlet Eight bytes (64 bits) of data. Not to be confused with "octet," which has been commonly used to describe eight bits of data. In this document, the term *byte*, rather than octet, is used to describe eight bits of data.

odd parity The mode of parity checking in which each combination of data bits plus a parity bit together contain an odd number of '1' bits.

opcode A bit pattern that identifies a particular instruction.

optional A feature not required for UltraSPARC Architecture compliance.

PA Physical address.

park The process of suspending a virtual processor from operation. There may be a delay until the virtual processor is parked, but no heavyweight operation (such as a reset) is required to complete the parking process.

parked A virtual processor suspended from operation. When parked, a virtual processor does not issue instructions for execution but (if enabled) still maintains cache coherency. *See also* **disabled, enabled,** and **running**.

PC Program counter.

PCR Performance Control register.

physical address An address that maps real physical memory or I/O device space. See also **virtual address**.

physical core The term *physical processor core*, or just *physical core*, is similar to the term *fiber* but represents a broader collection of hardware. A physical core includes an execution pipeline (fiber) plus associated structures, such as caches, that are required for performing the execution of instructions from one or more software threads. A physical core contains one or more virtual processors (strands). The physical core provides the necessary resources for the threads on each strand to make forward progress at a reasonable rate. A multistranded physical core can execute multiple software threads either by time multiplexing or partitioning resources (or any combination thereof). *See also* **fiber**, **processor**, **strand**, **thread**, *and* **virtual processor**.

PIC Performance Instrumentation Counter.

PIL Processor Interrupt Level register.

PIPT Physically indexed, physically tagged (cache).

POR Power-on reset.

prefetchable (1) An attribute of a memory location that indicates to an MMU that PREFETCH operations to that location may be applied.
(2) A memory location condition for which the system designer has determined that no undesirable effects will occur if a PREFETCH operation to that location is allowed to succeed. Typically, normal memory is prefetchable.

Nonprefetchable locations include those that, when read, change state or cause external events to occur. For example, some I/O devices are designed with registers that clear on read; others have registers that initiate operations when read. *See* **side effect**.

privileged An adjective that describes:
(1) the state of the processor when PSTATE.priv = 1 and HPSTATE.hpriv = 0, that is, *privileged mode*;
(2) processor state that is only accessible to software while the processor is in *privileged mode*; for example, privileged registers, privileged ASRs, or, in

general, privileged state;
(3) an instruction that can be executed only when the processor is in *privileged mode*.

privileged mode The mode in which a processor is operating when PSTATE.priv = 1 and HPSTATE.hpriv = 0. *See also* **nonprivileged**.

processor The unit on which a shared interface is provided to control the configuration and execution of a collection of strands. A processor contains one or more physical cores, each of which contains one or more strands. On a more physical side, a *processor* is a physical module that plugs into a system. A processor is expected to appear logically as a single agent on the system interconnect fabric. *Synonym:* **processor module**. *See also* **fiber**, **physical core**, **strand**, **thread**, *and* **virtual processor**.

processor core *See* **virtual processor**.

processor module *Synonym:* **processor**.

program counter (PC) A register that contains the address of the instruction currently being executed by the IU.

quadword A 16-byte datum. **Note:** The definition of this term is architecture dependent and may be different from that used in other processor architectures.

R register An integer register. Also called a general-purpose register or working register.

RA Real address.

RAS (1) Return Address Stack
(2) Reliability, Availability, and Serviceability

RAW Read After Write (hazard)

rd Rounding direction.

RDPR Read Privileged Register instruction.

recognized

RED_state Reset, Error, and Debug state. The virtual processor state when HPSTATE.red = 1. A restricted execution environment used to process resets and traps that occur when TL = *MAXTL* – 1.

RED_state trap A trap processed in RED_state. *Contrast with* **normal trap**.

reserved Describing an instruction field, certain bit combinations within an instruction field, or a register field that is reserved for definition by future versions of the architecture.

Reserved instruction fields must read as 0, unless the implementation supports extended instructions within the field. The behavior of a UltraSPARC Architecture 2005 virtual processor when it encounters a nonzero value in a reserved instruction field is as defined in *Reserved Opcodes and Instruction Fields* on page 145.

Reserved bit combinations within instruction fields are defined in Chapter 7, *Instructions*. In all cases, a UltraSPARC Architecture 2005 processor must decode and trap on these reserved combinations.

Reserved fields within registers should always be written by software with values of those fields previously read from that register or with zeroes; they should read as 0 in hardware. Software intended to run on future versions of UltraSPARC Architecture 2005 should not assume that these fields will read as 0 or any other particular value. Throughout this specification, figures and tables illustrating registers and instruction encodings indicate reserved fields and combinations with an em dash (—).

reset trap A vectored transfer of control to privileged software through a fixed-address reset trap table. Reset traps cause entry into `RED_state`.

restricted Describes an address space identifier (ASI) that may be accessed only while the virtual processor is operating in a privileged mode or hyperprivileged mode.

retired An instruction is said to be "retired" when one of (instruction) the following two events has occurred:
(1) A precise trap has been taken, with TPC containing the instruction's address (the instruction has not changed architectural state in this case).
(2) The instruction's execution has progressed to a point at which architectural state affected by the instruction has been updated such that all three of the following are true:

- The PC has advanced beyond the instruction.
- Except for deferred trap handlers, no consumer in the same instruction stream can see the old values and all consumers in the same instruction stream will see the new values.
- Stores are visible to all loads in the same instruction stream, including stores to noncacheable locations.

RMO Relaxed memory order.

rs1, rs2, rd The integer or floating-point register operands of an instruction. rs1 and rs2 are source registers; rd is the destination register.

RTO Read to Own (cache state).

RTS Read to Share (cache state).

running A state of a virtual processor in which it is in operation (maintaining cache coherency and issuing instructions for execution) and not parked.

service processor A device external to the processor that can examine and alter internal processor state. A service processor may be used to control/coordinate a multiprocessor system and aid in error recovery.

SFAR Synchronous Fault Address register.

SFSR Synchronous Fault Status register.

shall A keyword indicating a mandatory requirement. Designers must implement all such mandatory requirements to ensure interoperability with other UltraSPARC Architecture-compliant products. *Synonym:* **must**.

should A keyword indicating flexibility of choice with a strongly preferred implementation. *Synonym:* **it is recommended**.

side effect The result of a memory location having additional actions beyond the reading or writing of data. A side effect can occur when a memory operation on that location is allowed to succeed. Locations with side effects include those that, when accessed, change state or cause external events to occur. For example, some I/O devices contain registers that clear on read; others have registers that initiate operations when read. *See also* **prefetchable**.

SIMD Single Instruction/Multiple Data; a class of instructions that perform identical operations on multiple data contained (or "packed") in each source operand.

SIR Software-initiated reset.

snooping The process of maintaining coherency between caches in a shared-memory bus architecture. All cache controllers monitor (snoop) the bus to determine whether they have a copy of the shared cache block.

speculative load A load operation that is issued by a virtual processor speculatively, that is, before it is known whether the load will be executed in the flow of the program. Speculative accesses are used by hardware to speed program execution and are transparent to code. An implementation, through a combination of hardware and system software, must nullify speculative loads on memory locations that have side effects; otherwise, such accesses produce unpredictable results. *Contrast with* **nonfaulting load**.

store An instruction that writes (but does not explicitly read) memory or writes (but does not explicitly read) location(s) in an alternate address space. Some examples of *Store* includes stores from either integer or floating-point registers, block stores, Partial Store, and alternate address space variants of those instructions. *See also* **load** and **load-store**, the definitions of which are mutually exclusive with *store*.

strand Identifies the hardware state used to hold a software thread in order to execute it. *Strand* is specifically the software-visible architected state (program counter (PC), next program counter (NPC), general-purpose registers, floating-point registers, condition codes, status registers, ASRs, etc.) of a thread and any microarchitecture state required by hardware for its execution. *See also* **fiber**, **physical core**, **processor**, **thread**, *and* **virtual processor**.

subnormal number *Synonym:* **denormalized number**.

superscalar An implementation that allows several instructions to be issued, executed, and committed in one clock cycle.

supervisor software Software that executes when the virtual processor is in privileged mode.

suspend *See* **park**.

synchronization An operation that causes the processor to wait until the effects of all previous instructions are completely visible before any subsequent instructions are executed.

system A set of virtual processors that share a physical address space.

taken A control-transfer instruction (CTI) is *taken* when the CTI alters the control flow by writing a value into NPC other than the default value NPC = 4.

A trap is *taken* when the control flow changes in response to an exception, reset, Tcc instruction, or interrupt. An exception must be detected and recognized before it can cause a trap to be taken.

TBA Trap base address.

TEE Thread Execution Engine. *Synonym*: virtual processor.

thread A software entity that can be run on hardware. A thread is scheduled, may or may not be actively running on hardware at any given time, and may migrate around the hardware of a system. *See also* **fiber**, **physical core**, **processor**, **strand**, *and* **virtual processor**.

TLB *See* **Translation Lookaside Buffer (TLB).**

TLB hit The desired translation is present in the TLB.

TLB miss The desired translation is not present in the TLB.

TPC Trap-saved program counter.

Translation Lookaside Buffer (TLB) A cache within an MMU that contains recent partial translations. TLBs speed up closely following translations by often eliminating the need to reread Translation Table Entries from memory.

trap The action taken by a virtual processor when it changes the instruction flow in response to the presence of an exception, reset, a Tcc instruction, or an interrupt. The action is a vectored transfer of control to supervisor software through a table, the address of which is specified by the privileged Trap Base Address (TBA) register. *See also* **exception**.

TSB Translation storage buffer. A table of the address translations that is maintained by software in system memory and that serves as a cache of the address translations.

TSO Total store order.

TTE Translation Table Entry. Describes the virtual-to-physical translation and page attributes for a specific page in the page table. In some cases, the term is explicitly used for the entries in the TSB.

UA-2005 UltraSPARC Architecture 2005

unassigned A value (for example, an ASI number), the semantics of which are not architecturally mandated and which may be determined independently by each implementation within any guidelines given.

undefined An aspect of the architecture that has deliberately been left unspecified. Software should have no expectation of, nor make any assumptions about, an undefined feature or behavior. Use of such a feature can deliver unexpected results, may or may not cause a trap, can vary among implementations, and can vary with time on a given implementation.

Notwithstanding any of the above, undefined aspects of the architecture shall not cause security holes (such as changing the privilege state or allowing circumvention of normal restrictions imposed by the privilege state), put a virtual processor into privileged mode, or put the virtual processor into an unrecoverable state.

unimplemented An architectural feature that is not directly executed in hardware because it is optional or is emulated in software.

unpark The process of bringing a virtual processor out of suspension. There may be a delay until the virtual processor is unparked, but no heavyweight operation (such as a reset) is required to complete the unparking process.

unparked *Synonym:* **running**.

unpredictable *Synonym:* **undefined**.

uniprocessor system A system containing a single virtual processor.

unrestricted Describes an address space identifier (ASI) that can be used in all privileged modes; that is, regardless of the value of PSTATE.priv and HPSTATE.hpriv.

user application program *Synonym:* **application program**.

VA Virtual address.

virtual address An address produced by a virtual processor that maps all systemwide, program-visible memory. Virtual addresses usually are translated by a combination of hardware and software to physical addresses, which can be used to access physical memory.

virtual core, virtual processor, virtual processor core *Synonyms:* **virtual processor**.

virtual processor The term *virtual processor*, or *virtual processor core*, is used to identify each strand in a processor. Each virtual processor corresponds to a specific strand on a specific physical core where there may be multiple physical cores, each with multiple strands. Each virtual processor has its own interrupt ID. At any given time, an operating system can have a different thread scheduled on each virtual processor. *See also* **fiber**, **physical core**, **processor**, **strand**, *and* **thread**.

VIS™ VIS Instruction Set.

VP *Abbreviation for* **Virtual Processor**.

WDR Watchdog reset.

word A 4-byte datum. **Note:** The definition of this term is architecture dependent and may differ from that used in other processor architectures.

WRPR Write Privileged Register instruction.

XIR Externally initiated reset.