CALYPTECH

Signal Integrity Considerations for High Speed Digital Hardware Design

White Paper

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Abstract

As system clock frequencies and rise times increase, signal integrity design considerations are becoming ever more important. Unfortunately many Digital Designers may not recognise the importance of signal integrity issues and problems may not be identified until it is too late.

This paper presents the most common design issues affecting signal integrity in high-speed digital hardware design. These include impedance control, terminations, ground/power planes, signal routing and crosstalk. Armed with the knowledge presented here, a digital designer will be able to recognise potential signal integrity problems at the earliest design stage. Also, the designer will be able to apply techniques presented in this paper to prevent these issues affecting the performance of their design.

1 Introduction

Despite the fact that Signal Integrity (SI) is among the most fundamental of design practices for hardware engineers, the digital design community has long ignored it. Through the age of low-speed logic, designing for SI was considered wasted effort, as the probability of SI-related issues was low. However as clock rates and rise times increased through the years, the need for SI analysis and design also increased. Unfortunately many designers have not heeded the call and still neglect to consider SI in their designs.

Modern digital circuits can operate up to gigahertz frequencies with rise times in the order of fifty picoseconds. At these speeds, a carelessly designed PCB trace only needs to be an inch or so long before it radiates. Radiating traces create voltage, timing and interference problems not only on that line, but also across the entire board and even across adjacent boards.

The problem is even more critical with mixed-signal circuits. For example, consider a system that relies upon a high-performance ADC to digitize received analog signals. The energy on the digital outputs of the ADC could easily be 130dB (10,000,000,000,000 times) more the energy on the analog input. Any noise on the digital side of the ADC could annihilate the low-level analog signal so preventing noise leakage is critical.

Designing for SI need not be an arduous process. The key to designing for SI is to recognise potential problems as early in the design stage and prevent them from causing problems later. This paper outlines some key SI challenges and discusses some steps to address them.

2 Ensuring Signal Integrity

2.1 Isolation

Components on a PCB operate a variety of edge rates and have varying levels of tolerance to noise. The most straightforward method for improving SI is to physically isolate components on the PCB according to their edge rates and sensitivity. An example is shown in Figure 1. In this example, the power supply, digital I/O and high-speed logic are considered to be high-threat circuits to the sensitive clock and data converter circuits.

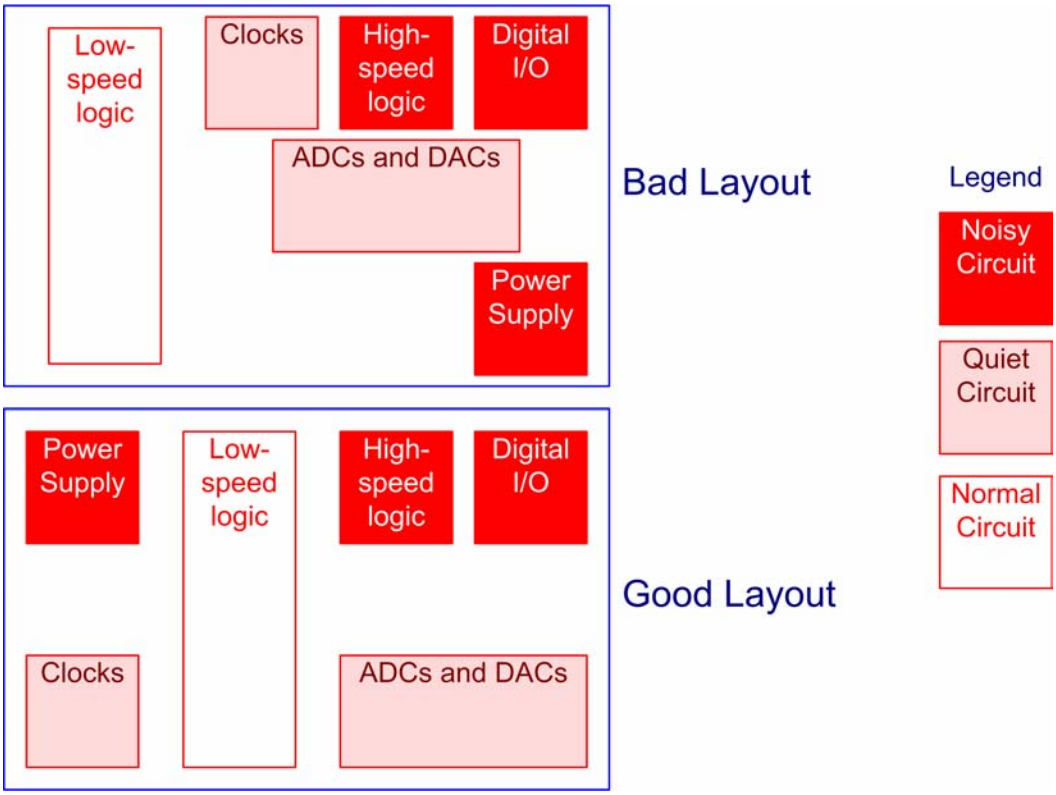

Figure 1: Isolation of Functional Blocks on a PCB

The first layout in Figure 1 places the clocks and data converters adjacent to noisy components. Noise will be coupled into the sensitive circuits and their performance will be compromised. The second layout is much better as the sensitive circuits are physically isolated from the power supply, high-speed logic and digital I/O.

2.2 Impedance, Reflections and Termination

Impedance control and terminations are fundamental design issues at high-speeds. This is a fact at the heart of every RF design. However some digital circuits operating at frequencies even higher than RF neglect to consider impedance and terminations in their design.

Impedance mismatches produce several detrimental effects in digital circuits as shown in Figure 2:

- Digital signals are reflected between the input on the receiving device and the output on the transmitting device. The reflected signals are bounced back and forward between the two ends of the line until eventually they are absorbed by resistive losses.
- The reflected signals introduce ringing on the signal being sent across the trace. Ringing impacts the voltage level and timing of the signal and can severely corrupt the trace.
- A mismatched signal path can cause the signal to be radiated into the environment.

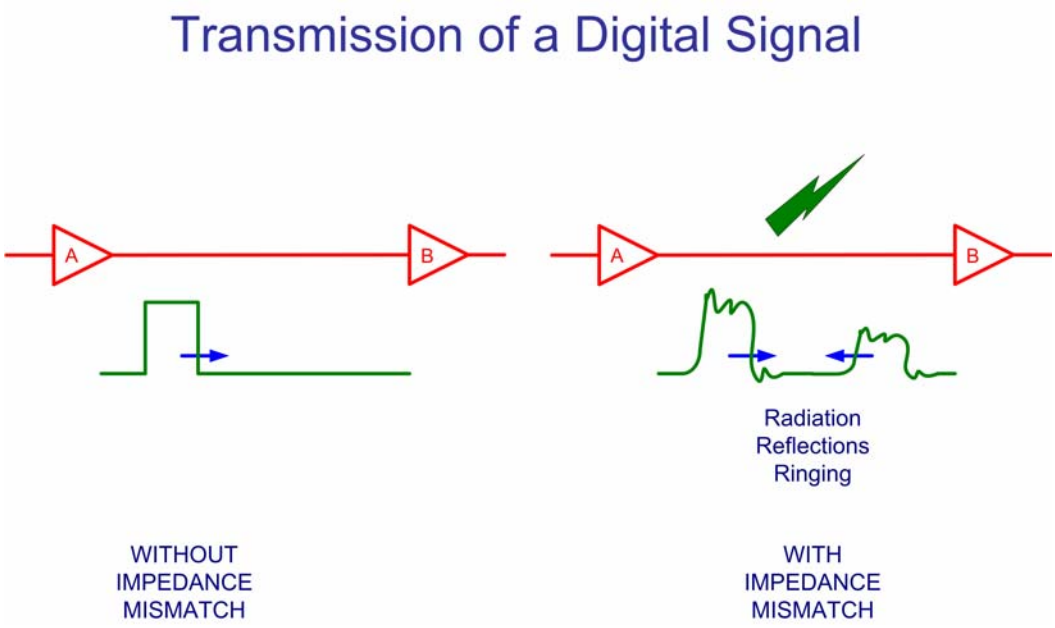

Figure 2: Transmission of a Digital Signal with and without Impedance Mismatch

Problems arising from impedance mismatch can be minimised through the use of terminators. Terminators are usually one or two discrete components placed on the signal line near the receiver. A simple example of a terminator is a low-value series resistor.

Terminators limit the rise time of a signal and partially absorb reflected energy. It is important to note that a terminator doesn't completely eliminate the destructive effects introduced by impedance mismatch. However by careful selection of the configuration and component values, a terminator can be quite effective in controlling the effects on signal integrity.

Not all traces require impedance control. Some standards such as Compact PCI require specific trace impedance and/or terminators. By making impedance requirements, these standards are quite effective in minimising reflections, ringing and emissions from signal lines.

Other standards have no specific requirement for impedance control and it is left to the designer's discretion whether or not to implement it. The decision criterion varies from one application to the next, but it tends to depend upon the length (line delay T_d) of the trace and the rise time (T_r) of the signal. An often used rule however is that impedance control is required if T_d is greater than $1/6^{th}$ of T_r [1].

2.3 Planes and Split Planes

A fact often neglected by digital designers is that current travels in loops. For example, consider a single-ended signal being transmitted between two gates as shown in Figure 3. The current travels in a loop from gate A to gate B and then back to gate A through the ground connection.

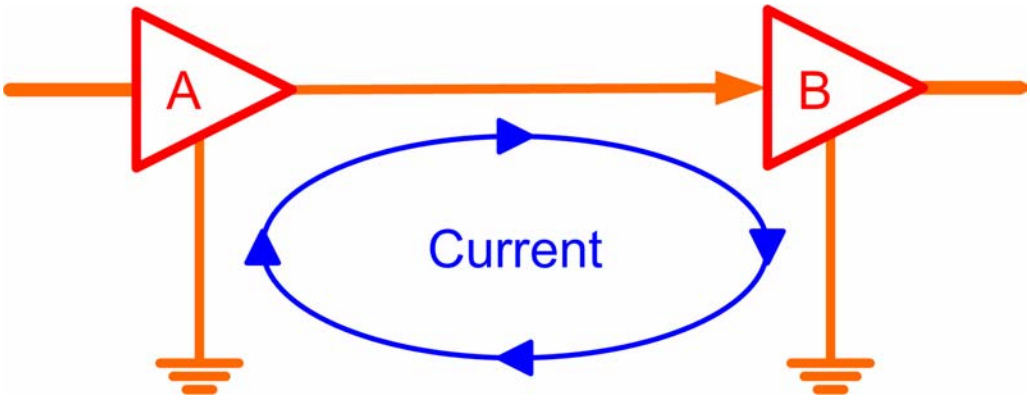

Figure 3: High Speed Signal being driven from point to point

There are two potential problems here:

1. <u>The grounds need to be connected by a low-impedance path</u>

   If the grounds are connected with a high-impedance path, then there is a voltage drop between the ground pins in Figure 3. This causes disruptions to all of the devices referenced to this ground and can degrade input noise margins.

2. <u>The loop area formed by the current loop needs to be as small as possible</u>

   Loops act as antennas. Generally speaking, a greater loop area will increase the chances of the loop radiating and conducting. It should be a goal of every PCB designer that the return current is able to travel directly underneath the signal trace, thus minimising loop area.

Using a solid plane for ground solves both problems simultaneously. A solid plane provides a low-impedance between all the ground points whilst allowing return currents to travel directly underneath their respective signal traces.

A common mistake made by PCB designers is to use holes and slots in the ground plane (Figure 4). Figure 4a shows the current flow when a signal trace is routed over a ground plane slot. The return current is forced around the slot, thus creating a large loop area. Figure 4b shows the current flow without a slot in the ground plane. Notice how the loop area is kept to a minimum.

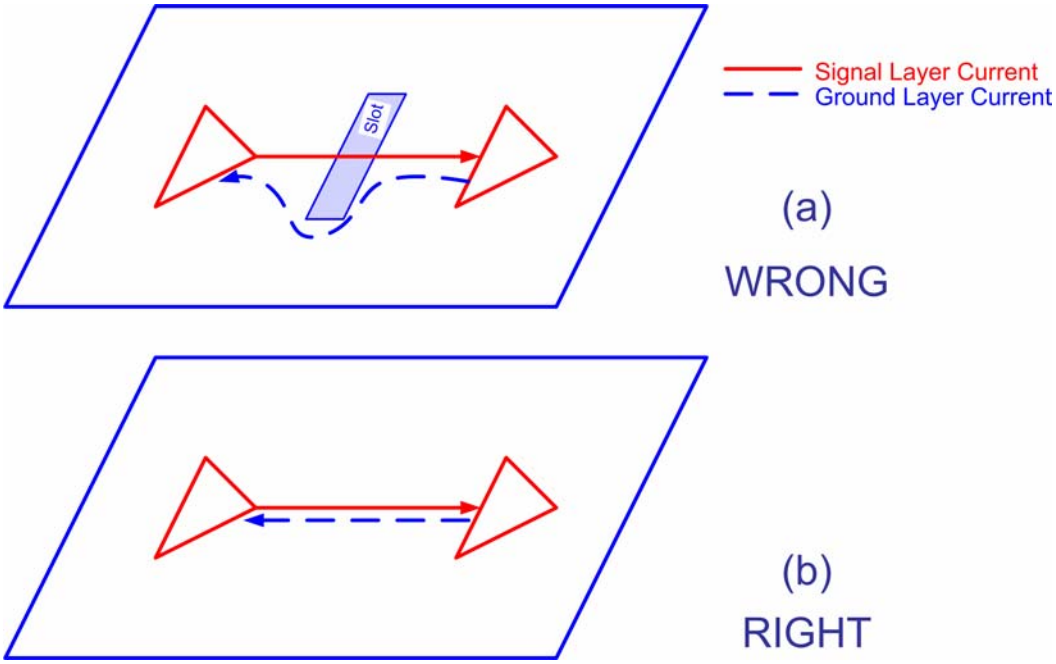

Figure 4: A Slot in a Ground Plane

Generally speaking, slots shouldn't be used in ground. However, there are occasions when slots cannot be avoided. When this happens, the PCB designer must ensure that no signal traces are routed over the slot.

The same rules apply for mixed-signal PCBs except that they often use multiple grounds. This is typical of a high-performance ADC that may utilise separate grounds for analog, digital and clock circuits. When using separate grounds, ground plane slots are imperative but again the PCB designer must be prudent in ensuring that no signals are routed over the slots.

For exactly the same reasons, the identical philosophy of using planes applies to power supplies with one minor difference: Occasionally, a PCB designed with power and ground planes will be found to radiate around the edge of the board. The electromagnetic energy emitted from the edge can disrupt adjacent cards. The situation is shown in Figure 5a. The solution, shown in Figure 5b, is to shrink the power plane so that the ground plane overlaps by a certain distance. This will reduce the amount of electromagnetic energy emitted outside of the board's immediate area and will reduce any impact on adjacent boards.

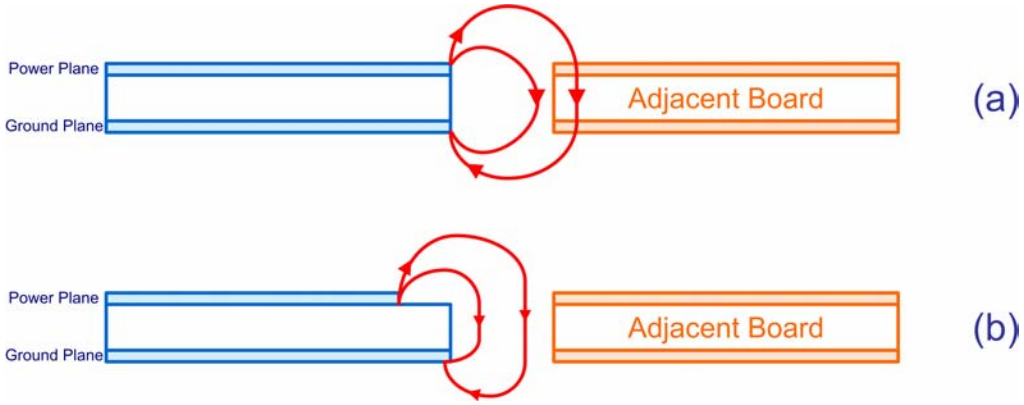

Figure 5: Edge Emissions from Power and Ground Planes

2.4 Signal Routing

An important part of ensuring signal integrity is in the physical routing of signal traces. The PCB designer is often under pressure, not only to shrink designs but also to maintain signal integrity. Finding the balance is a matter of knowing where problems can occur and how far the envelope can be pushed before the system fails.

High-speed currents cannot cope with discontinuities in the signal trace. Among the most common and problematic discontinuity is the right-angled corner (Figure 6a). Whilst right-angled corners work without problem at low-frequencies, at high-speeds they radiate. Instead, right-angles can be replaced by a mitred 90º corner (Figure 6b), or by two spaced 45º corners (Figure 6c).

Corners tighter than 90º should not even be considered for high-speed signals.

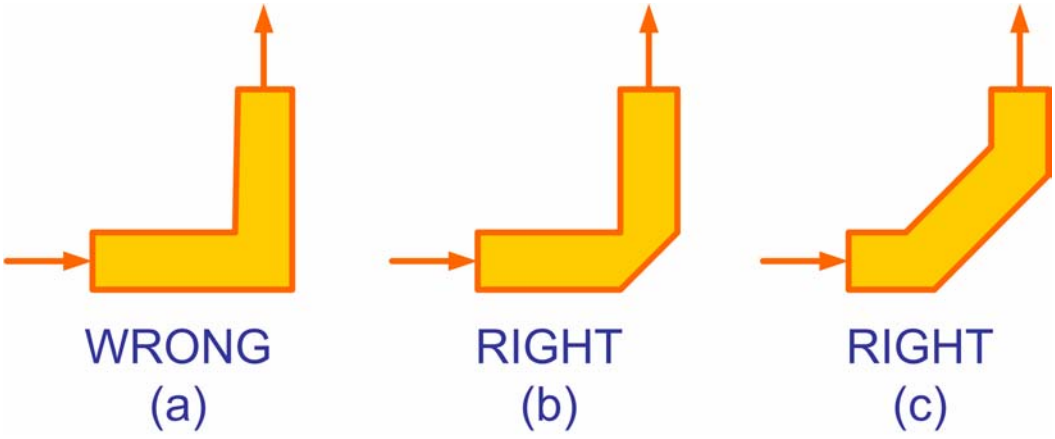

Figure 6: High-Speed Corners

Another common problem is stub traces. Unless there is a specific reason for using them, all stubs should be eliminated from the board. The problem is that at high frequencies, stubs can radiate as well as creating a host of impedance problems for signal traces.

Yet another key area in high-speed design is the routing of differential pairs. Differential pairs operate by driving two signal traces in a complementary fashion. Differential pairs

offer excellent immunity to noise and improved S/N ratio. However there are two constraints in realising these advantages:

1. The two traces must be routed adjacent to each other; and
2. The two traces must be matched in length [2].

Problems rise when a pair has to be routed around a bend as shown in Figure 7.

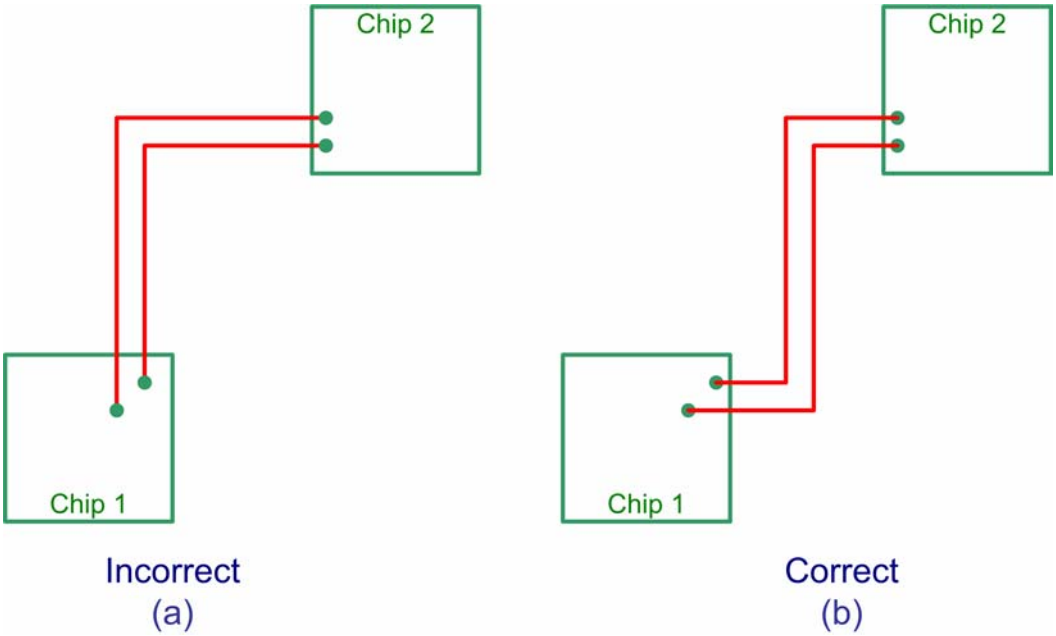

Figure 7: Routing a Differential Pair Around a Bend

The problem is to route a differential pair between two components that aren't aligned. The solution in Figure 7a is flawed because the track on the outside is clearly longer than the track on the inside. The correct solution is shown in Figure 7b. Here a left-hand turn is followed by a right-hand turn so both tracks are forced to be equal length. This illustrates a general rule in routing differential pairs: follow each bend by another in the opposite direction.

2.5 Crosstalk

Crosstalk is yet another major concern for PCB designers. Figure 8a shows the cross section of a PCB indicating three parallel traces and their associated electromagnetic (EM) fields. When the spacing between the traces is too narrow, the EM fields of the traces will interact and the signals on the traces become corrupted (Figure 8b). This is called crosstalk.

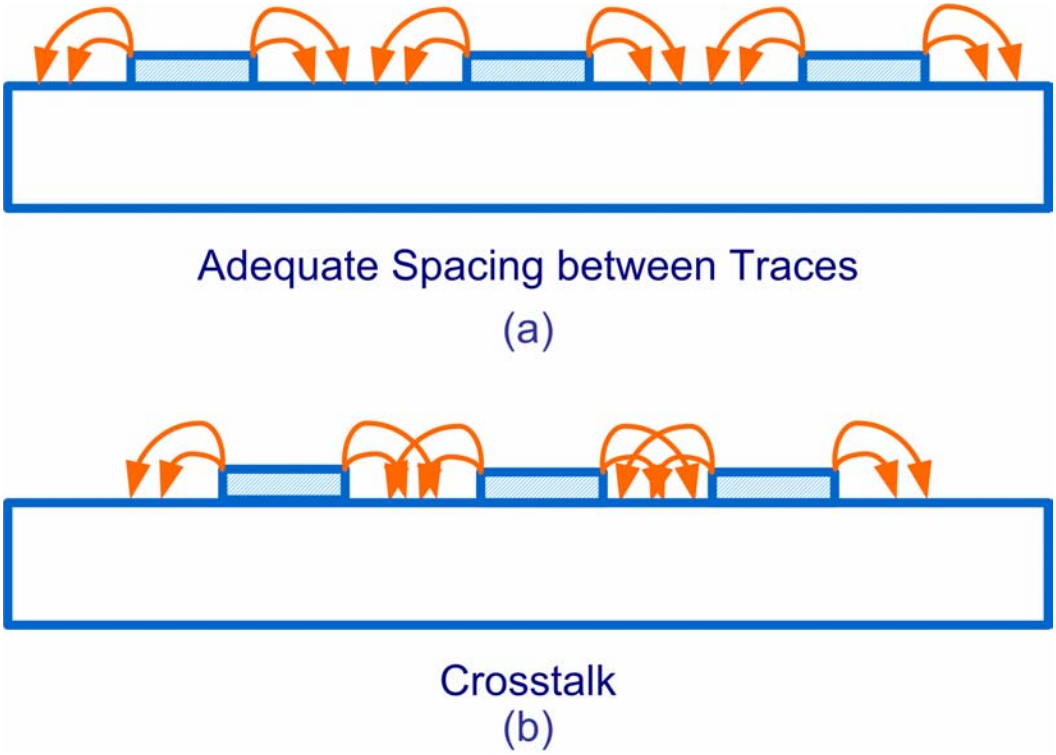

Figure 8: Crosstalk Between Adjacent PCB Traces

Crosstalk can be corrected by increasing the spacing between the spacing between tracks. However, PCB designers are under constant pressure to shrink their layouts and hence reduce the gap between tracks. Also, there are times when a designer has no alternative but to wear some amount of crosstalk in their design. Clearly, PCB designers need a strategy of managing crosstalk.

Many 'rules of thumb' have been published over the years about what is an acceptable spacing between conductors. A common rule is the 3W rule where the spacing between traces must be at least three times the width of the trace.

However the reality is that 'acceptable' spacing between conductors depends upon the application, the environment and the design margins. The spacing between traces changes from one situation to another and must be calculated for each. Furthermore, there are times when crosstalk can't be avoided and the impact of crosstalk must be calculated. In these situations there is no substitution for a computer simulation.

A good example of these issues is in high-speed, high-density connectors. Here the PCB designer may know that there is some amount of crosstalk between the conductors and he/she can't do anything about it because the geometry of the connector is fixed. By using a simulator, the designer can determine the impact on the signal integrity and can evaluate the effects on the system.

2.6 Power Supply De-coupling

Power supply de-coupling is now standard practice in digital design but we'll mention it here because of its importance in removing supply line noise.

High-frequency noise on power supplies causes problems for nearly every digital device. Such noise is typically generated by ground bounce, radiating signals or even by the digital device itself.

The simplest method of curing power supply noise is to use de-couple the high-frequency noise to ground via capacitors. Ideally, the de-coupling capacitors provide a low-impedance path to ground for the high-frequency noise, hence 'cleaning' the power supply.

The choice of de-coupling capacitors depends on the application. Most designs will locate surface mount chip capacitors as close to the power pins as physically possible. The value of these capacitors must be great enough to provide a low-impedance path for the anticipated power supply noise.

A common problem with de-coupling capacitors is that they often don't behave like capacitors. There are several reasons for this (Figure 9):

- The capacitor packaging includes some amount of lead inductance;
- Capacitors also have an amount of Equivalent Series Resistance (ESR);
- The trace between the power pin and the de-coupling capacitor has some amount of series inductance;
- The trace between the ground pin and the ground plane also has some amount of series inductance.

The cumulative effect of these problems is that:

1. The capacitor will resonate at a particular frequency and the impedance of the network will greatly change as that frequency is neared;
2. The ESR hampers the low-impedance path for the high-speed noise being de-coupled.

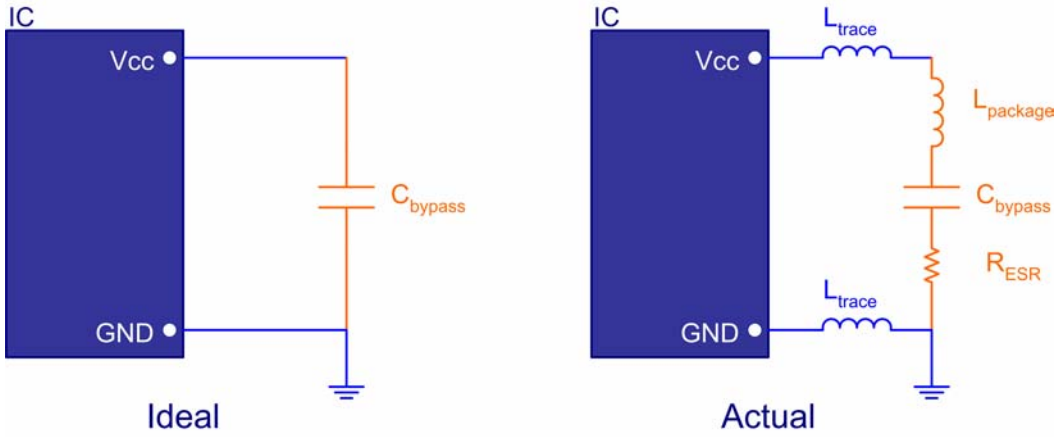

Figure 9: Realistic De-coupling

There are several things a digital designer can to counter these effects:

1. The traces emanating from the Vcc and GND pins on the device need to be as low-inductance as possible. This is done by making them as short and wide as the physical constraints allow;
2. Choosing a capacitor with a lower ESR will improve the power supply de-coupling.
3. Choosing a smaller package for the capacitor will reduce the package inductance. The trade-off for using a smaller package is the capacitance variation over temperature. After selecting a capacitor, these specs need to be verified for the design requirements;

The last point can introduce a trap for the unwary. For example, using a Y5V capacitor instead of an X7R device may allow for a smaller package and hence lower inductance, but this is at the cost of poor performance at high temperature.

A further point to consider is that a larger capacitor is often employed to provide bulk storage on the board as well as implementing low-frequency de-coupling. These capacitors are distributed more sparingly and are often electrolytic or tantalum devices.

3 Conclusion

Signal integrity is among the most important issues for high-speed digital design. This whitepaper has presented the fundamentals of signal integrity for digital hardware, including:

- Physical isolation of sensitive components from noisy components;
- Impedance control, reflections and terminations on signal traces;
- The use of solid planes for power and ground;
- Routing of signals to avoid right angle corners and stub traces;
- Routing of differential pairs to achieve length matching;
- Crosstalk in high-speed designs; and
- Power supply de-coupling.

Using the information presented here, a digital hardware designer can identify and correct potential signal integrity problems at the earliest possible stage.

The field of signal integrity is continuously developing and as such, the topics listed in this whitepaper shouldn't be considered exhaustive. The reader is encouraged to explore the topic further and make use of tools packaged with EDA software. The book and article listed as references are good places to begin searching for further information.

Glossary

ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
EDA	Electronic Design Automation
EM	Electromagnetic
ESR	Equivalent Series Resistance
IC	Integrated Circuit
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
RF	Radio Frequency
SI	Signal Integrity

References

[1] High Speed Digital Design: A Handbook of Black Magic, Johnson H and Graham M, 1993, Prentice-Hall PTR, Upper Saddle River, NJ, USA

[2] Differential Signals: Rules to Live By, Brooks D, 2001, Taken from http://www.ultracad.com/differentialrules.com