AVR 与虚拟仪器

AVR 与虚拟仪器（AVRVi），成立于 2006 年 10 月，是一家集研发、生产、教学、销售、服务为一体的机构，有正式的工商注册与网站备案。

网站中文名 AVR 与虚拟仪器，英文名 AVRVi，其中 AVR 为 ATmel 公司生产的高性能 8 位快速单片机，VI 是虚拟仪器（Virtual Instruments）的简称，本站的域名：www.avrvi.com 及子域名 *.avrvi.com 。

AVR 与虚拟仪器（AVRVi），拥有自己独立的服务器，托管于济南市双线机房，拥有电信网通双 IP，智能解析，南北互通。

网站可以提供涉及 AVR 与 Labview 的软、硬件产品与服务并可提供相应的技术支持。网站论坛提供大量的技术资料和入门教程，还有热心的会员及时地回答你在实际操作中遇到的问题，相信我们会带给你满意的服务。

目前商城中的主要产品是 AVR 开发板，AVR 仿真器和 avr 芯片，采集卡。

本站产品领域：
远程实验虚拟仪器
VI 数据采集盒、开发板
单片机教学平台
AVR 仿真器、开发板
SOC 教学平台、开发板
针对 AVR 单片机和 Labview 的相关培训
常见电子元器件

我们的目标是做好 AVR 单片机和虚拟仪器（VI）以及 Labview 的联合应用，我们的 AVR 开发板既是单片机学习板，也是虚拟仪器的采集卡。AVR 单片机我们不是最强的，Labview 我们也不是最强的，但是二者的结合点上，AVR 与虚拟仪器是第一的。

边看边译系列——TLC2543

****

特性：

12-Bit-Resolution A/D Converter
12 位 AD 转换器
10-ms Conversion Time Over Operating Temperature
10-ms 转换时间
11 Analog Input Channels
11 路模拟输入通道
Linearity Error . . . ±1 LSB Max
最大±1LSB 误差
On-Chip System Clock
片上系统时钟
End-of-Conversion Output
转换结束输出
Programmable MSB or LSB First
MSB / LSB 优先可编程
Programmable Power Down
电源管理可编程
Programmable Output Data Length
输出长度可编程

****

引脚说明：

AIN0 – AIN10：

Analog input. These 11 analog-signal inputs are internally multiplexed. The driving source impedance should
be less than or equal to 50 W for 4.1-MHz I/O CLOCK operation and be capable of slewing the analog input
voltage into a capacitance of 60 pF.

模拟输入

CS：

Chip select. A high-to-low transition on CS resets the internal counters and controls and enables DATA OUT,

DATA INPUT, and I/O CLOCK. A low-to-high transition disables DATA INPUT and I/O CLOCK within a setup time.

片选，下降沿复位内部计数器和控制器并时能数据输出，输入和 I/O 时钟。上升沿在一个准备时间内关闭数据输入和 I/O 时钟

DATA INPUT：

Serial-data input. A 4-bit serial address selects the desired analog input or test voltage to be converted next.
The serial data is presented with the MSB first and is shifted in on the first four rising edges of I/O CLOCK.
After the four address bits are read into the address register, I/O CLOCK clocks the remaining bits in order.

串行数据输入。4 位的串行地址选择模拟输入通道或者测试下次将要被转换的电压。串行数据 MSB 优先，在前 4 个上升沿被锁存。在四个地址位之后读到地址寄存器里面， I/O 时钟

驱动剩余的位按顺序排列

DATA OUT：

The 3-state serial output for the A/D conversion result. DATA OUT is in the high-impedance state when CS
is high and active when CS is low. With a valid CS, DATA OUT is removed from the high-impedance state
and is driven to the logic level corresponding to the MSB/LSB? value of the previous conversion result. The
next falling edge of I/O CLOCK drives DATA OUT to the logic level corresponding to the next MSB / LSB, and
the remaining bits are shifted out in order.

3 态 AD 转换结果输出端口。在 CS 高时输出端处于高阻状态，在 CS 低时使能输出。当 CS 有效时输出端口从高阻态变为前一次转换结果的 MSB/LSB 逻辑电平。下一个 I/O 时钟下

降沿驱动输出端变为下一个 MSB/LSB 逻辑电平（移位），其他数据位按顺序移位输出。

EOC：

End of conversion. EOC goes from a high to a low logic level after the falling edge of the last I/O CLOCK and
remains low until the conversion is complete and the data is ready for transfer.

转换结束。最后一个 I/O 时钟下降沿后 EOC 从高变为低并保持到转换完成数据准备传输。

GND：

Ground. GND is the ground return terminal for the internal circuitry. Unless otherwise noted, all voltage
measurements are with respect to GND.

地

I/O CLOCK：

Input /output clock. I/O CLOCK receives the serial input and performs the following four functions:

1. It clocks the eight input data bits into the input data register on the first eight rising edges of I/O CLOCK with the multiplexer address available after

the fourth rising edge.

2. On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplexer input begins charging the capacitor array and continues to

do so until the last falling edge of the I/O CLOCK.

3. It shifts the 11 remaining bits of the previous conversion data out on DATA OUT. Data changes on the falling edge of I/O CLOCK.

4. It transfers control of the conversion to the internal state controller on the falling edge of the last I/O CLOCK.

输入输出时钟。接受串行输入实现一些四个功能：

1、驱动 8 位输入数据到输入数据寄存器在前八个上升沿和多路地址位在四个上升沿。

2、在四个下降沿，模拟输入电压开始为电容器充电并且在最后一个下降沿到来之前一直如此。

3、驱动 11 位转换结果数据输出（因为第一位由 CS 控制输出）。数据在下降沿变化。

4、最后一个 I/O 时钟的下降沿在下降沿传输控制转换命令到内部状态控制寄存器。

REF + ：

Positive reference voltage The upper reference voltage value (nominally VCC) is applied to REF+.

The
maximum input voltage range is determined by the difference between the voltage applied to this terminal and
the voltage applied to the REF – terminal.

参考正电压输入（正常为 VCC）。最大值取决于正负参考电压之间的差。

REF－：

Negative reference voltage. The lower reference voltage value (nominally ground) is applied to REF –.

参考负电压输入（正常为 GND）

VCC：

电源正

****

操作：

Initially, with chip select (CS) high, I/O CLOCK and DATA INPUT are disabled and DATA OUT is in the
high-impedance state. CS going low begins the conversion sequence by enabling I/O CLOCK and DATA INPUT
and removes DATA OUT from the high-impedance state.

开始时将 CS 置高，I/O 时钟 和 DATA INPUT 关闭， DATA OUT 高阻态。使能 I/O 时钟 和 DATA INPUT ，将 DATA OUT 从高阻态变化 ，CS 变低开始转换。

The input data is an 8-bit data stream consisting of a 4-bit analog channel address (D7–D4), a 2-bit data length
select (D3–D2), an output MSB or LSB first bit (D1), and a unipolar or bipolar output select bit (D0) that are
applied to DATA INPUT. The I/O CLOCK sequence applied to the I/O CLOCK terminal transfers this data to the
input data register.

输入的数据为 8 位数据流。包括 4 位的模拟通道地址位 (D7－D4) ，2 位数据长度选择 (D3－D2) ，MSB or LSB 优先选择 (D1),一位单极和两极输出选择位 (D0) 。I/O 时钟将这些数

据打入输入数据寄存器。

During this transfer, the I/O CLOCK sequence also shifts the previous conversion result from the output data
register to DATA OUT. I/O CLOCK receives the input sequence of 8, 12, or 16 clock cycles long depending on
the data-length selection in the input data register. Sampling of the analog input begins on the fourth falling edge
of the input I/O CLOCK sequence and is held after the last falling edge of the I/O CLOCK sequence. The last
falling edge of the I/O CLOCK sequence also takes EOC low and begins the conversion.

在传输的过程中 I/O 时钟同样可以将转换结果通过输出引脚从输出数据寄存器中输出。I/O 时钟接收 8, 12, 16 时钟周期的长度，取决于在输入数据寄存器中数据长度的选择。

例如：模拟输入在第四个 I/O 时钟下降沿开始，在最后一个 I/O 时钟下降沿保持。最后一个下降沿同时将 EOC 拉低开始转换。

转换操作：

I/O cycle：

The I/O cycle is defined by the externally provided I/O CLOCK and lasts 8, 12, or 16 clock periods, depending on the selected output data length.

I/O 时钟周期在外部预先宏定义，持续 8, 12, or 16 时钟周期，取决于输出数据的长度。

During the I/O cycle, the following two operations take place simultaneously.

在 I/O 时钟周期内，以下两种操作同时发生。

An 8-bit data stream consisting of address and control information is provided to DATA INPUT. This data is shifted into the device on the rising edge of the

first eight I/O CLOCKs. DATA INPUT is ignored after the first eight clocks during 12- or 16-clock I/O transfers.

8 位的数据流，包括地址，控制信息等。这些数据在前八个上升沿移位输入，在 12 或 16 时钟周期的设置中后续时钟被忽略。

The data output, with a length of 8, 12, or 16 bits, is provided serially on DATA OUT. When CS is held low, the first output data bit occurs on the rising

edge of EOC. When CS is negated between conversions, the first output data bit occurs on the falling edge of CS. This data is the result of the previous

conversion period, and after the first output data bit, each succeeding bit is clocked out on the falling edge of each succeeding I/O CLOCK.

数据输出（包括 8, 12, or 16 位）预先串行传输到输出端口。当 CS 脚保持低时，第一位在 EOC 的上升沿输出。其他 11 位的靠 I/O 时钟输出。这个数据是先前转换的结果。

conversion cycle：

The conversion cycle is transparent to the user, and it is controlled by an internal clock synchronized to I/O CLOCK. During the conversion period, the

device performs a successive-approximation conversion on the analog input voltage. The EOC output goes low at the start of the conversion cycle and goes high

when conversion is complete and the output data register is latched. A conversion cycle is started only after the I/O cycle is completed, which minimizes the

influence of external digital noise on the accuracy of the conversion.

转换周期对于用户来说一目了然，受与 I/O 时钟同步的内部时钟控制。在转换周期内采用逐次逼近的方法转换模拟输入电压。在转换的开始 EOC 输出变为低，转换结束后变为高

，并且输出数据寄存器被锁定。转换周期只有在 I/O 时钟周期结束后才开始以减小外部数字噪声的干扰，保证转换的正确性。

power up and initialization：

After power up, CS must be taken from high to low to begin an I/O cycle. EOC is initially high, and the input data register is set to all zeroes. The

contents of the output data register are random, and the first conversion result should be ignored. To initialize during operation, CS is taken high and is

then returned low to begin the next I/O cycle. The first conversion after the device has returned from the power-down state may not read accurately due to

internal device settling.

上电后， CS 引脚必须从高拉低以开始一个 I/O 周期。EOC 初始为高，数据输入寄存器全部置零。输出寄存器数据随机，首次准换的结果必须被忽略。在操作中初始化，CS 脚为高

，如果被拉低则启动一次 I/O 周期。刚从断电状态返回后的第一次转换可能不准确，原因是内部设备的设置。

data input：

The data input is internally connected to an 8-bit serial-input address and control register. The register defines the operation of the converter and the

output data length. The host provides the data word with the MSB first.

数据输入在内部连接到 8 位的输入地址和控制寄存器。该寄存器决定了转换和输出的数据长度和 MSB/LSB 优先选择

Each data bit is clocked in on the rising edge of the I/O CLOCK sequence

每一个数据位在 I/O 时钟上升沿被打入。

输入寄存器数据格式见数据手册。

Select input channel：D7 D6 D5 D4

AIN0	0000
AIN1	0001
AIN2	0010
AIN3	0011
AIN4	0100
AIN5	0101
AIN6	0110
AIN7	0111
AIN8	1000
AIN9	1001
AIN10	1010

Select test voltage：D7 D6 D5 D4

(Vref+ – Vref–)/2	1011
Vref–	1100
Vref+	1101
Software power down	1110

Output data length：D3 D2

8 bits	01
12 bits	x0
16 bits	11

Output data format： D1

MSB first 0
LSB first (LSBF) 1

Unipolar (binary)： D0

Unipolar (binary) 0
Bipolar (BIP) 2s complement 1
---

data input address bits：

The four MSBs (D7 – D4) of the data register address one of the 11 input channels, a reference-test voltage, or the power-down mode. The address bits affect

the current conversion, which is the conversion that immediately follows the current I/O cycle. The reference voltage is nominally equal to Vref+ – Vref–.

数据输入位地址位：控制模拟输入通道，参考测试电压和软件电源关闭模式。地址位影响现有的转换。参考电压正常选择为 Vref+ – Vref –

data output length：

数据输出长度：

The next two bits (D3 and D2) of the data register select the output data length. The data-length selection is valid for the current I/O cycle (the cycle in

which the data is read). The data-length selection, being valid for the current I/O cycle, allows device startup without losing I/O synchronization. A data

length of 8, 12, or 16 bits can be selected. Since the converter has 12-bit resolution, a data length of 12 bits is suggested.

由于转换精度为 12 位所以推荐数据长度为 12 位。

With D3 and D2 set to 00 or 10, the device is in the 12-bit data-length mode and the result of the current conversion is output as a 12-bit serial data

stream during the next I/O cycle. The current I/O cycle must be exactly 12 bits long for proper synchronization, even when this means corrupting the output

data from a previous conversion. The current conversion is started immediately after the twelfth

falling edge of the current I/O cycle.

With bits D3 and D2 set to 11, the 16-bit data-length mode is selected, which allows convenient communication with 16-bit serial interfaces. In the 16-bit

mode, the result of the current conversion is output as a 16-bit serial data stream during the next I/O cycle with the four LSBs always reset to 0 (pad

bits). The current I/O cycle must be exactly 16 bits long to maintain synchronization even when this means corrupting the output data from the previous

conversion. The current conversion is started immediately after the sixteenth falling edge of the current I/O cycle.

With bits D3 and D2 set to 01, the 8-bit data-length mode is selected, which allows fast communication with 8-bit serial interfaces. In the 8-bit mode, the

result of the current conversion is output as an 8-bit serial data stream during the next I/O cycle. The current I/O cycle must be exactly eight bits long to

maintain synchronization, even when this means corrupting the output data from the previous conversion. The four LSBs of the conversion result are truncated

and discarded. The current conversion is started immediately after the eighth falling edge of the current I/O cycle.

Since D3 and D2 take effect on the current I/O cycle when the data length is programmed, there can be a conflict with the previous cycle when the data-word

length is changed from one cycle to the next. This may occur when the data format is selected to be least significant bit first, since at the time the data

length change becomes effective (six rising edges of I/O CLOCK), the previous conversion result has already started shifting out.

In actual operation, when different data lengths are required within an application and the data length is changed between two conversions, no more than one

conversion result can be corrupted and only when it is shifted out in LSB-first format.

在 LSB-first 格式下不超过一次的转换会是错误的。

sampling period：

采样周期：

During the sampling period, one of the analog inputs is internally connected to the capacitor array of the converter to store the analog input signal. The

converter starts sampling the selected input immediately after the four address bits have been clocked into the input data register. Sampling starts on the

fourth falling edge of I/O CLOCK. The converter remains in the sampling mode until the eighth, twelfth, or sixteenth falling edge of the I/O CLOCK depending

on the data-length selection. After the EOC delay time from the last I/O CLOCK falling edge, the EOC output goes low indicating that the sampling period is

over and the conversion period has begun. After EOC goes low, the analog input can be changed without affecting the conversion result. Since the delay from

the falling edge of the last I/O CLOCK to EOC low is fixed, time-varying analog input signals can be digitized at a fixed rate without introducing systematic

harmonic distortion or noise due to timing uncertainty.

在四位地址位被送入输入数据寄存器中后采样立即开始。采样在 I/O CLOCK 第四个上升沿开始，采样模式保持直到输出数据长度设置。在 EOC 延时后 EOC 变为低指示采样周期结束转

换周期开始。EOC 变为低后模拟输入数据可以被转换为有效的转换结果。

After the 8-bit data stream has been clocked in, DATA INPUT should be held at a fixed digital level until EOC goes high (indicating that the conversion is

complete) to maximize the sampling accuracy and minimize the influence of external digital noise.

在 8 位数据流被打入之后， DATA INPUT 应当被保持在一个确定的电平直到 EOC 变为高（指示转换结束）以尽可能的扩大采样的准确性减小外部的数字噪声。

data register, LSB first：

D1 in the input data register (LSB first) controls the direction of the output binary data transfer. When D1 is reset to 0, the conversion result is shifted

out MSB first. When set to 1, the data is shifted out LSB first. Selection of MSB first or LSB first always affects the next I/O cycle and not the current

I/O cycle. When changing from one data direction to another, the current I/O cycle is never disrupted.

data register, bipolar format：

D0 (BIP) in the input data register controls the binary data format used to represent the conversion result. When D0 is cleared to 0, the conversion result

is represented as unipolar (unsigned binary) data. Nominally, the conversion result of an input voltage equal to Vref– is a code of all zeros (000 . . . 0),

the conversion result of an input voltage equal to Vref+ is a code of all ones (111 . . . 1), and the conversion result of (Vref + + Vref–) /2 is a code of

a one followed by zeros (100 . . . 0).

决定输出数据是否有正负之分。Vref－等于 000 . . . 0 ，Vref+ 等于 111 . . . 1 。(Vref + + Vref －) /2 等于 100 . . . 0。

When D0 is set to 1, the conversion result is represented as bipolar (signed binary) data. Nominally, conversion of an input voltage equal to Vref– is a

code of a one followed by zeros (100 . . . 0), conversion of an input voltage equal to Vref+ is a code of a zero followed by all ones (011 . . . 1), and the

conversion of (Vref+ + Vref–) /2 is a code of all zeros (000 . . . 0). The MSB is interpreted as the sign bit. The bipolar data format is related to the

unipolar format in that the MSBs are always each other’s complement.

如果设置为有符号的输出则 MSB 为符号位。

Selection of the unipolar or bipolar format always affects the current conversion cycle, and the result is output during the next I/O cycle. When changing

between unipolar and bipolar formats, the data output during the current I/O cycle is not affected.

数据格式设置影响当前转换周期，即在下一周期输出。设置过程中当前 I/O 时钟周期不受影响。

EOC output：

The EOC signal indicates the beginning and the end of conversion. In the reset state, EOC is always high. During the sampling period (beginning after the

fourth falling edge of the I/O CLOCK sequence), EOC remains high until the internal sampling switch of the converter is safely opened. The opening of the

sampling switch occurs after the eighth, twelfth, or sixteenth I/O CLOCK falling edge, depending on the data-length selection in the input data register.

After the EOC signal goes low, the analog input signal can be changed without affecting the conversion result.

EOC 指示转换开始和结束。复位状态下 EOC 为高。在采样周期 EOC 保持高直到内部转换开关打开。内部转换开关打开在 eighth, twelfth, or sixteenth I/O CLOCK 下降沿，取决于数

据长度的设置。在 EOC 信号变为低以后模拟输入信号可以被改变而不会影响转换结果（内置采样保持）

The EOC signal goes high again after the conversion is completed and the conversion result is latched into the output data register. The rising edge of EOC

returns the converter to a reset state and a new I/O cycle begins.

转换结束以后 EOC 信号重新变为高。转换结果被所存到输出数据寄存器中。EOC 的上升沿将转换器转换为复位状态，新的 I/O 周期开始。

On the rising edge of EOC, the first bit of the current conversion result is on DATA OUT when CS is low. When CS is negated between conversions, the first

bit of the current conversion result occurs at DATA OUT on the falling edge of CS.

EOC 的上升沿，转换结果的第一位在 DATA OUT 引脚上等待 CS 变为低时输出。在转换过程中当 CS 无效时，当前转换结果的第一位出现在 CS 上升沿 DATA OUT 上。

data format and pad bits：

D3 and D2 of the input data register determine the number of significant bits in the digital output that represent the conversion result. The LSB-first bit

determines the direction of the data transfer while the BIP bit determines the arithmetic conversion. The numerical data is always justified toward the MSB

in any output format.

The internal conversion result is always 12 bits long. When an 8-bit data transfer is selected, the four LSBs of the internal result are discarded to provide

a faster one-byte transfer. When a 12-bit transfer is used, all bits are transferred. When a 16-bit transfer is used, four LSB pad bits are always appended

to the internal conversion result. In the LSB-first mode, four leading zeros are output. In the MSB-first mode, the last four bits output are zeros.

When CS is held low continuously, the first data bit of the newly completed conversion occurs on DATA OUT on the rising edge of EOC. When a new conversion is

started after the last falling edge of I/O CLOCK, EOC goes low and the serial output is forced to a setting of 0 until EOC goes high again.

当 CS 保持为低时，新完成转换的数据的第一位在 EOC 上升沿出现在 DATA OUT 上。当新一轮转换开始时，EOC 变为低，串行数据输出被强行设置成 0，直到 EOC 再次变成高。

When CS is negated between conversions, the first data bit occurs on DATA OUT on the falling edge of CS.

On each subsequent falling edge of I/O CLOCK after the first data bit appears, the data is changed to the next bit in the serial conversion result until the

required number of bits has been output.

第一位数据移出后，之后的数据移位。

chip-select input (CS)：

CS enables and disables the device. During normal operation, CS should be low. Although the use of CS is not necessary to synchronize a data transfer, it can

be brought high between conversions to coordinate the data transfer of several devices sharing the same bus.

正常操作过程中 CS 为低。

When CS is brought high, the serial-data output is immediately brought to the high-impedance state, releasing its output data line to other devices that may

share it. After an internally generated debounce time, I/O CLOCK is inhibited, thus preventing any further change in the internal state.

CS 设置为高时串行输出引脚被设置成高阻态，释放输出数据线以供其他设备使用数据线。

When CS is subsequently brought low again, the device is reset. CS must be held low for an internal debounce time before the reset operation takes effect.

After CS is debounced low, I/O CLOCK must remain inactive (low) for a minimum time before a new I/O cycle can start.

当 CS 被设置为低的时候，设备复位。

CS can interrupt any ongoing data transfer or any ongoing conversion. When CS is debounced low long enough before the end of the current conversion cycle,

the previous conversion result is saved in the internal output buffer and shifted out during the next I/O cycle.

CS 可以中断任何传输中的数据传输或者转换。在转换周期内如果 CS 被足够长的时间设置成低时，先前转换的结果被保存在输出缓存区内并且在下一个 I/O 周期输出。

power-down features：

When a binary address of 1110 is clocked into the input data register during the first four I/O CLOCK cycles, the power-down mode is selected. Power down is

activated on the falling edge of the fourth I/O CLOCK pulse.

当地址寄存器被打入 1110 时，掉电模式被选择。

During power down, all internal circuitry is put in a low-current standby mode. No conversions are performed, and the internal output buffer keeps the

previous conversion cycle data results provided that all digital inputs are held above VCC – 0.5 V or below 0.5 V. The I/O logic remains active so the

current I/O cycle must be completed even when the power-down mode is selected. Upon power-on reset and before the first I/O cycle, the converter normally

begins in the power-down mode. The device remains in the power-down mode until a valid input address (other than 1110) is clocked in. Upon completion of that

I/O cycle, a normal conversion is performed with the results being shifted out during the next I/O cycle.
掉电模式下不会产生转换，内部输出缓存区内是上一次转换周期的结果。所有输入引脚保持高于 VCC – 0.5 V 或者低于 0.5 V。I/O 仍然活跃，所以即使掉电模式 I/O 周期必须完成。
测试结果计算公式：测试电压=[(Vref+)-(Vref－)]*转换返回值/4096

客户服务

欢迎选购我公司编程器，仿真器，开发板等。请到http://shop.avrvi.com查询。

保修服务：

时限：一年。

- 免费保修；（正确使用下产生的质量问题，免费保修）
- 收费保修；（非正确使用情况下产生的质量问题，视损坏程度收取 5%-30%维修费）
- 请妥善保留好收据、发票；
- 若有往来的运费产生，运费由客户方承担。

售后服务：

时限：一年。

- 售后服务只限产品的使用服务，不包括教导相关软件使用等；（配套光盘已有软件使用教程）
- 不负责上门服务。

联系我们：

AVR 与虚拟仪器：

网址：http://www.avrvi.com

论坛：http://bbs.avrvi.com

商城：http://shop.avrvi.com

电话(传真)：0531-80870158