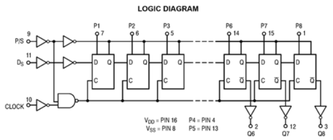

Truth Table

Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	Q_N	Q_S (Note 1)	Q'_S
⌐	0	X	X	Hi Z	Hi Z	Q7	No Change
¬	0	X	X	Hi Z	Hi Z	No Change	Q7
⌐	1	0	X	No Change	No Change	Q7	No Change
⌐	1	1	0	0	Q_N–1	Q7	No Change
⌐	1	1	1	1	Q_N–1	Q7	No Change
¬	1	1	1	No Change	No Change	No Change	Q7

X = Don't Care
¬ = HIGH-to-LOW
⌐ = LOW-to-HIGH

Note 1: At the positive clock edge, information in the i^{th} shift register stage is transferred to Q8 and Q_S.

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制图: 高永祥 Gao Yongxiang		日期: