PRELIMINARY DATA SHEET

AC508

Integrated 10/100BASE-T/TX 9-Port Switch

GENERAL DESCRIPTION

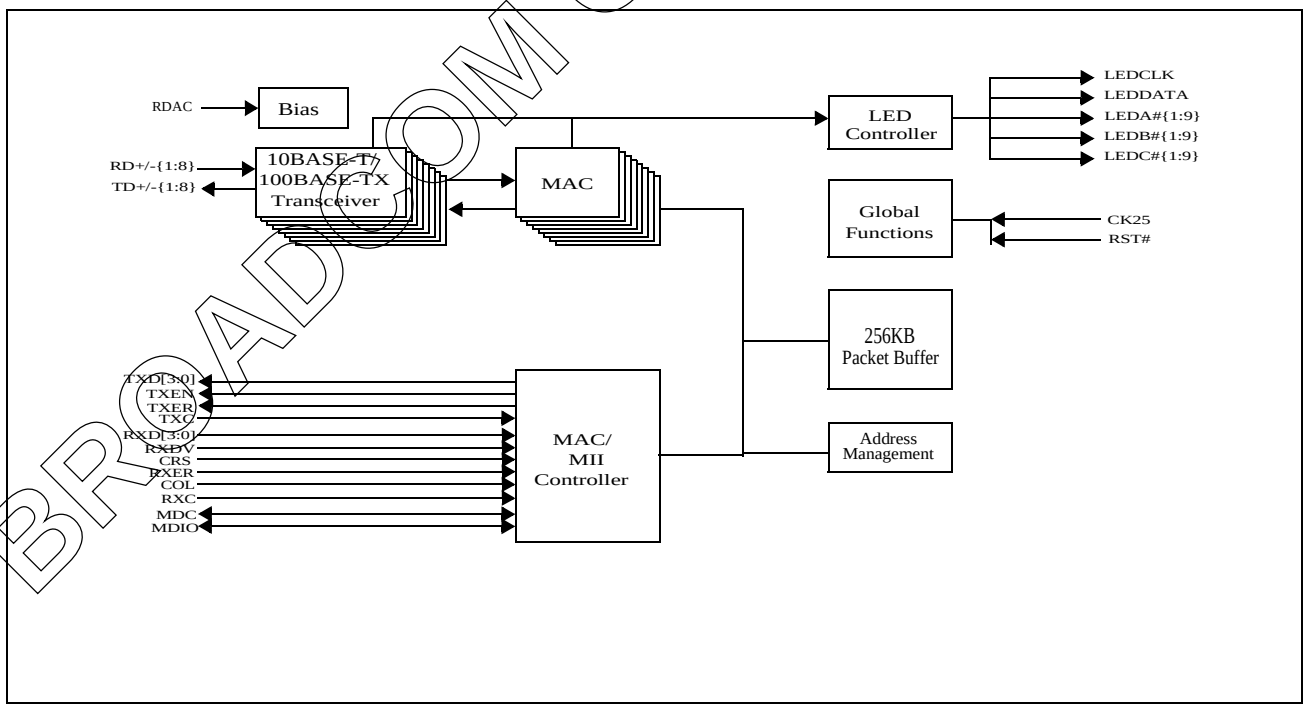
The AC508 is a nine-port, 10/100BASE-T/TX integrated switch targeted at cost-sensitive Fast Ethernet unmanaged switch systems. The device contains eight full-duplex 10BASE-T/100BASE-TX Fast Ethernet transceivers, each of which performs all of the physical layer interface functions for 10BASE-T Ethernet on CAT 3, 4 or 5 unshielded twisted pair (UTP) cable and 100BASE-TX Fast Ethernet on CAT 5 UTP cable.

The AC508 device provides a very highly integrated solution. It combines all of the functions of a high speed switch system, including packet buffer, transceivers, media access controllers, address management and a non-blocking switch controller, into a single monolithic 0.18µm CMOS device. It complies with the IEEE 802.3, 802.3u, and 802.3x specifications, including the MAC control PAUSE frame and Auto-Negotiation subsections, providing compatibility with all industry-standard Ethernet and Fast Ethernet devices.

The AC508 supports very low cost management utilizing the proprietary MIB Autocast™ function. This function requires only a small low cost microcontroller to initialize and configure the device.

FEATURES

- Nine-port 10/100 Mbps integrated switch controller
- 256-KB on-chip Packet Buffer
- Eight integrated 10/100BASE-T/TX IEEE 802.3u Compliant Transceivers
- Integrated Full-Duplex Capable 802.3x Compliant Media Access Controllers
- Integrated Address Management
  - Supports up to 4K unicast addresses
- Ninth MII port provided for an additional TX/FX uplink
- Low-power 3.3 / 1.8V, 0.18mm CMOS Technology
- 208-pin PQFP package



Functional Block Diagram

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REVISION HISTORY

Revision	*Date*	*Change Description*
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Section 1: Functional Description

OVERVIEW

The AC508 is a single-chip, nine-port 10/100BASE-TX switch device. This device integrates eight 10/100BASE-TX transceivers, one general use (10/100BASE-TX/FX) MII, nine full-duplex capable Media Access Controllers (MACs), a Serial Management Port, high-performance integrated packet buffer memory, an address resolution engine, a non-blocking switch controller.

The integrated 10/100BASE-TX transceivers perform all the physical layer interface functions for 100BASE-TX full-duplex or half-duplex Ethernet on CAT 5 twisted pair cable and 10BASE-T full- or half-duplex Ethernet on CAT 3, 4, or 5 cable.

The transceiver performs 4B5B, MLT3, NRZI, and Manchester encoding and decoding, clock and data recovery, stream cipher scrambling/descrambling, digital adaptive equalization, line transmission, carrier sense and link integrity monitor, auto-negotiation and MII management functions. Each of the eight integrated transceiver ports of the AC508 connects directly to the network media through isolation transformers. The integrated transceiver is fully compliant with the IEEE 802.3 and 802.3u standards.

The device provides nine internal media access controllers. Each MAC is dual-speed and both half- and full-duplex capable. Flow control is provided in the half-duplex mode with backpressure. In full-duplex mode, 802.3x frame-based flow control is provided. The MAC is 802.3 compliant and supports a maximum frame size of 1536 bytes.

An integrated address management engine provides address learning and recognition functions at maximum frame rates. The address table provides capacity for up to 4K unicast addresses. Addresses are added to the table after receiving an error-free packet. Broadcast and multicast frames are forwarded to all ports except the port where it was received.

GLOBAL FUNCTIONS

CLOCKS

The device requires a single 25-MHz clock signal at the CK25 input pin. The other clock option is using a 25-Mhz crystal at XTALI/CK25 and XTALO pins. An internal PLL derives all the clock frequencies needed by the device from the single clock input. The device generates all internal clocks to the packet buffer memory. When using a ninth MII port, an additional 25-MHz receive and transmit clock must be supplied by the external transceiver.

RESET

A power-on, or hard reset, is initiated by an active low reset pulse on the RST# signal pin. An internal circuit guarantees a sufficiently long reset pulse is applied to all internal circuits. The initialization process loads all pin configurable modes, resets all internal processes and returns them to an idle state, and initializes the memory structure. At the completion of the reset sequence, all ports are enabled for frame reception and transmission.

During initialization, the CK25 input signal must be active and the power supply to the device stable.

PHYSICAL LAYER TRANSCEIVERS

ENCODER/DECODER

In 100BASE-TX mode, the transceiver transmits and receives a continuous data stream on twisted pair. During transmission, nibble wide (4-bit) data from the MAC is encoded into 5-bit code groups and inserted into the transmit data stream. The transmit packet is encapsulated by replacing the first 2 nibbles of preamble with a start of stream delimiter (J/K codes) and appending an end of stream delimiter (T/R codes) to the end of the packet. When the MII transmit error input is asserted during a packet, the transmit error code group (H) is sent in place of the corresponding data code group. The transmitter repeatedly sends the idle code group in between packets.

In TX mode, the encoded data stream is scrambled by a stream cipher block and then serialized and encoded into MLT3 signal levels. A multimode transmit DAC is used to drive the MLT3 data onto the twisted pair cable.

Following baseline wander correction, adaptive equalization and clock recovery in TX mode, the receive data stream is converted from MLT3 to serial NRZ data. The NRZ data is descrambled by the stream cipher block and then deserialized and aligned into 5-bit code groups.

The 5-bit code groups are decoded into 4-bit data nibbles and provided as the input data stream to the MAC. The start of stream delimiter is replaced with preamble nibbles and the end of stream delimiter and idle codes are replaced with all zeros. When an invalid code group is detected in the data stream, the transceiver asserts a receiver error indication to the MAC.

In 10BASE-T mode, Manchester encoding and decoding is performed on the data stream. The multimode transmit DAC performs pre-equalization for 100 meters of CAT 3 cable.

LINK MONITOR

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal or certain invalid signals are detected on the receive pair, the link monitor enters and remains in the Link Fail state where only idle codes will be transmitted. When a valid signal is detected on the receive pair for a minimum period of time, the link monitor enters the Link Pass state and the transmit and receive functions are enabled.

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the RD+/- pins for the presence of valid link pulses.

COLLISION DETECTION

In half-duplex mode, collisions are detected whenever the transceiver is simultaneously transmitting and receiving activity.

AUTO-NEGOTIATION

Each internal transceiver contains the ability to negotiate its mode of operation over the twisted pair link using the auto-negotiation mechanism defined in the IEEE 802.3u specification. During auto-negotiation, each port automatically chooses its mode of operation by advertising its abilities and comparing them with those received from its link partner. The AC508 is configured to advertise 802.3x flow-control capability, and can also advertise that it is Next Page capable. The transceiver negotiates with its link partner and chooses the highest level of operation available for its own link. In FDX mode, flow control is also negotiated. In HDX mode, flow control is enabled/disabled based on pin strappings. The auto-negotiation algorithm supports the Parallel Detection function for legacy 10BASE-T devices and 100BASE-TX-only devices that do not support auto-negotiation.

DIGITAL ADAPTIVE EQUALIZER

The digital adaptive equalizer removes inter-symbol interference created by the transmission channel media. The equalizer accepts sampled unequalized data from the ADC on each channel and produces equalized data. The AC508 achieves an optimum signal-to-noise ratio by using a combination of feed-forward equalization and decision-feedback equalization. This

powerful technique achieves a 100BASE-TX BER of less than 1 x 10^{-12} for transmission up to 100 meters on CAT 5 twisted-pair cable, even in harsh noise environments. The digital adaptive equalizers in the AC508 achieve performance close to theoretical limits. The all-digital nature of the design makes the performance very tolerant to on-chip noise. The filter coefficients are self-adapting to any quality of cable or cable length. Due to transmit pre-equalization in 10BASE-T mode and complete lack of ISI in 100BASE-FX mode, the adaptive equalizer is bypassed in these two modes.

ADC

The receive channel has a 6-bit, 125-MHz analog-to-digital converter (ADC). The ADC samples the incoming data on the receive channel and produces a 6-bit output. The output of the ADC is fed to the digital adaptive equalizer. Advanced analog circuit techniques achieve low-offset, high-power supply noise rejection, fast settling time, and low bit error rate.

Digital Clock Recovery/Generator

The all-digital clock recovery and generator block creates all internal transmit and receive clocks. The transmit clock is locked to the 25-MHz clock input while the receive clock is locked to the incoming data stream. Clock recovery circuits optimized to MLT3, NRZI, and Manchester encoding schemes are included for use with each of the three different operating modes. The input data stream is sampled by the recovered clock and fed synchronously to the digital adaptive equalizer.

Baseline Wander Correction

A 100BASE-TX data stream is not always DC balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can wander. This effect, known as baseline wander, can greatly reduce the noise immunity of the receiver. The transceiver automatically compensates for baseline wander by removing the DC offset from the input signal, and thereby significantly reduces the chance of a receive symbol error.

Digital to Analog Converter

The multimode transmit digital-to-analog converter (DAC) transmits MLT3-coded symbols in 100BASE-TX mode and Manchester-coded symbols in 10BASE-T mode. It performs programmable edge-rate control in TX mode, which decreases unwanted high frequency signal components, thus reducing EMI. High-frequency pre-emphasis is performed in 10BASE-T mode. The transmit DAC utilizes a current drive output that is well balanced and produces very low noise transmit signals.

Stream Cipher

In 100BASE-TX mode, the transmit data stream is scrambled to reduce radiated emissions on the twisted-pair cable. The data is scrambled by exclusive Oring the NRZ signal with the output of an 11-bit-wide linear feedback shift register (LFSR), which produces a 2047-bit, non-repeating sequence. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies.

The receiver descrambles the incoming data stream by exclusive Oring it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle codes. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle code groups. The receiver does not attempt to decode the data stream unless the descrambler is locked. When locked, the descrambler continuously monitors the data stream to make sure that it has not lost synchronization. The receive data stream is expected to contain inter-packet idle periods. If the descrambler does not detect enough idle codes within 724 µs, it becomes unlocked, and the receive decoder is disabled. The descrambler is always forced into the unlocked state when a link failure condition is detected.

Stream cipher scrambling/descrambling is not used in 10BASE-T modes.

MII MANAGEMENT

Each transceiver within the AC508 contains a complete set of MII management registers. The 5-bit transceiver address is assigned by concatenation of the 2-bit 00 and the internal 3-bit port ID. All MII Management registers can be accessed through the shared MII Management Port using the MDC and MDIO signals, or through the Serial Management Port.

MEDIA ACCESS CONTROLLERS

The AC508 contains nine internal dual-speed MACs. The MACs automatically select 10- or 100-Mbit mode, CSMA/CD or full-duplex, based on the result of auto-negotiation. In FDX mode, 802.3x PAUSE-frame-based flow control is also determined through auto-negotiation. The MACs are compliant with IEEE 802.3, 802.3u, and 802.3x specifications.

RECEIVE FUNCTION

The MAC initiates frame reception following the assertion of receive data valid indication from the physical layer. The MAC monitors the frame for the following error conditions:

- Receive error indication from the PHY
- Runt frame error if frame is fewer than 64 bytes
- CRC error
- Long frame error if frame is greater than 1536 bytes

If no errors are detected the frame is processed by the switch controller. Frames with errors are discarded.

TRANSMIT FUNCTION

Frame transmission begins with the switch controller queuing a frame to the MAC transmitter. The frame data is transmitted as received from the switch controller. The transmit controller is responsible for preamble insertion, carrier deferral, collision backoff, and inter-packet gap enforcement.

In half-duplex mode, when a frame is queued for transmission, the transmit controller behaves as specified by the 802.3 requirements for frame deferral. Following deferral, the transmitter adds 8 bytes of preamble and SFD to the frame data received from the switch controller. If, during frame transmission, a collision is observed and the collision window timer has not expired, the transmit controller asserts jam and then executes the backoff algorithm. The frame is retransmitted when appropriate. On the sixteenth consecutive collision the backoff algorithm starts over at the initial state, the collision counter is reset and attempts to transmit the current frame continue. Following a late collision, the frame is aborted and the switch controller is allowed to queue the next frame for transmission.

While in full-duplex mode, the transmit controller ignores carrier activity and collision indication. Transmission begins after the switch controller queues the frame and the 96 bit times of IPG have been observed.

FLOW CONTROL

The AC508 implements an intelligent flow control algorithm to minimize the system impact resulting from flow control measures. Buffer memory allocation is adaptive to the status of each port's speed and duplex mode, providing an optimal balance between flow management and per-port memory depth. The AC508 initiates flow control in response to buffer memory conditions on a per-port basis.

The MACs are capable of flow control in both full-and half-duplex modes. In half-duplex mode, the MAC backpressures a receiving port by transmitting a 96-bit time-jam packet to the port. A single jam packet is asserted for each received packet for the duration of the time the port is in the flow control state.

Flow control in full-duplex mode functions as specified by the IEEE 802.3x requirements. In the receiver, MAC flow control frames are recognized and, when properly received, set the flow control pause time for the transmit controller. The pause time is assigned from the 2-byte pause time field following the pause opcode. MAC control PAUSE frames are not forwarded from the receiver to the switch controller.

When the switch controller requests flow control from a port, the transmit controller transmits a MAC control PAUSE frame with the pause time set to the PAUSE_QUANTA register value (default is set to maximum). When the condition that caused the flow control state is no longer present, a MAC control PAUSE frame is sent with the pause time field set to 0.

The flow control capabilities of the AC508 are enabled based on the results of auto-negotiation and the state of the ENFDXFLOW and ENHDXFLOW control signals loaded during reset. Flow control in half-duplex mode is independent of the state of the link partner's flow control capability. See Table 1 for more detailed information.

Table 1: Flow Control Modes

LPFCCAP	*ENFDXFlow*	*ENHDXFLOW*	*FLOW CONTROL*	
			Full Duplex	*Half Duplex*
X	X	0	-	Disabled
X	X	1	-	Enabled
0	0	X	Disabled	-
0	1	X	Disabled	-
1	0	X	Disabled	-
1	1	X	Enabled	-

Note: **LPFCCAP**: Link Partner Flow Control Capability. Obtained from Result of auto-negotiation.

ADDRESS MANAGEMENT

The AC508 Address Resolution Logic contains the following features:

- The ‘two-bin per bucket” address table configuration
- Hashing of the DA MAC address to generate the address table pointer

The address management unit of the AC508 provides packet rate learning and recognition functions. The address table supports 2K unicast addresses in the 256 KB on-chip memory. Although the address table shares the packet buffer memory, adequate memory bandwidth is provided for both functions to operate at maximum packet rate.

ADDRESS TABLE ORGANIZATION

The address table is in the bottom of the internal SRAM, occupying the address range from 3800 to 3FFF. Each bucket contains two entries (or bins). The address table is organized into 1K buckets with two entries in each bucket. This allows up to two MAC addresses with the same index bits to be mapped into the address table.

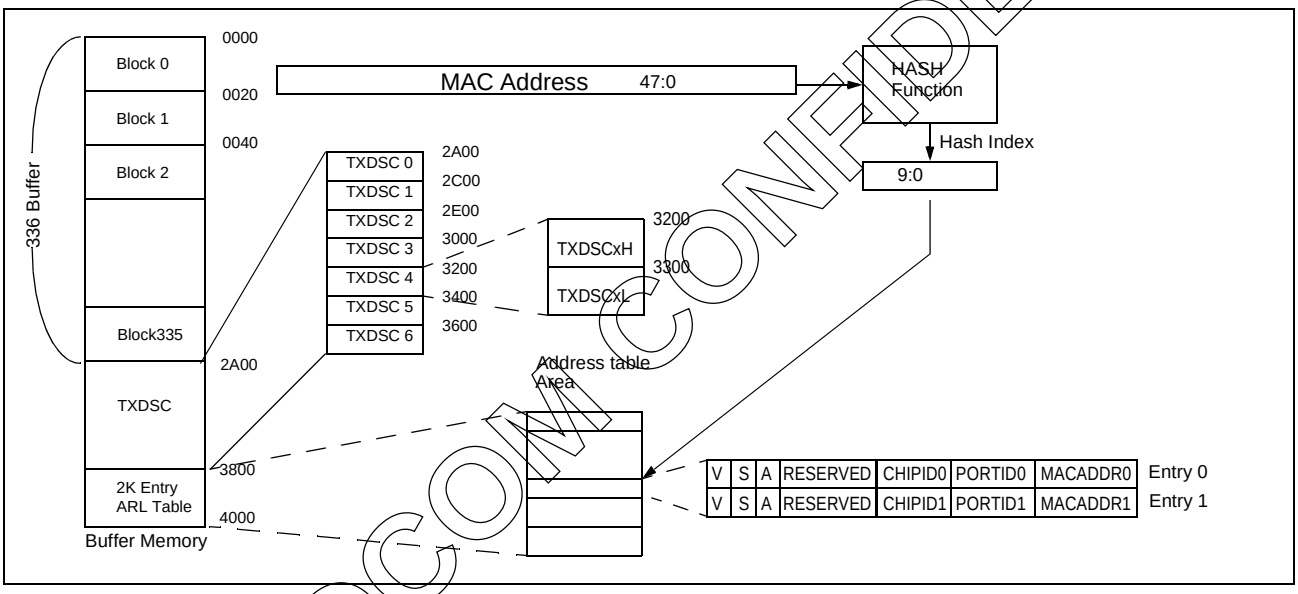


Figure 1: AC508 Mode Address Table Organization

The index into the address table is computed from the MAC address using a hash algorithm. The hash algorithm uses the CRC-CCITT polynomial. The 48-bit MAC address is reduced to a 16 bit CRC hash value. Bits 9:0 of the CRC are used index the 2k address table.

The CRC-CCITT polynomial is:

$$x^{16}+x^{12}+x^{5}+1$$

Hashing can be disabled by setting HASH_DISABLE = 1 in the ARL Configuration register, in which case the AC508 device will revert to the direct addressing method.

RESERVED ADDRESSES

The AC508 treats certain of the 802.1 administered “reserved multicast” destination addresses in specific ways, dependent on the mode of operation. Table 2 defines the response to these reserved multicast addresses.

Table 2: Behavior for Reserved Multicast Addresses

MAC Address	Function	802.1 Specified Action	Action
01-80-C2-00-00-00	Bridge Group Address	Drop Frame	Forward Frame
01-80-C2-00-00-01	IEEE Std 802.3x MAC Control Frame	Drop Frame	Receive MAC Determines if Valid PAUSE Frame and Acts Accordingly
01-80-C2-00-00-02	RESERVED	Drop Frame	Drop Frame
01-80-C2-00-00-03	RESERVED	Drop Frame	Drop Frame
01-80-C2-00-00-04	RESERVED	Drop Frame	Drop Frame
01-80-C2-00-00-05	RESERVED	Drop Frame	Drop Frame
01-80-C2-00-00-06	RESERVED	Drop Frame	Drop Frame
01-80-C2-00-00-07	RESERVED	Drop Frame	Drop Frame
01-80-C2-00-00-08	RESERVED	Drop Frame	Drop Frame
01-80-C2-00-00-09	RESERVED	Drop Frame	Drop Frame
01-80-C2-00-00-0A	RESERVED	Drop Frame	Drop Frame
01-80-C2-00-00-0B	RESERVED	Drop Frame	Drop Frame
01-80-C2-00-00-0C	RESERVED	Drop Frame	Drop Frame
01-80-C2-00-00-0D	RESERVED	Drop Frame	Drop Frame
01-80-C2-00-00-0E	RESERVED	Drop Frame	Drop Frame
01-80-C2-00-00-0F	RESERVED	Drop Frame	Drop Frame
01-80-C2-00-00-10	All LANs Bridge Management Group Address	Forward Frame	Forward Frame
01-80-C2-00-00-20	GMRP address	Forward Frame	Forward Frame
01-80-C2-00-00-21	GVRP address	Forward Frame	Forward Frame
01-80-C2-00-00-22	RESERVED	Forward Frame	Forward Frame
01-80-C2-00-00-23	RESERVED	Forward Frame	Forward Frame
01-80-C2-00-00-24	RESERVED	Forward Frame	Forward Frame
01-80-C2-00-00-25	RESERVED	Forward Frame	Forward Frame
01-80-C2-00-00-26	RESERVED	Forward Frame	Forward Frame
01-80-C2-00-00-27	RESERVED	Forward Frame	Forward Frame
01-80-C2-00-00-28	RESERVED	Forward Frame	Forward Frame
01-80-C2-00-00-29	RESERVED	Forward Frame	Forward Frame
01-80-C2-00-00-2A	RESERVED	Forward Frame	Forward Frame
01-80-C2-00-00-2B	RESERVED	Forward Frame	Forward Frame
01-80-C2-00-00-2C	RESERVED	Forward Frame	Forward Frame
01-80-C2-00-00-2D	RESERVED	Forward Frame	Forward Frame
01-80-C2-00-00-2E	RESERVED	Forward Frame	Forward Frame
01-80-C2-00-00-2F	RESERVED	Forward Frame	Forward Frame

LEARNING

During the receive process the source address (SA) of the packet is saved until completion of the packet. The address is stored in the address table memory if the following conditions are met:

- The packet is not from the Management port.
- The packet has been received without error.
- The packet is of legal length.
- The packet has a unicast address.
- There is a free space available in one of the two entries in the bucket that the hashed address indexes to. If there is no free space available in the bucket, the address is not learned.

When learning, the MAC address and the source port ID is stored into the address table. The **VALID** bit is set, the **AGE** bit is set.

RESOLUTION

The destination address (DA) of the received packet is used by the address resolution function to search the address table and assign a destination port for the packet. The destination port is assigned by locating a matching address in the address table and selecting the source port identifier field as the destination port. The search for a matching address occurs only for unicast packets. The address resolution function for unicast packets proceeds as follows:

- The lower 11 bits of the DA are used as a pointer into the address table memory and both entries in the bucket are retrieved. The address resolution logic processes the two entries in parallel.
- If the valid indicator is set and the address stored at one of the locations matches the DA of the packet received, the port identifier is assigned to be the destination port of the packet.
- If the destination port matches the source port, the packet is not forwarded.
- If the valid indicator is not set or the address stored does not match the DA address of the packet, the packet is forwarded as a broadcast packet and will be transmitted to all other ports.
- If the DA matches the globally assigned multicast address of the 802.3x MAC Control PAUSE frame of 01-80-C2-00-00-01, the packet is not forwarded.
- If the DA matches the Bridge Group Address, the packet is forwarded to all ports except the source port.
- If the DA matches one of the other globally assigned reserved address (between 01-80-C2-00-00-02 and 01-80-C2-00-00-0F), the packet is not forwarded.
- All other multicast and broadcast packets are forwarded to all ports except the source port and the Management Port.

AGING

The Aging process periodically removes dynamically learned addresses. The AGE_TIME is a timer with a value of 300 s. For each entry in the Address Table, the Aging process performs the following:

- If the VALID bit is not set, do nothing.
- If the VALID bit is set, and the AGE bit is set, reset the AGE bit. This keeps the entry in the table.
- If the VALID bit is set, and the AGE bit is reset, reset the VALID bit. This effectively deletes the entry from the Address Table.

HASH FUNCTION

The address resolution logic incorporates a hash function to randomize storage location for the MAC address. The hash function can be disabled using the HASH_DISABLE bit in the Switch Mode register.

SWITCH CONTROLLER

The core of the AC508 device is a cost effective and high performance switch controller. The controller manages packet forwarding between the MAC receive and transmit ports through the frame buffer memory with a store and forward architecture. The switch controller encompasses the functions of buffer management, memory arbitration and transmit descriptor queueing.

BUFFER MANAGEMENT

The frame buffer memory is divided into 256 bytes per page. Each packet received may allocated more than one page, of which, six pages are required for store maximum 1536B frame data. Frame data is stored to the memory block as the packet is received. After reception, the frame is queued to the egress port(s) transmit queue. For unicast frames, following transmission of a packet from the frame buffer memory, the block of memory for the frame is released to the free buffer pool. If the frame is destined to multiple ports, the memory block is not released until all ports complete transmission of the frame.

MEMORY ARBITRATION

Processes requesting access to the internal memory include the receive and transmit frame data handlers, address resolution, learning and aging functions, and output port queue managers. These processes are arbitrated to provide fair access to the memory and minimize latency of critical processes to provide a fully non blocking solution.

TRANSMIT OUTPUT PORT QUEUES

When the Quality of Service (QoS) function is turned off, the switch controller maintains an output port queue for each port. The queues are located in the internal memory and the maximum depth of the queue is 336 (i.e., 336 transmit descriptors). The queue depth becomes 256 for each output port when the QoS function is on. Transmit descriptors are updated after the packet has been received and the destination port resolved. One or two transmit descriptors are assigned to each destination port queue linking the destination with the frame data. For packets which have frame sizes larger than 1024 bytes, two transmit descriptors are required. In the case of multicast and broadcast packets, a transmit descriptor for the packet is assigned to the transmit descriptor queues of multiple ports.

For each port, frames are initiated for transmission with minimum IPG until the transmit descriptor queue of the port is empty.

INTEGRATED HIGH-PERFORMANCE MEMORY

The AC508 includes 256 KB of integrated, high-performance RAM which stores all packet buffer and address table information; and eliminates the need for external memory. This allows for the implementation of extremely low-cost systems.

The internal RAM controller efficiently executes memory transfers and achieves non-blocking performance.

CLOCKING

The AC508 provides simple clock selection. From a single 25-MHz clock input, the device's internal clocks operate up to 83 MHz; this affects the operation of the system logic and internal RAM.

MII/7-WIRE PORT

The AC508 provides a fully 802.3u compatible MII as well as 7 Wire interface as a ninth network port. The port can be configured to operate differently dependent on the programming of the internal registers.

MII MAC PORT

In its default mode after power-up, the MII operates as a normal MAC-based MII port, capable of interfacing directly to an external TX or FX transceiver. The port incorporates a ninth internal MAC, and functions identically to the eight integrated 10/100 ports. By using the strap pin, the ninth network port can be configured to use a 7-Wire interface. The 7-Wire interface enables glueless connection to legacy processors for management functions.

LED INTERFACES

The AC508 provides visibility per port of link status, port speed, duplex mode, combined transmit and receive activity, and collision. Both a parallel and serial interface are supplied to drive the status to the LEDs. The parallel interface provides the lowest cost solution for implementing LEDs. However, as the port density of the system increases, the number of signals required for the parallel implementation may become prohibitively large. In these cases, the serial mode will be more appropriate. The serial interface provides up to 5 status indications per port; whereas, the parallel interface indicates only up to three. Combinations of serial and parallel status can also be effective in lowering the system cost.

During power-on and reset, the parallel LED signals are driven low and the serial interface shifts a continuous low value for 1.34s.

PARALLEL LED INTERFACE

Three pins per port, including the MII port, are provided for directly driving LED status: LEDA#, LEDB#, LEDC#. The LED mode configuration signals control the LED status type driven by each pin. Table 3 on page 14 describes the selectable status types and Table 4 on page 14 gives a complete LED mode matrix for parallel interface.

SERIAL LED INTERFACE

A two pin serial interface, LEDDATA and LEDCLK, provides data and clock to enable external shift registers to capture the LED status indications from the AC508 for each internal port. The status encapsulated within the shift sequence is configured by the LED mode configuration signals. The configuration signals select both the number of status bits per port and the status type of each bit. The serial interface also provides an 8-bit value indicating the percentage of total bandwidth used by the switch.

The LEDCLK is generated by dividing the 25 MHz input clock by 16, providing a 640 ns clock period. The LEDDATA outputs are generated on the falling edge of the LEDCLK, and have adequate setup and hold time to be clock externally on the rising edge of LEDCLK. The shift sequence is a consecutive stream of 8-bit status words. The first word of the sequence is the LOAD status, followed by optional port status words. Each 8-bit port status word contains one bit for each port of the designated LED status type. The words are shifted MSB first. For a port status word, the MSB corresponds to port 7. The shift sequence is repeated every 42 ms.

Refer to Figure 2 on page 12 for an illustration of the serial LED shift sequence, Table 3 for LED status Type, and Table 4 for LED mode matrix.

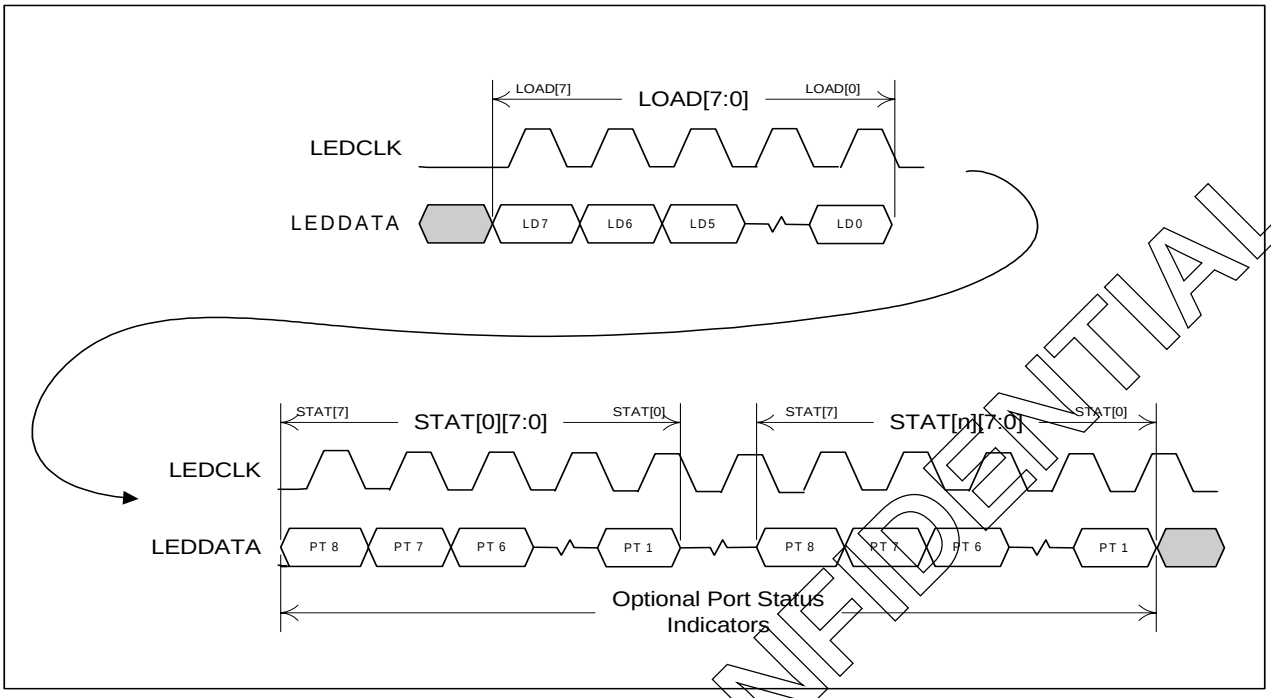


Figure 2: Serial LED Shift Sequence

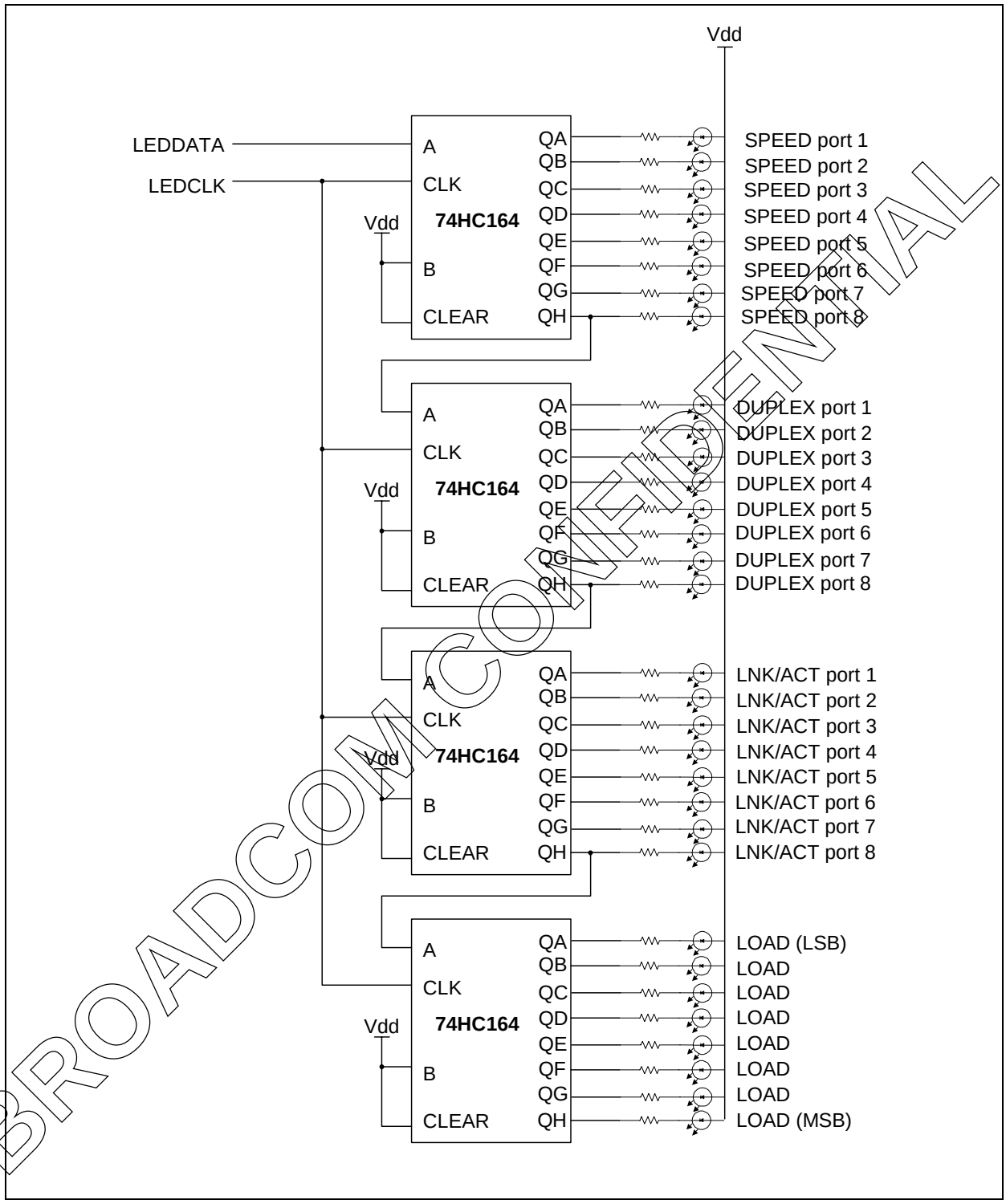


Figure 3: External Circuit for Serial LED Mode

Table 3: LED Status Types

Name	*Description*
LOAD	Bandwidth utilization meter. 8-bit value indicating the percentage of total bandwidth of the switch utilized over a 42 ms interval for packet data.
LNK/ACT	Link and Activity status indicator. Low when link is established. Blinking at 12 Hz when link is up and port is transmitting and receiving.
LNK/ACT/SPD	Link, Activity and Speed indicator. Active when link is up. Blinking at 3 Hz when port is transmitting or receiving in 10 MB mode. Blinking at 12 Hz when port is transmitting or receiving in 100 MB mode.
LNK	Link status indicator. Low when link is established.High when link is off.
DUPLEX	Duplex mode indicator. High for half-duplex or no link, and low for full-duplex and link.
SPEED	Speed indicator. High for 10 Mbps or no link, and low for 100 Mbps and link
ACT	Activity. Low for 42 ms when transmit or receive activity is detected during previous 42 ms interval. High during no activity or no link.
COLSN	Collision. Low for 42 ms when collision is detected during the previous 42 ms interval. High in the absence of collisions or no link.
LEDERR#	Error indication. Internal memory fails self test during power-on reset. Low if failure occurs.

Table 4: LED Mode Matrix (Cont.)

LED Mode [2]	*LED Mode [1]*	*LED Mode [0]*	*LEDA#*	*LEDB#*	*LEDC#*	*Shift Sequence*
0	0	0	LNK/ACT	DUPLEX	SPEED	RESVD (1 bit) LEDERR# (1 bit) LOAD# (8 bits) LNK/ACT (8 bits) DUPLEX (8 bits) SPEED (8 bits)
0	0	1	LNK/ACT/SPD	DUPLEX	-	RESVD (1 bit) LEDERR# (1 bit) LOAD# (8 bits) LNK/ACT/SPD (8 bits) DUPLEX (8 bits)
0	1	0	LNK	ACT	SPEED	RESVD (1 bit) LEDERR# (1 bit) LOAD# (8 bits) LINK (8 bits) ACTIVITY (8 bits) SPEED (8 bits) DUPLEX (8 bits)

Table 4: LED Mode Matrix (Cont.)

LED Mode [2]	LED Mode [1]	LED Mode [0]	LEDA#	LEDB#	LEDC#	Shift Sequence
1	0	0	LNK/ACT	DUPLEX	SPEED	RESVD (1 bit) LEDERR# (1 bit) LOAD# (8 bits) LNK/ACT (8 bits) DUPLEX (8 bits) SPEED (8 bits) COLSN (8 bits)
1	0	1	LNK/ACT/SPD	DUPLEX	COLSN	RESVD (1 bit) LEDERR# (1 bit) LOAD# (8 bits) LNK/ACT/SPD (8 bits) DUPLEX (8 bits) COLSN (8 bits)
1	1	0	LNK	ACT	SPEED	RESVD (1 bit) LEDERR# (1 bit) LOAD# (8 bits) DUPLEX (8 bits) COLLISION (8 bits)

LOAD METER LED

The load meter LEDs provide a bar-graph indication of the percentage of total available bandwidth of the switch utilized by packet data over a periodic interval of 42 ms. The bar-graph scale is shown in Table 5 on page 15. The load meter is valid in both single and expanded systems.

Table 5: Load Meter LED Decode

Load Value Load[7:0]#	Bandwidth (%)
11111111	<0.4 (all LEDs off)
11111110	less than 0.8
11111100	less than 1.6
11111000	less than 3.2
11110000	less than 6.4
11100000	less than 12.8
11000000	less than 25
10000000	less than 50
00000000	>50 (all LED's on)

CONFIGURATION

Configuration of the AC508 takes place during reset by loading internal control values from pins on the device. All of the pins used for initialization are also used as functional pins during normal operation. These pins are configured to default settings with internal pullup or pulldown resistors and must be configured with external pullup or pulldown resistors to change the default value. The value at the pin is loaded when the reset sequence completes and the pin transitions to normal operation.

Section 2: Hardware Signal Definitions

Table 6: Signal Descriptions

Signal Name	Type	Description
MEDIA CONNECTIONS		
RD[1:8]±	I	**Receive Pair.** Differential data from the media is received on the **RD**± signal pair.
TD[1:8]±	O	**Transmit Pair.** Differential data is transmitted to the media on the **TD**± signal pair.
CLOCK/RESET		
XTALI/CK25 XTALO	I O	**25 MHz Crystal/Clock Input.** For a single-ended clock signal input, connect a 25.000 (+/- 50 ppm) MHz reference clock to the CK25 pin. This pin must be driven with a continuous clock. Leave XTALO unconnected for this mode of operation. Alternatively, a 25.000 MHz parallel-resonant crystal can be connected between the XTALI/XTALO pins, with a 27 pF capacitor from each pin to GND. Note that this mode should only be used in a non-expanded system, as all clocks in a multi-chip system require the same source clock.
RST#	I	**Reset.** Active Low. Resets the AC508.
MII/7-WIRE PORT		
TXC	I/O_{PD}	**Transmit Clock.** For MII mode, 25 MHz input in 100BASE-X mode and 2.5 MHz in 10BASE-T mode. This clock must be a continuously driven input, generated from the PHY. This signal becomes the TXC output for 7-wire.
TXD[3:0]	I/O_{PD}	**Transmit Data Output.** Nibble-wide transmit data is output on these pins synchronously to TXC. TXD[3] is the most significant bit. TXD[0] is referenced as TXD during 7-wire mode.
TXEN	I/O_{PD}	**Transmit Enable.** Indicates that the data nibble is valid on TXD[3:0]. TXEN for 7-wire.
TXER	I/O_{PD}	**Transmit Error.** Asserted while TXEN is active to force a bad code into the transmit data stream.
RXC	I/O_{PD}	**Receive Clock.** 25 MHz input in 100BASE-X mode and 2.5 MHz input in 10BASE-T mode. RXC is expected to be continuously running. RXC may have an irregular period when RXDV= 0 at the beginning of a packet. RXC for 7-wire.
RXD[3] RXD[2] RXD[1] RXD[0]	I_{PD} I_{PD} I_{PD} I/O_{PD}	**Receive Data Inputs.** Nibble-wide receive data. RXD[3] is the most significant bit. RXD[0] is referenced as RXD during 7-wire mode.
RXDV	I/O_{PD}	**Receive Data Valid.** Active high. Indicates that a receive frame is in progress, and that the data stream present on the RXD input pins is valid. RXDV for 7-wire.

Note: # = active-low signal; I = input; O = output; I/O = bidirectional; I_{PU} = input w/ internal pull-up; O_{OD} = open-drain output; O_{3S} = three-state output; B = Bias; PWR = power supply; GND = ground

Table 6: Signal Descriptions (Cont.)

Signal Name	Type	Description
RXER	I_{PD}	**Receive Error Detected.** Active high. Indicates that there has been an error during a receive frame.
CRS	I_{PD}	**Carrier Sense.** Active high. Indicates traffic on link.
COL	I/O_{PD}	**Collision Detect.** In half-duplex mode, active high input indicates that a collision has occurred. In full-duplex mode, COL remains low. COL is an asynchronous input signal. In 7-wire mode, acts as output signal COL.
MDIO	I/O_{PD}	**Management Data I/O.** This serial input/output bit is used to read from and write to the MII registers of the internal transceivers. The data value on the MDIO pin is valid and latched on the rising edge of MDC.
MDC	I/O_{PD}	**Management Data Clock.** MDC must be provided to the AC508 as an input to allow MII management functions. Clock frequencies up to 12.5 MHz are supported. If the AC508 detects SCK activity on the SMP, the AC508 will source a 2.5 MHz clock to the external PHY device.
LINK#	I_{PU}	**Link Status Indicator.** Active low indication of the link status of the transceiver connected at the MII port. When low, the link pass condition is indicated.
BIAS		
RDAC	B	**DAC Bias Resistor.** Adjusts the drive level of the transmit DAC. A 1% precision resistor must be connected between the RDAC pin and GND. See Table 16 on page 31 for the required value.
LEDS		
LED[1:9]A# LED[1:9]B# LED[1:9]C#	O	**Per Port LED Indicators.** Refer to Table 3 on page 14 and Table 4 on page 14 for a functional description of these signals.
LEDCLK	O	**LED Shift Clock**. Periodically active to enable the shift of LEDDATA into external registers. Shared with LEDMODE0.
LEDDATA	O	**LED Data Output.** Serial LED data is shifted out when LEDCLK is active. Refer to Table 3 on page 14 and Table 4 on page 14 for a functional description of these signals. Shared with LEDMODE1.
TEST INTERFACE		
CONFIGURATION		
ENFDXFLOW	I_{PU}	**Enable Automatic Full Duplex Flow Control.** In combination with the results of Auto-Negotiation, sets the flow control mode. Refer to Table 1 on page 5 for more information.
ENHDXFLOW	I_{PU}	**Enable Automatic Backpressure.** ENHDXFLOW =0: Half-duplex flow control is disabled. ENHDXFLOW =1: Half-duplex flow control is enabled. Refer to Table 1 on page 5 for more information.

Note: # = active-low signal; I = input; O = output; I/O = bidirectional; I_{PU} = input w/ internal pull-up; O_{OD} = open-drain output; O_{3S} = three-state output; B = Bias; PWR = power supply; GND = ground

Table 6: Signal Descriptions (Cont.)

Signal Name	Type	Description
LEDMODE[2], LEDMODE[1], LEDMODE[0]	I_{PU}, I_{PD}, I_{PD}	**LED Mode.** LEDMODE0 shared with LEDCLK. LEDMODE1 shared with LEDDATA. LEDMODE2 shared with ERDYO. See Table 5 on page 15 for details.
MDIX_DIS	I_{PD}	**HP Auto-MDIX Disable.** MDIX_DIS = 0: Automatic TX cable swap detection enabled. MDIX_DIS = 1: Automatic TX cable swap detection disabled.
MII_FDX#	I_{PD}	**MII Duplex operation.** Sets the duplex setting of the MII port. Can be overridden by software through the MII Port State Override Register. MII_FDX# = 1: MII port operates in half-duplex. MII_FDX# = 0: MII port operates in full-duplex.
MII_SPD100#	I_{PD}	**MII default Speed operation.** Sets the speed setting of the MII port. Can be overridden by software through the MII Port State Override Register. MII_SPD100# = 0: MII port operates at 100 Mb/s. MII_SPD100# = 1: MII port operates at 10 Mb/s.
MII_FLOWCTRL	I_{PD}	**MII Link Partner Flow Control capability.** MII_FLOWCTRL = 0: MII port partner does not support 802.3x flow control in full duplex mode. MII_FLOWCTRL = 1: MII port partner supports 802.3x flow control in full duplex mode.
MII_7WIRE_SEL	I_{PU}	**MII or 7WIRE Interface Selection.** MII_7WIRE_SEL = 0: Configures MII pins to connect to 7 Wire CPU. MII_7WIRE_SEL = 1: Configures MII pins to support connection to an external MII device. Shared with TXD2.
POWER		
VDDC	PWR	**1.8V Digital Core VDD.**
GNDC	GND	**Digital Core GND.**

Note: # = active-low signal; I = input; O = output; I/O = bidirectional; I_{PU} = input w/ internal pull-up; O_{OD} = open-drain output; O_{3S} = three-state output; B = Bias; PWR = power supply; GND = ground

Table 6: Signal Descriptions (Cont.)

Signal Name	Type	Description
VDDP	PWR	**3.3V Digital Periphery (Output Buffer) VDD.**
GNDP	GND	**Digital Periphery (Output Buffer) GND.**
VDDA	PWR	**1.8V Analog VDD.**
GNDA	GND	**Analog GND.**
VDDBIAS	PWR	**3.3V Bias Circuit VDD.**
GNDBIAS	GND	**Bias Circuit GND.**
VDDPLL	PWR	**1.8V PLL Circuit VDD.**
GNDPLL	GND	**PLL Circuit GND.**
VDDXTAL	PWR	**3.3V XTAL VDD.**
GNDXTAL	GND	**XTAL Circuit GND.**

Note: # = active-low signal; I = input; O = output; I/O = bidirectional; I_{PU} = input w/ internal pull-up; O_{OD} = open-drain output; O_{3S} = three-state output; B = Bias; PWR = power supply; GND = ground

Section 3: Pin Assignments

Table 7: Pin Assignment by Pin Number

Pin #	Signal Name
1	GNDA
2	NC
3	NC
4	VDDA
5	GNDA
6	RD1-
7	RD1+
8	GNDA
9	TD1-
10	TD1+
11	GNDA
12	TD2+
13	TD2-
14	GNDA
15	RD2+
16	RD2-
17	GNDA
18	VDDA
19	GNDA
20	VDDA
21	GNDA
22	RD3-
23	RD3+
24	GNDA
25	TD3-
26	TD3+
27	GNDA
28	TD4+
29	TD4-
30	GNDA
31	RD4+
32	RD4-
33	GNDA

Pin #	Signal Name
34	VDDA
35	GNDA
36	VDDC
37	GNDC
38	VDDC
39	GNDC
40	LED1A#
41	LED1B#
42	LED1C#
43	LED2A#
44	LED2B#
45	LED2C#
46	VDDP
47	GNDP
48	LED3A#
49	LED3B#
50	LED3C#
51	LED4A#
52	LED4B#
53	LED4C#
54	VDDBIAS
55	RDAC
56	GNDBIAS
57	VDDPLL
58	VDDXTAL
59	CK25
60	CK25O
61	GNDXTAL
62	GNDPLL
63	VDDA
64	GNDA
65	RD5-
66	RD5+

Pin #	Signal Name
67	GNDA
68	TD5-
69	TD5+
70	GNDA
71	TD6+
72	TD6-
73	GNDA
74	RD6+
75	RD6-
76	GNDA
77	VDDA
78	GNDA
79	GNDA
80	VDDA
81	GNDA
82	RD7-
83	RD7+
84	GNDA
85	TD7-
86	TD7+
87	GNDA
88	TD8+
89	TD8-
90	GNDA
91	RD8+
92	RD8-
93	GNDA
94	VDDA
95	GNDA
96	TEST1
97	TEST0
98	MDIO
99	MDC

Pin #	Signal Name
100	NC
101	NC
102	NC
103	NC
104	LED5A#
105	LED5B#
106	LED5C#
107	LED6A#
108	LED6B#
109	LED6C#
110	VDDP
111	GNDP
112	LED7A#
113	LED7B#
114	LED7C#
115	VDDP
116	GNDP
117	LED8A#
118	LED8B#
119	LED8C#
120	LED9A#
121	LED9B#
122	LED9C#
123	GNDC
124	VDDC
125	VDDC
126	GNDC
127	RST#
128	LEDCLK/LEDMODE0
129	LEDDATA/LEDMODE1
130	NC
131	NC
132	NC
133	NC
134	NC
135	MDIX_DIS
136	VDDP

Pin #	Signal Name
137	GNDP
138	NC
139	NC
140	NC
141	NC
142	NC
143	NC
144	NC
145	ENFDXFLOW
146	VDDP
147	GNDP
148	ENHDXFLOW
149	NC
150	HW_FWDG_EN
151	NC
152	NC
153	NC
154	NC
155	NC
156	LINK#
157	CRS
158	COL
159	TXD3
160	TXD2/MII_7WIRE_SEL
161	TXD1
162	VDDP
163	VDDC
164	GNDC
165	GNDP
166	TXD0
167	TXEN
168	TXC
169	TXER
170	VDDP
171	GNDP
172	RXER
173	RXC

Pin #	Signal Name
174	RXDV
175	RXD0
176	RXD1
177	NC
178	RXD3
179	VDDC
180	GNDC
181	GNDP
182	VDDP
183	NC
184	NC
185	NC
186	NC
187	NC
188	NC
189	VDDC
190	GNDC
191	NC
192	NC
193	NC
194	NC
195	NC
196	NC
197	NC
198	MII_FLOWCTRL
199	VDDP
200	GNDP
201	MII_SPD100#
202	MII_FDX#
203	NC
204	NC
205	NC
206	LEDMODE2
207	NC
208	NC

Table 8: Pin Assignment by Signal Name

Pin #	Signal Name
59	CK25
60	CK25O
158	COL
157	CRS
145	ENFDXFLOW
148	ENHDXFLOW
1	GNDA
5	GNDA
8	GNDA
11	GNDA
14	GNDA
17	GNDA
19	GNDA
21	GNDA
24	GNDA
27	GNDA
30	GNDA
33	GNDA
35	GNDA
64	GNDA
67	GNDA
70	GNDA
73	GNDA
76	GNDA
78	GNDA
79	GNDA
81	GNDA
84	GNDA
87	GNDA
90	GNDA
93	GNDA
95	GNDA
56	GNDBIAS
37	GNDC
39	GNDC
123	GNDC

Pin #	Signal Name
126	GNDC
164	GNDC
180	GNDC
190	GNDC
47	GNDP
111	GNDP
116	GNDP
137	GNDP
147	GNDP
165	GNDP
171	GNDP
181	GNDP
200	GNDP
62	GNDPLL
61	GNDXTAL
150	HW_FWDG_EN
40	LED1A#
41	LED1B#
42	LED1C#
43	LED2A#
44	LED2B#
45	LED2C#
48	LED3A#
49	LED3B#
50	LED3C#
51	LED4A#
52	LED4B#
53	LED4C#
104	LED5A#
105	LED5B#
106	LED5C#
107	LED6A#
108	LED6B#
109	LED6C#
112	LED7A#
113	LED7B#

Pin #	Signal Name
114	LED7C#
117	LED8A#
118	LED8B#
119	LED8C#
120	LED9A#
121	LED9B#
122	LED9C#
128	LEDCLK/LEDMODE0
129	LEDDATA/LEDMODE1
206	LEDMODE2
156	LINK#
99	MDC
98	MDIO
135	MDIX_DIS
202	MII_FDX#
198	MII_FLOWCTRL
201	MII_SPD100#
2	NC
3	NC
100	NC
101	NC
102	NC
103	NC
130	NC
131	NC
132	NC
133	NC
134	NC
138	NC
139	NC
140	NC
141	NC
142	NC
143	NC
144	NC
149	NC

Pin #	Signal Name
151	NC
152	NC
153	NC
154	NC
155	NC
183	NC
184	NC
185	NC
186	NC
187	NC
188	NC
191	NC
192	NC
193	NC
194	NC
195	NC
196	NC
197	NC
203	NC
204	NC
205	NC
207	NC
208	NC
6	RD1-
7	RD1+
16	RD2-
15	RD2+
22	RD3-
23	RD3+
32	RD4-
31	RD4+
65	RD5-
66	RD5+
75	RD6-
74	RD6+
82	RD7-
83	RD7+

Pin #	Signal Name
92	RD8-
91	RD8+
55	RDAC
127	RST#
173	RXC
175	RXD0
176	RXD1
177	RXD2
178	RXD3
174	RXDV
172	RXER
9	TD1-
10	TD1+
13	TD2-
12	TD2+
25	TD3-
26	TD3+
29	TD4-
28	TD4+
68	TD5-
69	TD5+
72	TD6-
71	TD6+
85	TD7-
86	TD7+
89	TD8-
88	TD8+
97	TEST0
96	TEST1
168	TXC
166	TXD0
161	TXD1
160	TXD2/MII_7WIRE_SEL
159	TXD3
167	TXEN
169	TXER
4	VDDA

Pin #	Signal Name
18	VDDA
20	VDDA
34	VDDA
63	VDDA
77	VDDA
80	VDDA
94	VDDA
54	VDDBIAS
36	VDDC
38	VDDC
124	VDDC
125	VDDC
163	VDDC
179	VDDC
189	VDDC
46	VDDP
110	VDDP
115	VDDP
136	VDDP
146	VDDP
162	VDDP
170	VDDP
182	VDDP
199	VDDP
57	VDDPLL
58	VDDXTAL

Section 4: Timing Characteristics

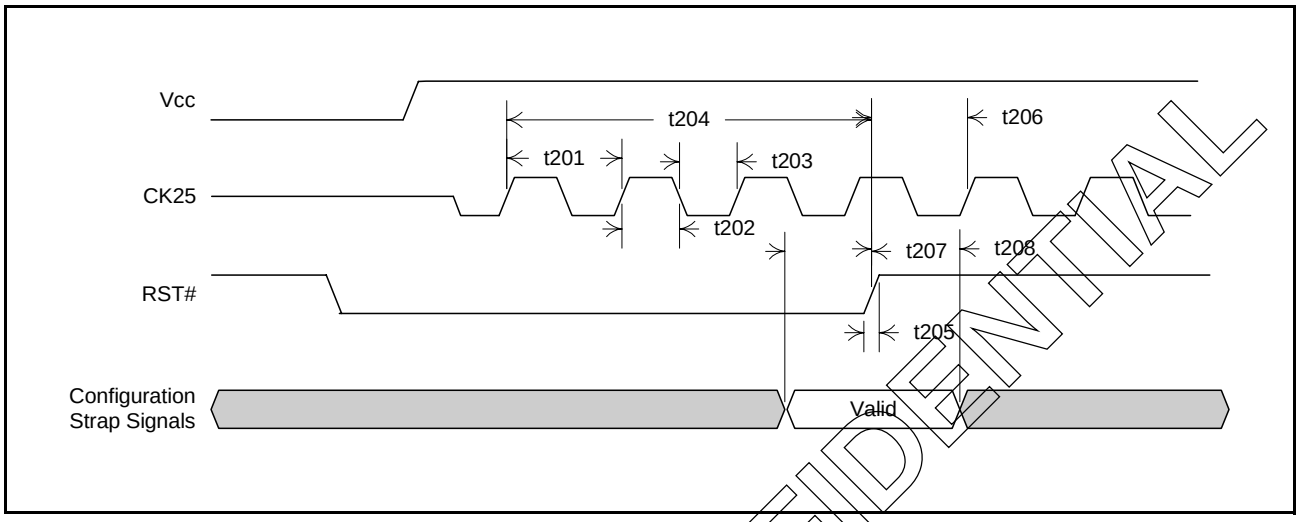


Figure 4: Reset and Clock Timing

Table 9: Reset and Clock Timing

Parameter	*Description*	*Min*	*Typ*	*Max*
t201	CK25 Period	39.998 ns	40 ns	40.002 ns
t202	CK25 High Time	18 ns		22 ns
t203	CK25 Low Time	18 ns		22 ns
t204	RST# Low Pulse Duration	400 ns		
t205	RST# Rise Time			5 ns
t206	RST# Rising Setup to CK25 Rising	10 ns		
t207	Configuration Valid Setup to RST# Rising	100 ns		
t208	Configuration Valid Hold from RST# Rising			0 ns

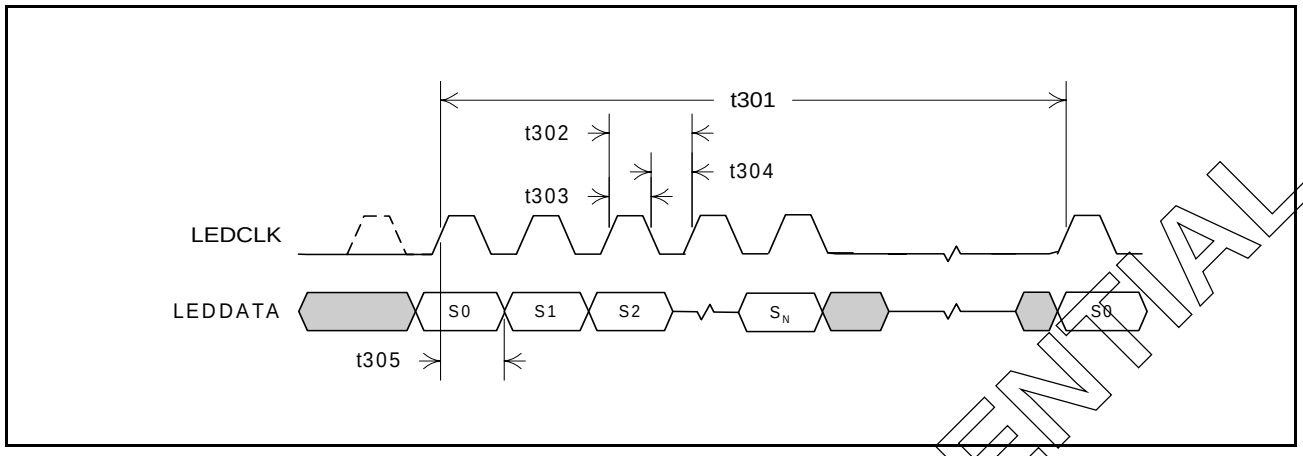


Figure 5: Serial LED Timing

Table 10: Serial LED Timing

Parameter	*Description*	*Min*	*Typ*	*Max*
t301	LED UPDATE CYCLE PERIOD		42 ms	
t302	LEDCLK PERIOD		640 ns	
t303	LEDCLK High Pulse Width	310 ns		330 ns
t304	LEDCLK Low Pulse Width	310 ns		330 ns
t305	LEDCLK to LEDDATA Output Time	270 ns		340 ns

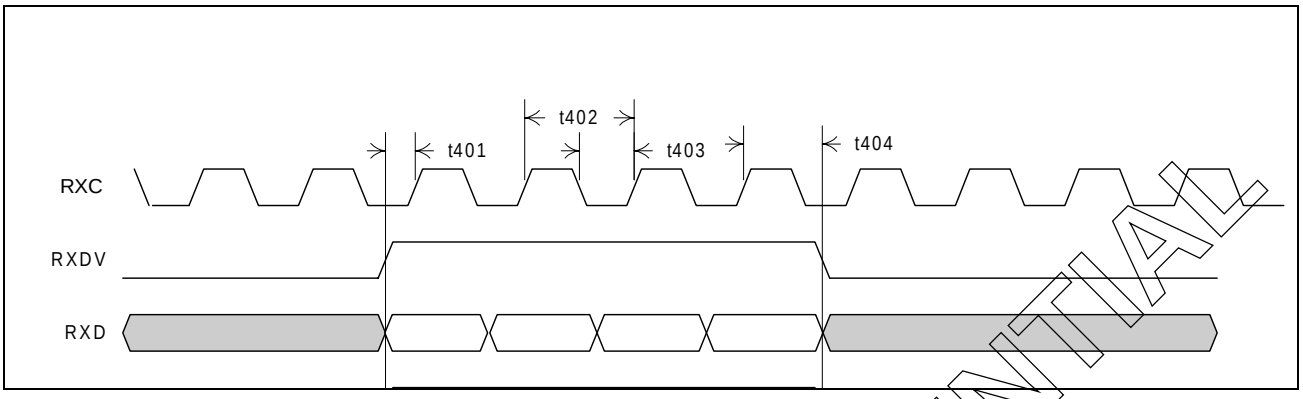


Figure 6: MII Input Timing

Table 11: MII Input Timing

Parameter	*Description*	*Min*	*Typ*	*Max*
t401	RXDV, RXD, RXERR, to RXC Rising Setup Time	10 ns		
t402	RXC Clock Period (10BASE-T mode)		400 ns	
	RXC Clock Period (100BASE-T mode)		40 ns	
t403	RXC High/Low Time (100BASE-T mode)	160 ns		240 ns
	RXC High/Low Time (10BASE-T mode)	14 ns		26 ns
t404	RXDV, RXD, RXERR, to RXC Rising Hold Time			10 ns

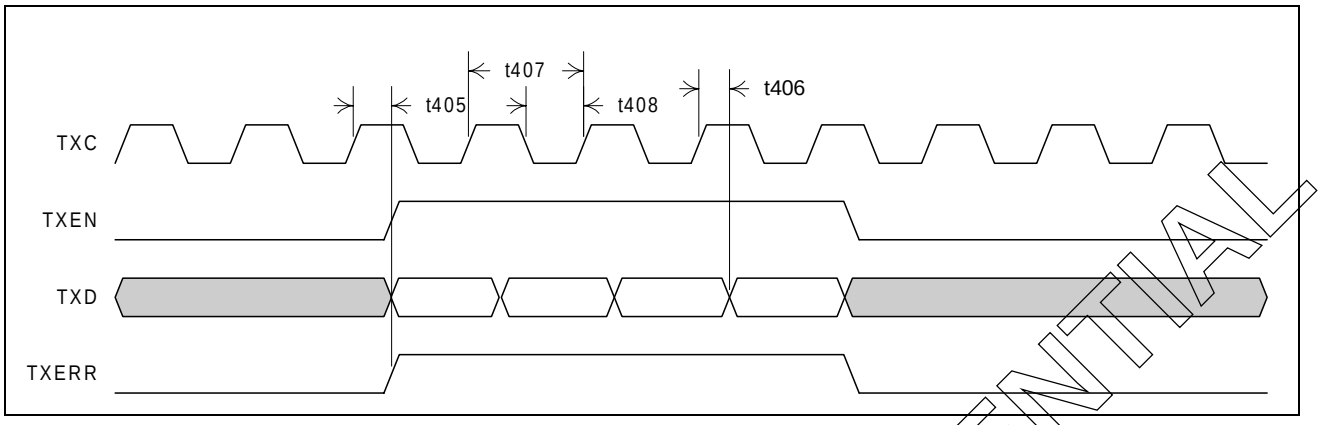


Figure 7: MII Output Timing

Table 12: MII Output Timing

Parameter	*Description*	*Min*	*Typ*	*Max*
t405	TXC High to TXEN, TXD, TXERR Valid			25 ns
t406	TXC High to TXEN, TXD, TXERR Invalid	15 ns		
t407	TXC Clock Period	39.998 ns	40 ns	40.002 ns
t408	TXC High/Low Time	14 ns		26 ns

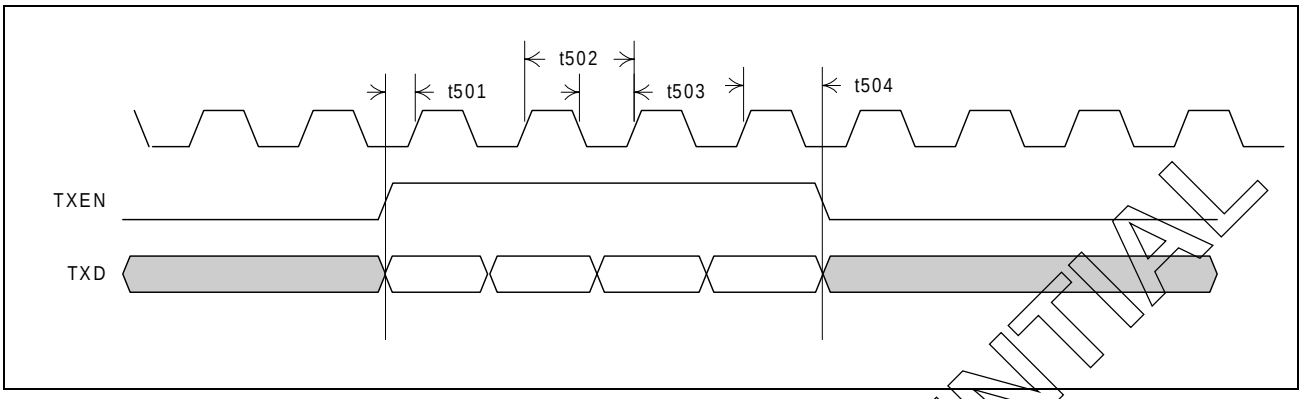


Figure 8: 7-Wire Input Timing

Table 13: 7-Wire Input Timing

Parameter	*Description*	*Min*	*Typ*	*Max*
t501	TXEN, TXD, to TXC Rising Setup Time	20 ns		
t502	TXC Clock Period		100 ns	
t503	TXC High/Low Time	40 ns		60 ns
t504	TXEN, TXD, to TXC Rising Hold Time	0 ns		

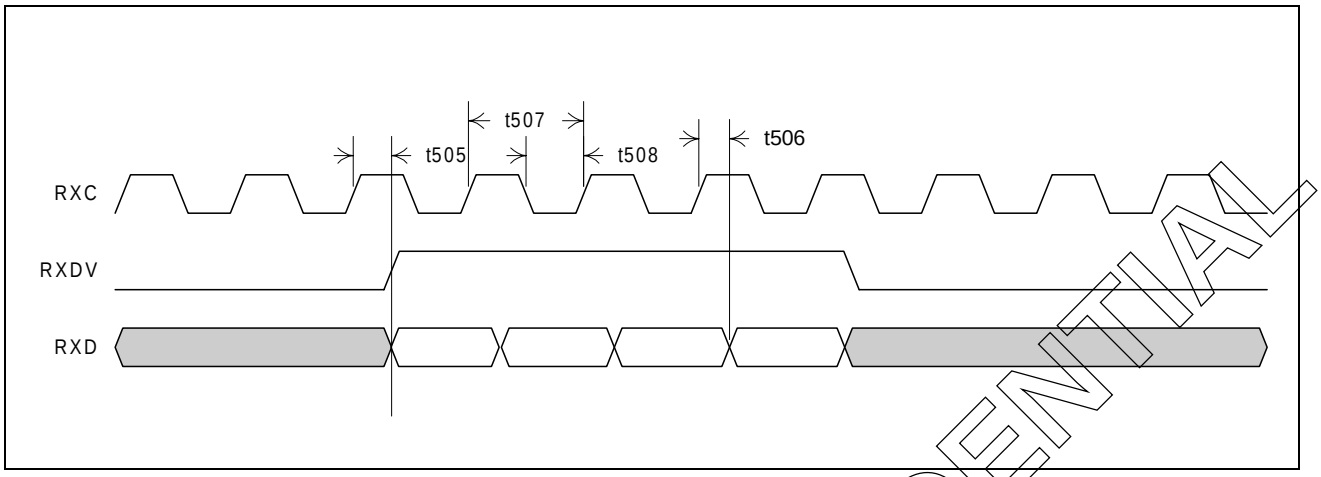


Figure 9: 7-Wire Output Timing

Table 14: 7-Wire Output Timing

Parameter	*Description*	*Min*	*Typ*	*Max*
t505	RXC High to RXDV, RXD Valid			75 ns
t506	RXC High to RXDV, RXD Invalid	40		
t507	RXC Clock Period		100 ns	
t508	RXC High/Low Time	40 ns		60 ns

Section 5: Electrical Characteristics

Table 15: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	Supply Voltage: VDDC, VDDA, VDDPLL	GND – 0.3	1.98	V
V_I	Supply Voltage: VDDP, VDDBIAS, VDDXTAL, Input Voltage	GND – 0.3	3.60	V
I_I	Input Current		±10	mA
T_{STG}	Storage Temperature	–40	+125	°C
V_{ESD}	Electrostatic Discharge		1000	V
Note: These specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect long-term reliability of the device.				

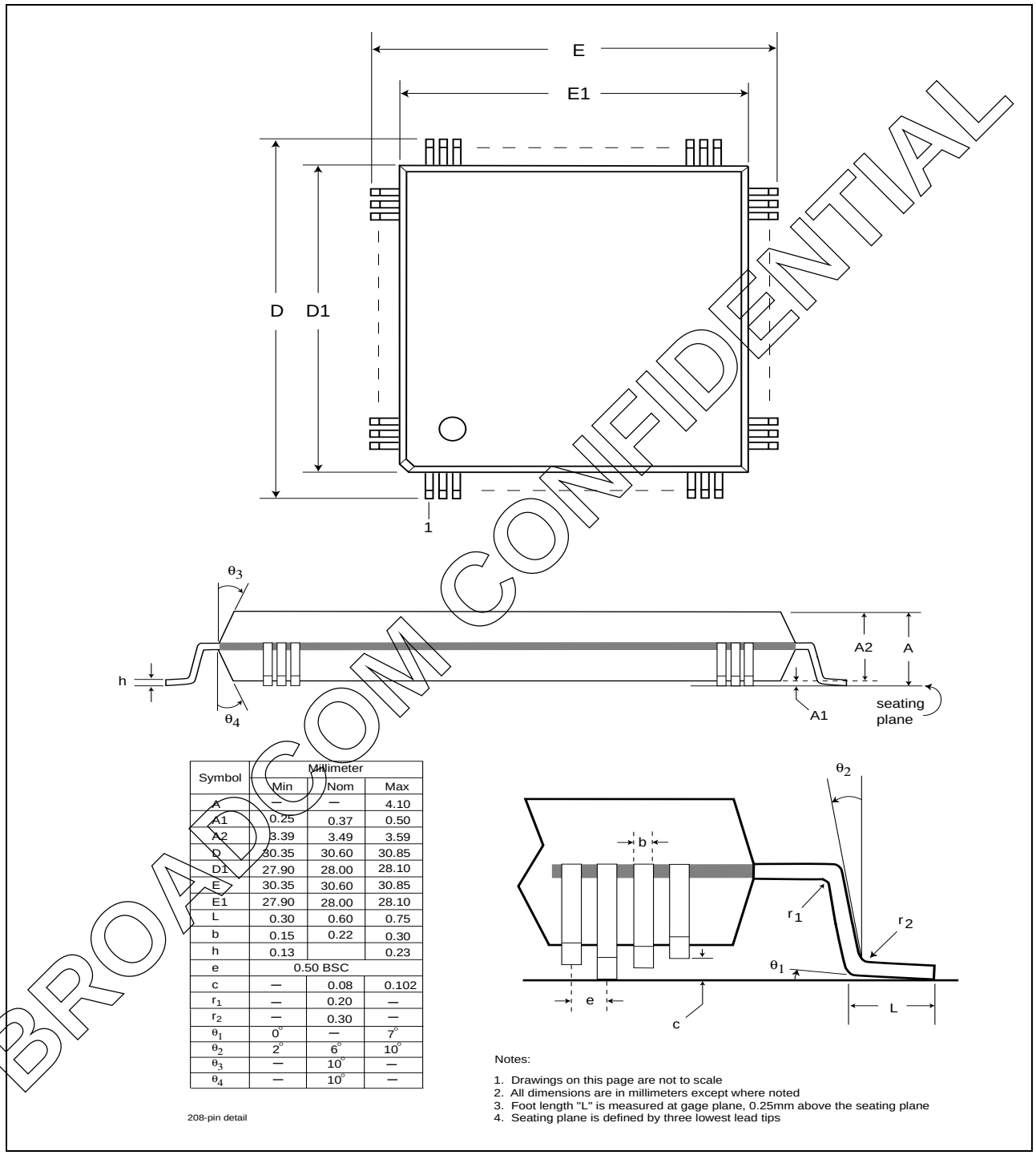
Table 16: Recommended Operating Conditions

Sym	Parameter	Pins	Operating Mode	Min	Max	Units
V_{DD}	Supply Voltage	VDDC, VDDA, VDDPLL		1.71	1.89	V
		VDDXTAL		3.135	3.465	V
		VDDP,VDDBIAS		3.135	3.465	V
V_{IH}	High-Level Input Voltage	All Digital Inputs		2.0		V
V_{IL}	Low-Level Input Voltage	All Digital Inputs			0.8	V
V_{IDIFF}	Differential Input Voltage	RD± {1:8}		150		mV
R_{DAC}	DAC Current-Setting Resistance	RDAC		1.18	1.30	kΩ
T_A	Ambient Operating Temperature			0	70	°C

Table 17: Electrical Characteristics

Sym	Parameter	Pins	Conditions	Min	Typ	Max	Units
$I_{DD1.8}$	Total Supply Current	VDDC, VDDPLL, VDDA	100BASE-TX				A
$I_{DD3.3}$	Total Supply Current	VDDP, VDDBIAS, VDDXTAL	100BASE-TX				A
V_{OH}	High-Level Output Voltage	LEDA#, LEDB#, LEDC#, LEDDATA, LEDCLK	I_{OH} = –5 mA	2.4			V
		TD± {1:8}	driving loaded magnetics module			VDD + 1.5	V
V_{OL}	Low-Level Output Voltage	LEDA#, LEDB#, LEDC#, LEDDATA, LEDCLK	I_{OL} =5 mA			0.4	V
		TD± {1:8}	driving loaded magnetics module	VDD – 1.5			V
I_I	Input Current	Digital Inputs w/ Pull-Up Resistors	V_I = VDDP			+100	µA
			V_I = GND			–200	µA
		Digital Inputs w/ Pull-Down Resistors	V_I = VDDP			+200	µA
			V_I = GND			–10	µA
		All other Digital Inputs	GND ≤ V_I ≤ VDDP			±100	µA
I_{OZ}	High-Impedance Output Current	All Three-state Outputs	GND ≤ V_O ≤ VDDP			±10	µA
		All Open-drain Outputs	V_O = VDDP			+10	µA
V_{BIAS}	Bias Voltage	RDAC		1.18		1.30	V

Section 6: Mechanical Information



Symbol	Millimeter		
	Min	Nom	Max
A	—	—	4.10
A1	0.25	0.37	0.50
A2	3.39	3.49	3.59
D	30.35	30.60	30.85
D1	27.90	28.00	28.10
E	30.35	30.60	30.85
E1	27.90	28.00	28.10
L	0.30	0.60	0.75
b	0.15	0.22	0.30
h	0.13		0.23
e	0.50 BSC		
c	—	0.08	0.102
r_1	—	0.20	—
r_2	—	0.30	—
θ_1	0°	—	7°
θ_2	2°	6°	10°
θ_3	—	10°	—
θ_4	—	10°	—

208-pin detail

Notes:

1. Drawings on this page are not to scale
2. All dimensions are in millimeters except where noted
3. Foot length "L" is measured at gage plane, 0.25mm above the seating plane
4. Seating plane is defined by three lowest lead tips

Figure 10: 208-MQFP Package Outline Drawing

Section 7: Ordering Information

Part Number	*Package*	*Ambient Temperature*
AC508(rev*)KQM	208-MQFP	0 –70 °C (with suitable heat sink and airflow)

* = Initial revision of silicon = A0 as of 8/6/01

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