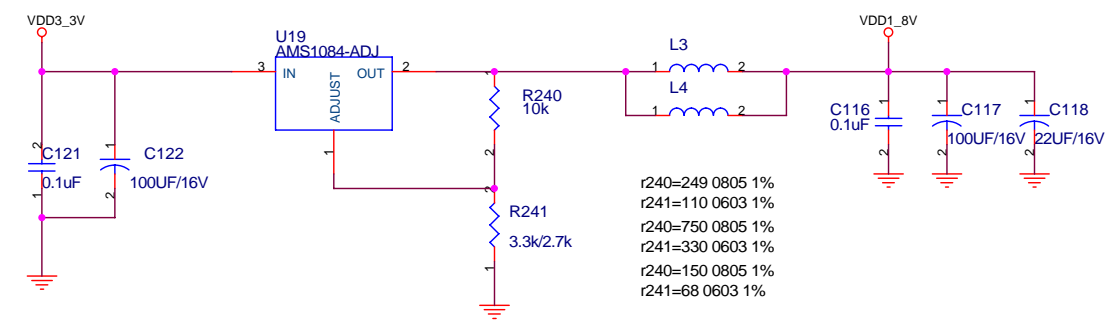
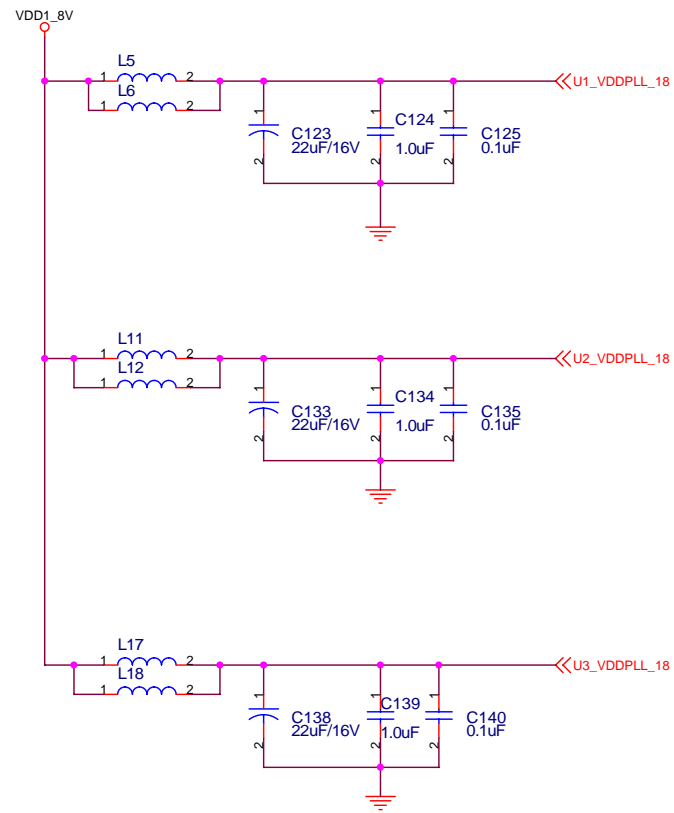
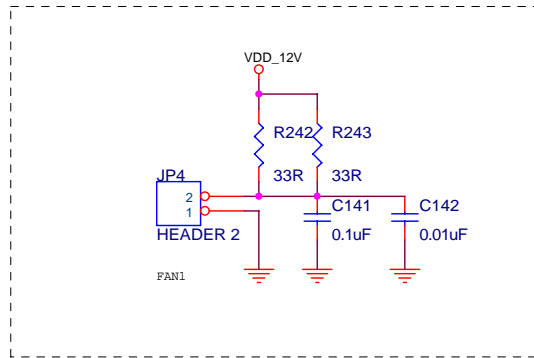
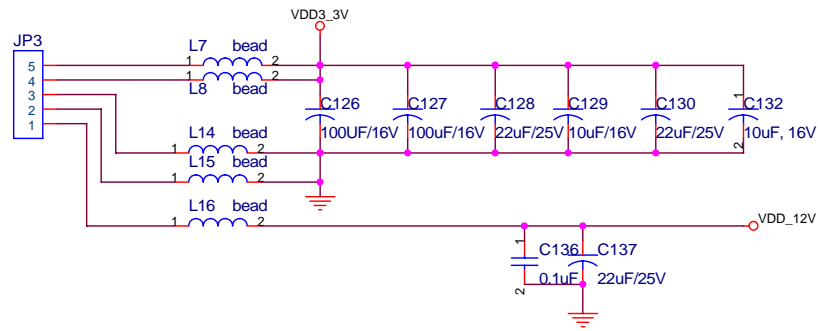


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 r239=110 0603 1%
 r238=750 0805 1%
 r239=330 0603 1%
 r238=150 0805 1%
 r239=68 0603 1%



r240=249 0805 1%
 r241=110 0603 1%
 r240=750 0805 1%
 r241=330 0603 1%
 r240=150 0805 1%
 r241=68 0603 1%

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FILTERED 1.8V PLL POWER SUPPLIES

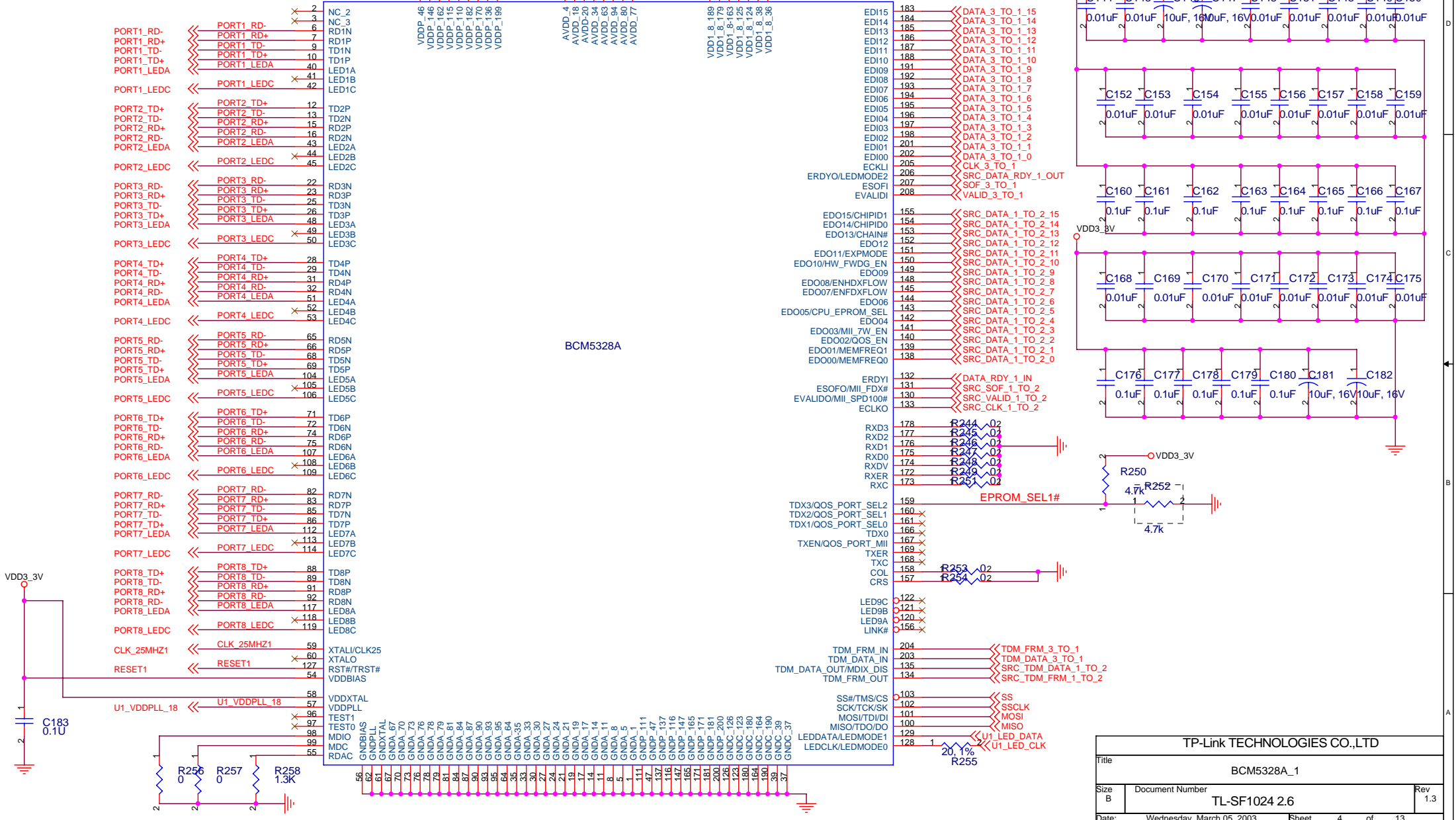
TP-Link TECHNOLOGIES CO.,LTD		
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LED MODE[2:0]=000
 LEDA--LIK/ACT
 LEDB--DUPLEX
 LEDC--SPEED

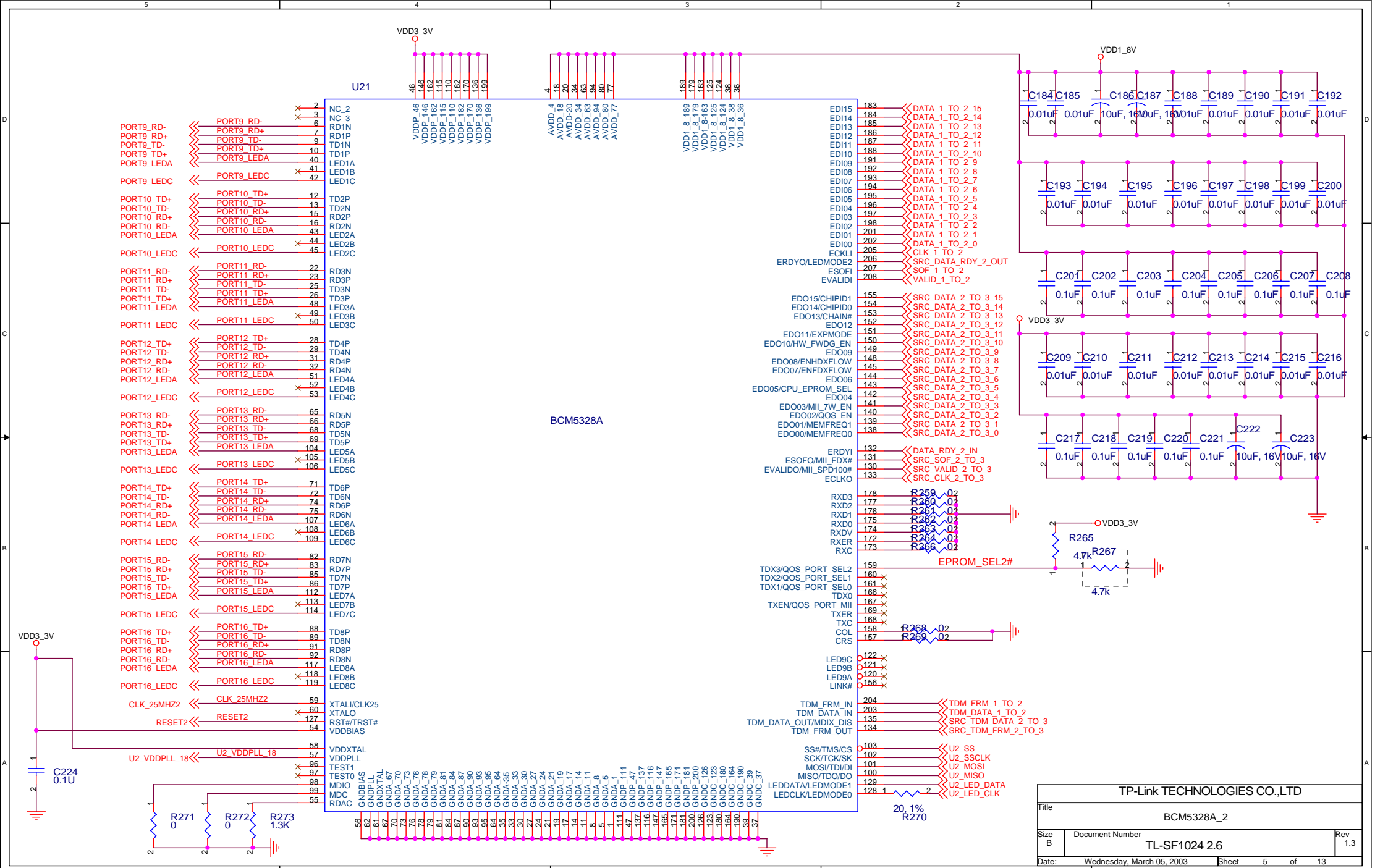
U20

VDD3_3V

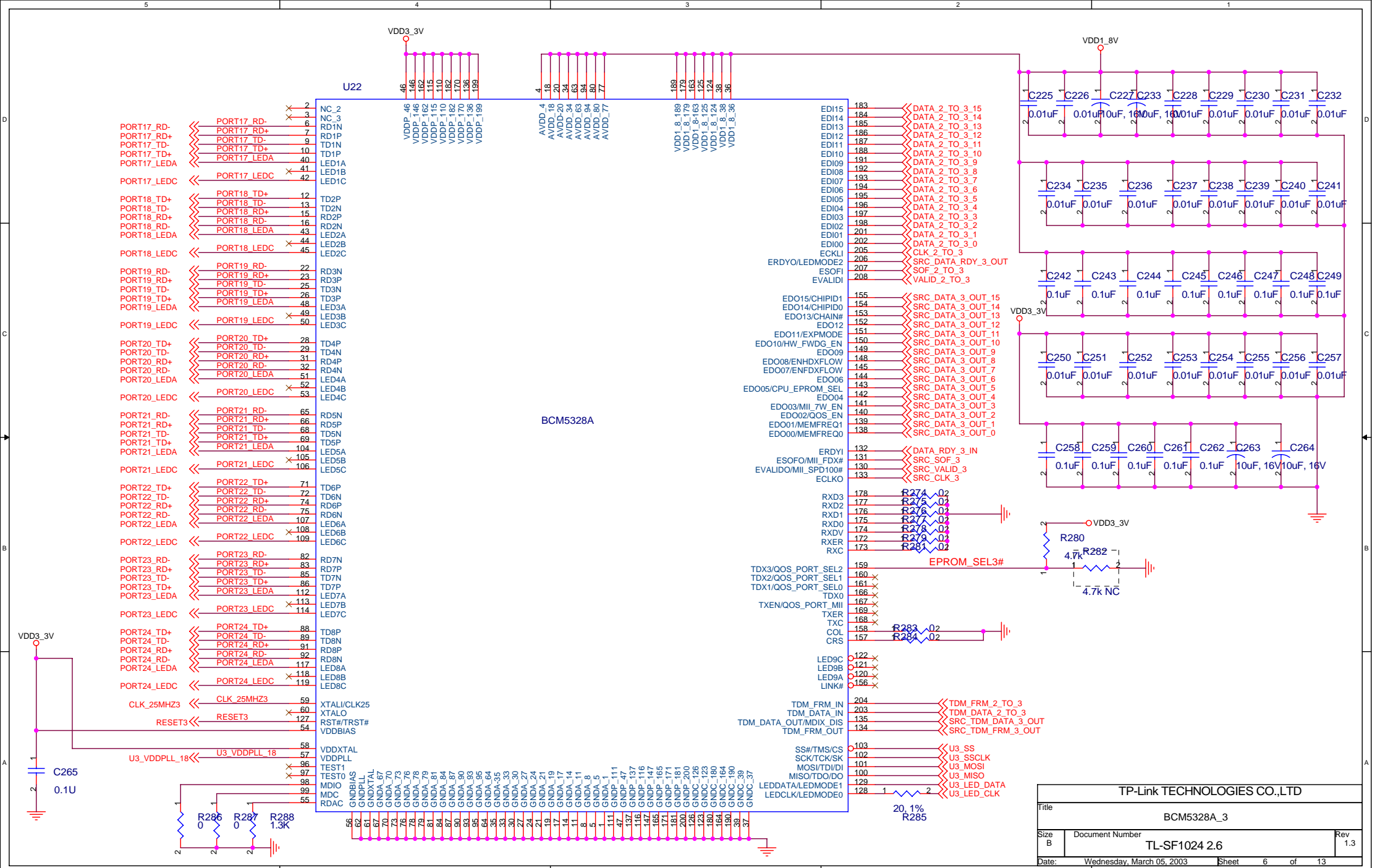
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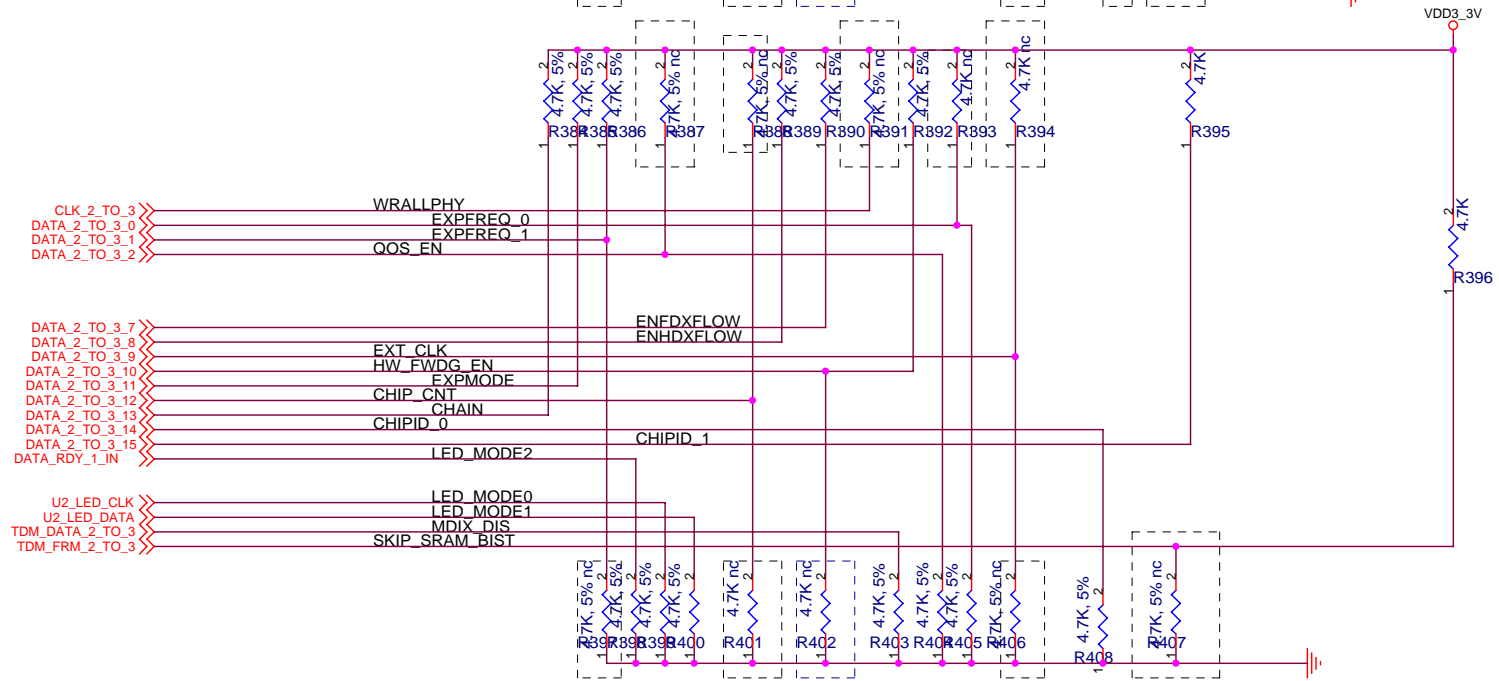
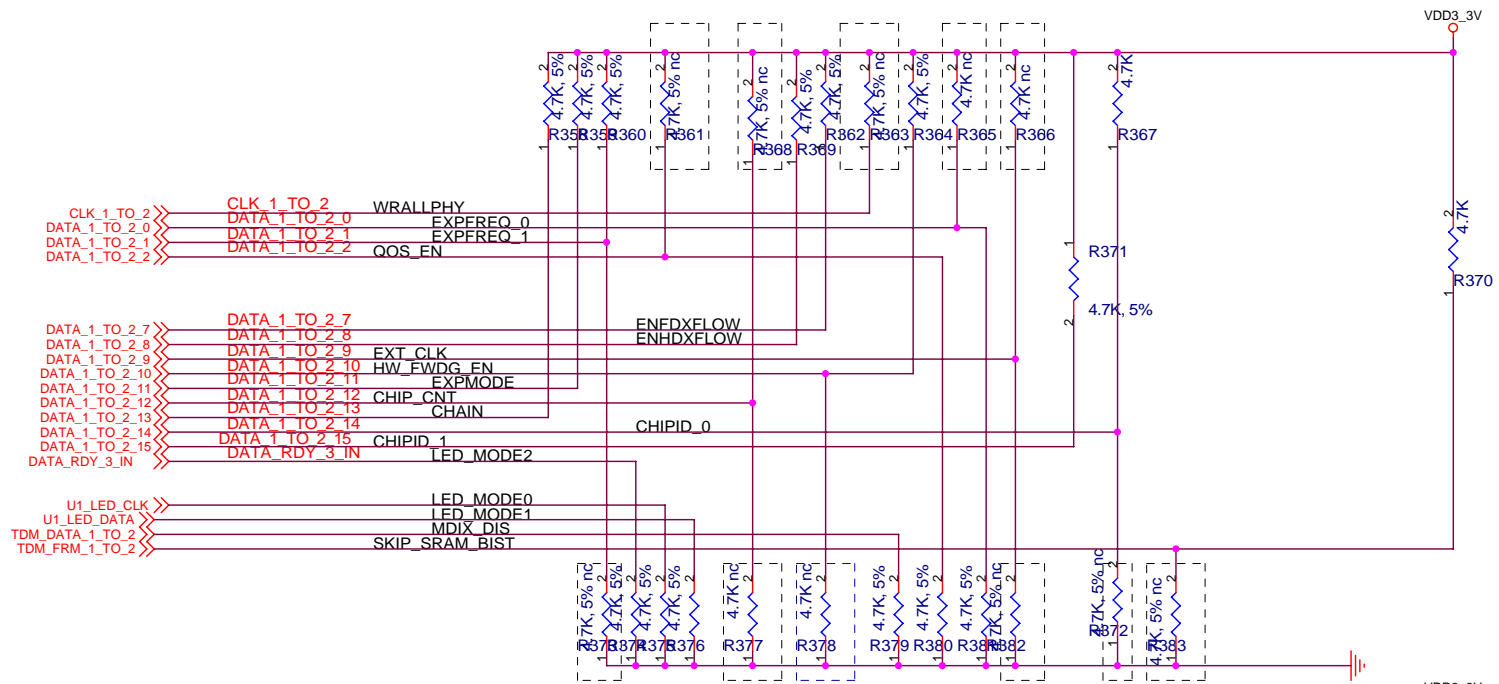
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SRC_DATA_1_TO_2_15 >> 20.1% 1 <<> R289 <<> DATA_1_TO_2_15
 SRC_DATA_1_TO_2_14 >> 20.1% 1 <<> R290 <<> DATA_1_TO_2_14
 SRC_DATA_1_TO_2_13 >> 20.1% 1 <<> R291 <<> DATA_1_TO_2_13
 SRC_DATA_1_TO_2_12 >> 20.1% 1 <<> R292 <<> DATA_1_TO_2_12
 SRC_DATA_1_TO_2_11 >> 20.1% 1 <<> R293 <<> DATA_1_TO_2_11
 SRC_DATA_1_TO_2_10 >> 20.1% 1 <<> R294 <<> DATA_1_TO_2_10
 SRC_DATA_1_TO_2_9 >> 20.1% 1 <<> R295 <<> DATA_1_TO_2_9
 SRC_DATA_1_TO_2_8 >> 20.1% 1 <<> R296 <<> DATA_1_TO_2_8
 SRC_DATA_1_TO_2_7 >> 20.1% 1 <<> R297 <<> DATA_1_TO_2_7
 SRC_DATA_1_TO_2_6 >> 20.1% 1 <<> R298 <<> DATA_1_TO_2_6
 SRC_DATA_1_TO_2_5 >> 20.1% 1 <<> R299 <<> DATA_1_TO_2_5
 SRC_DATA_1_TO_2_4 >> 20.1% 1 <<> R300 <<> DATA_1_TO_2_4
 SRC_DATA_1_TO_2_3 >> 20.1% 1 <<> R301 <<> DATA_1_TO_2_3
 SRC_DATA_1_TO_2_2 >> 20.1% 1 <<> R302 <<> DATA_1_TO_2_2
 SRC_DATA_1_TO_2_1 >> 20.1% 1 <<> R303 <<> DATA_1_TO_2_1
 SRC_DATA_1_TO_2_0 >> 20.1% 1 <<> R304 <<> DATA_1_TO_2_0
 SRC_DATA_RDY_1_OUT >> 20.1% 1 <<> R305 <<> DATA_RDY_3_IN
 SRC_SOF_1_TO_2 >> 20.1% 1 <<> R306 <<> SOF_1_TO_2
 SRC_VALID_1_TO_2 >> 20.1% 1 <<> R307 <<> VALID_1_TO_2
 SRC_CLK_1_TO_2 >> 20.1% 1 <<> R308 <<> CLK_1_TO_2
 SRC_TDM_DATA_1_TO_2 >> 20.1% 1 <<> R309 <<> TDM_DATA_1_TO_2
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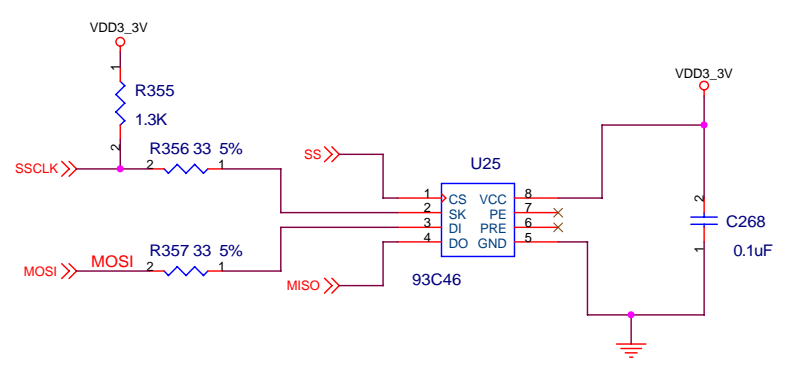
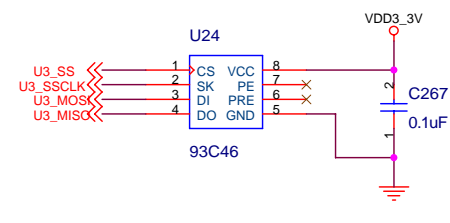
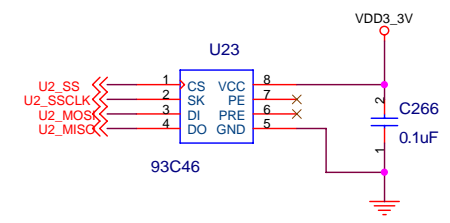
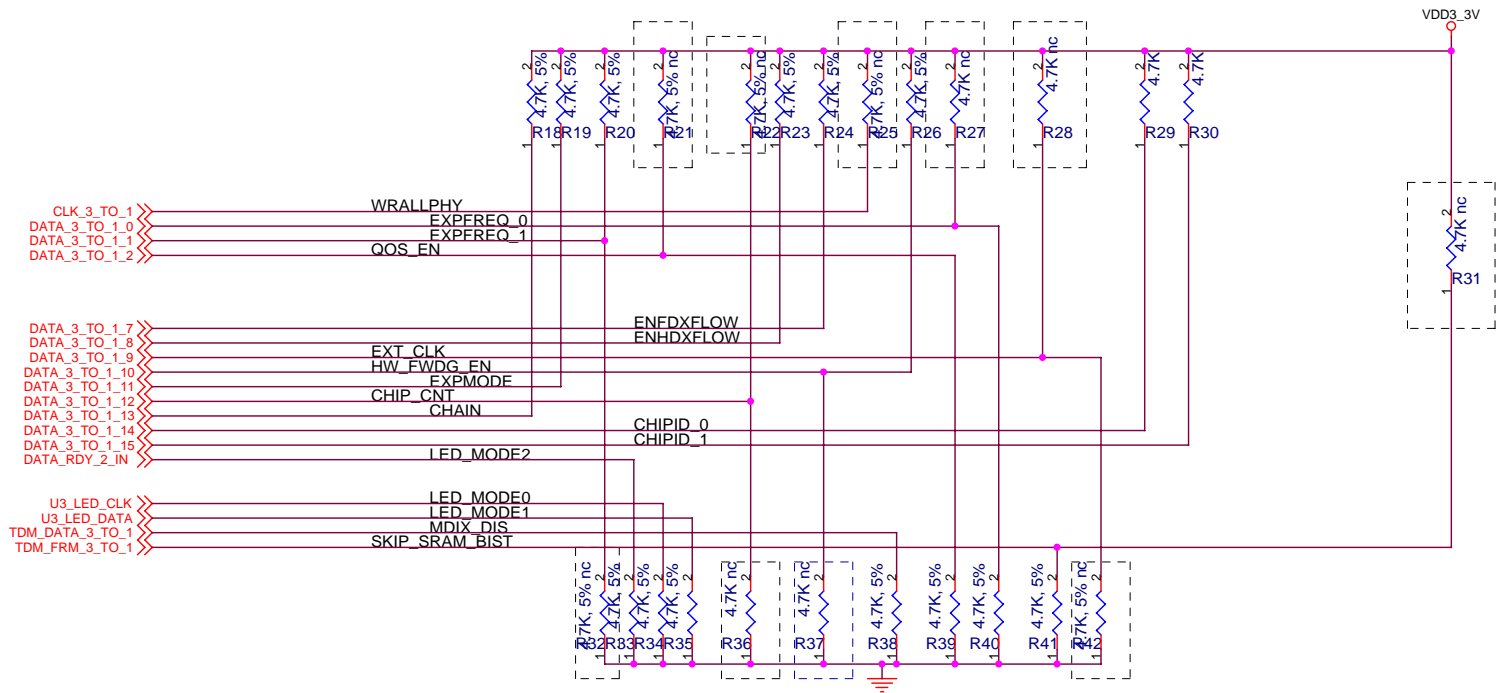
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 SRC_DATA_2_TO_3_12 >> 20.1% 1 <<> R314 <<> DATA_2_TO_3_12
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 SRC_DATA_2_TO_3_9 >> 20.1% 1 <<> R317 <<> DATA_2_TO_3_9
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 SRC_DATA_2_TO_3_3 >> 20.1% 1 <<> R323 <<> DATA_2_TO_3_3
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 SRC_DATA_2_TO_3_0 >> 20.1% 1 <<> R326 <<> DATA_2_TO_3_0
 SRC_DATA_RDY_2_OUT >> 20.1% 1 <<> R327 <<> DATA_RDY_1_IN
 SRC_SOF_2_TO_3 >> 20.1% 1 <<> R328 <<> SOF_2_TO_3
 SRC_VALID_2_TO_3 >> 20.1% 1 <<> R329 <<> VALID_2_TO_3
 SRC_CLK_2_TO_3 >> 20.1% 1 <<> R330 <<> CLK_2_TO_3
 SRC_TDM_DATA_2_TO_3 >> 20.1% 1 <<> R331 <<> TDM_DATA_2_TO_3
 SRC_TDM_FRM_2_TO_3 >> 20.1% 1 <<> R332 <<> TDM_FRM_2_TO_3

SRC_DATA_3_OUT_15 >> 20.1% 1 <<> R333 <<> DATA_3_TO_1_15
 SRC_DATA_3_OUT_14 >> 20.1% 1 <<> R334 <<> DATA_3_TO_1_14
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 SRC_DATA_3_OUT_12 >> 20.1% 1 <<> R336 <<> DATA_3_TO_1_12
 SRC_DATA_3_OUT_11 >> 20.1% 1 <<> R337 <<> DATA_3_TO_1_11
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 SRC_DATA_3_OUT_8 >> 20.1% 1 <<> R340 <<> DATA_3_TO_1_8
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 SRC_DATA_3_OUT_3 >> 20.1% 1 <<> R345 <<> DATA_3_TO_1_3
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 SRC_SOF_3 >> 20.1% 1 <<> R350 <<> SOF_3_TO_1
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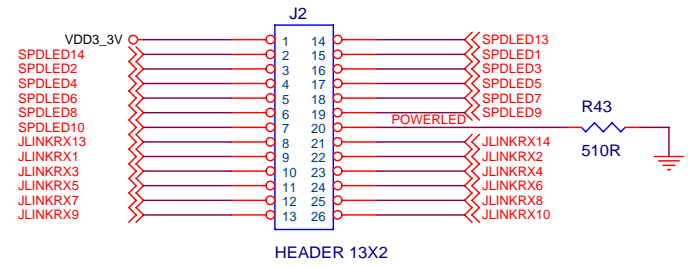
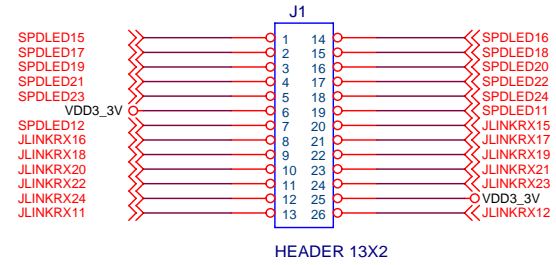
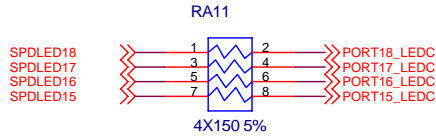
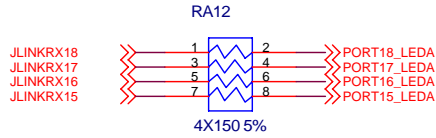
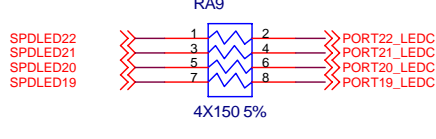
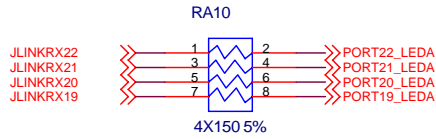
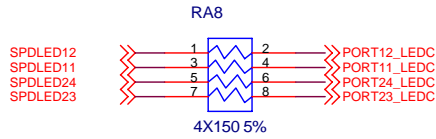
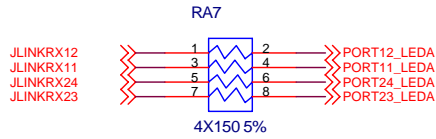
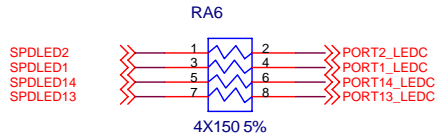
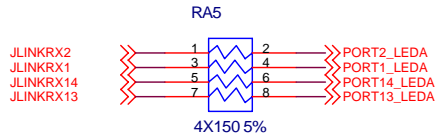
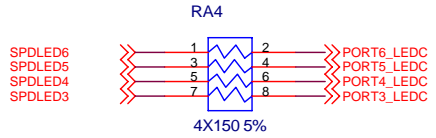
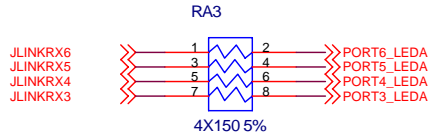
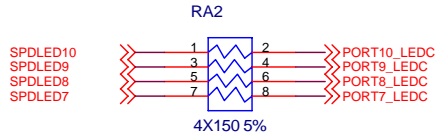
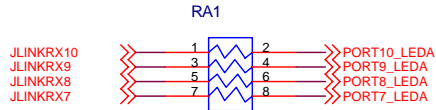
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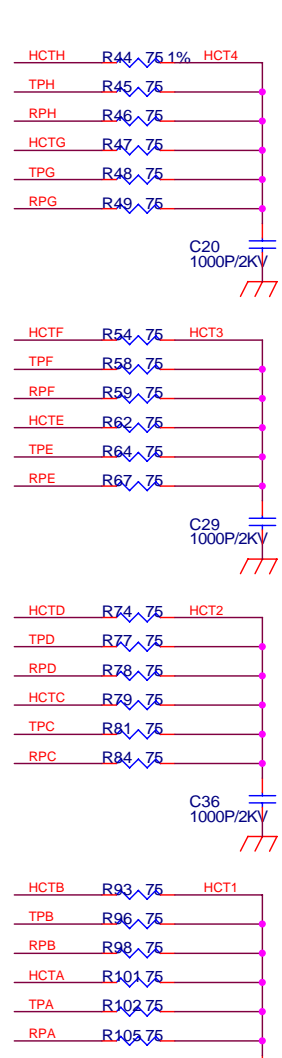
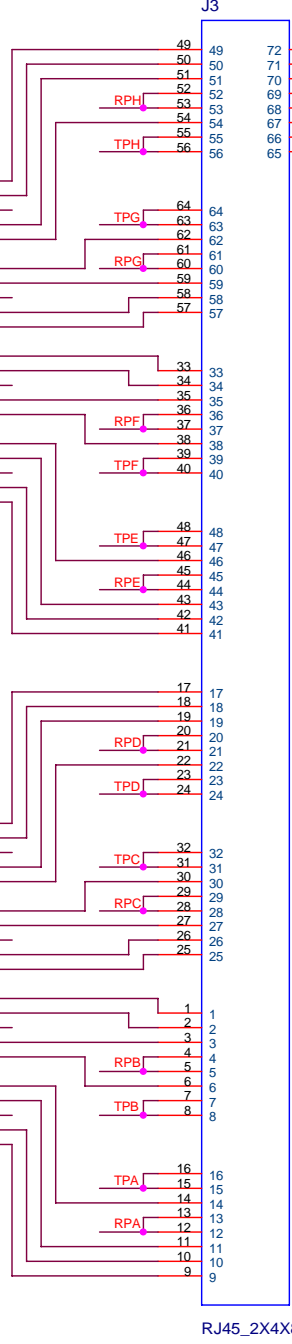
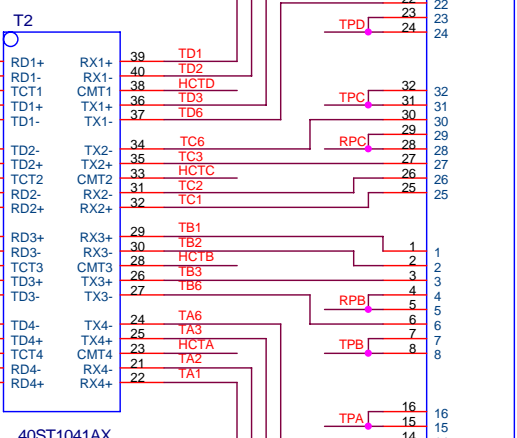
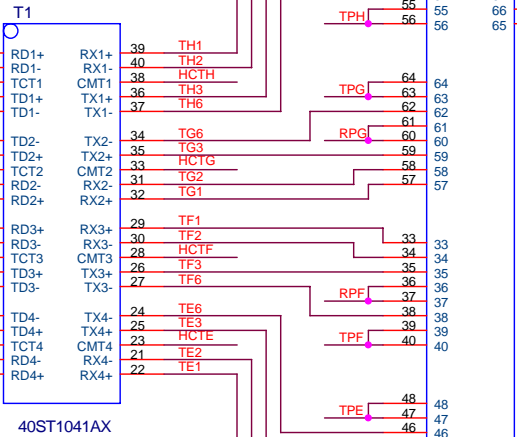
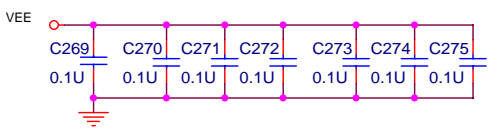
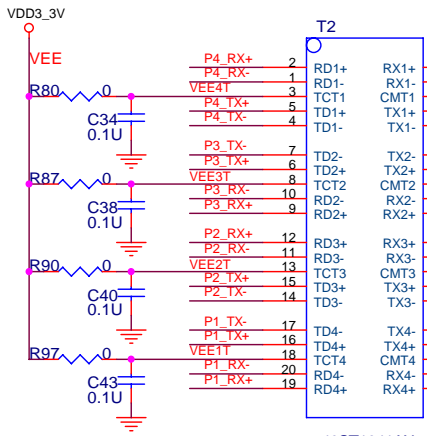
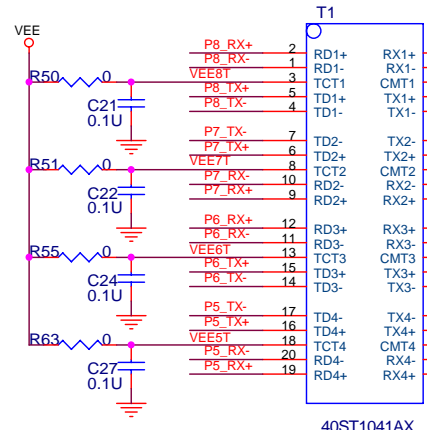
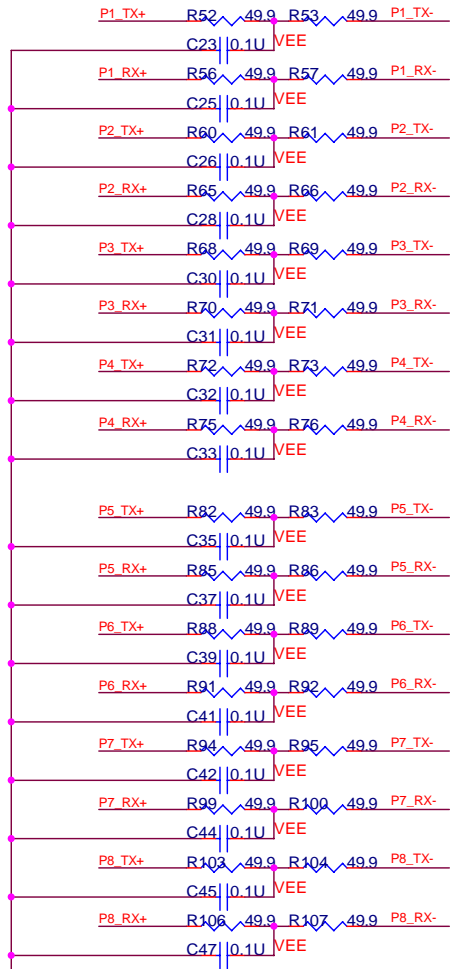
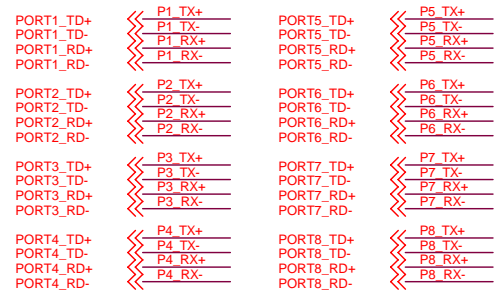
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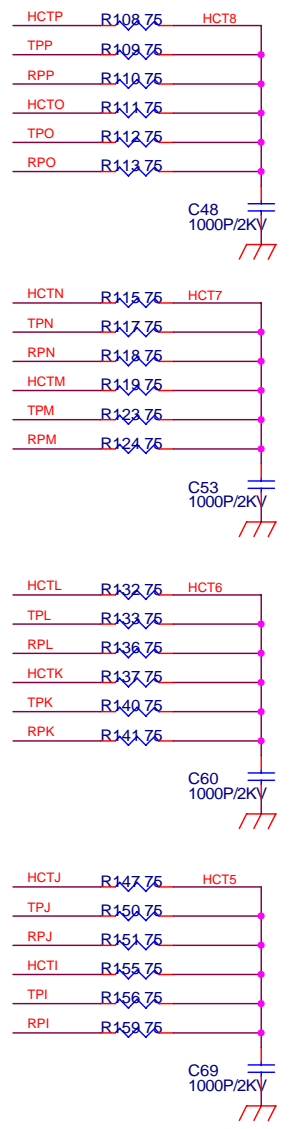
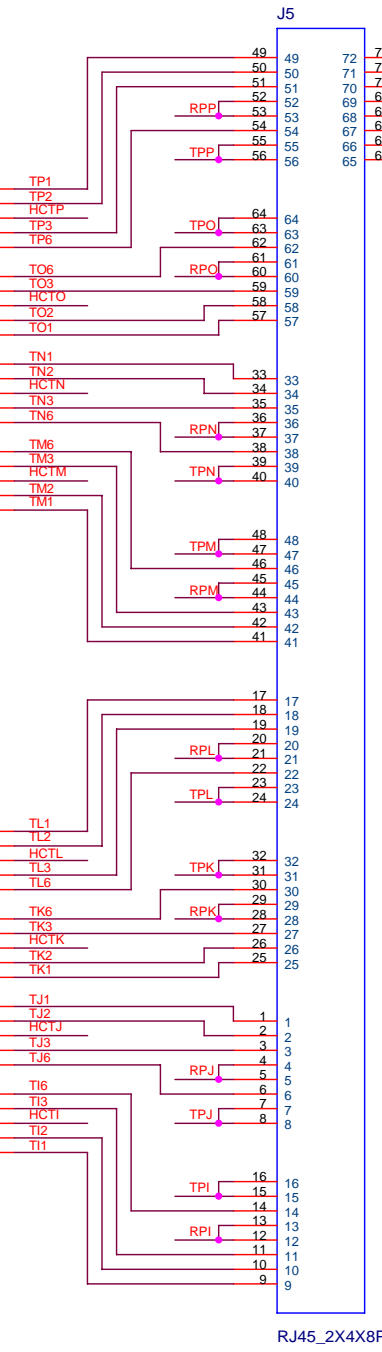
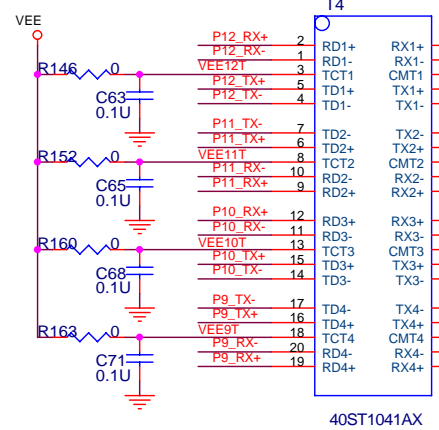
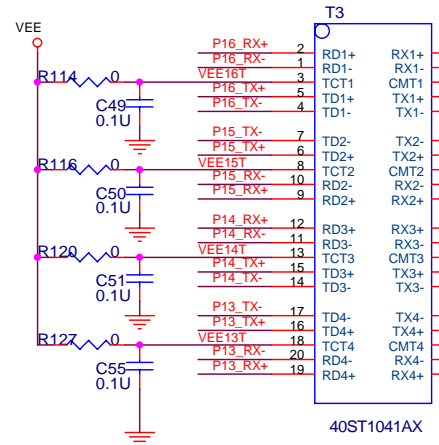
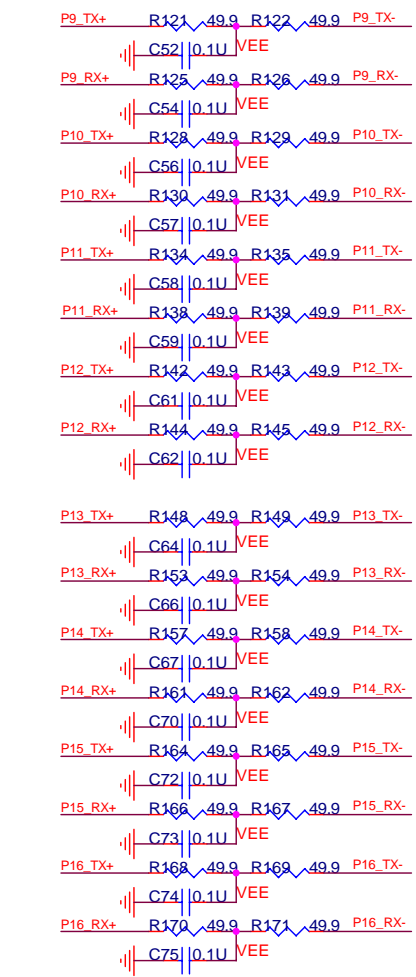
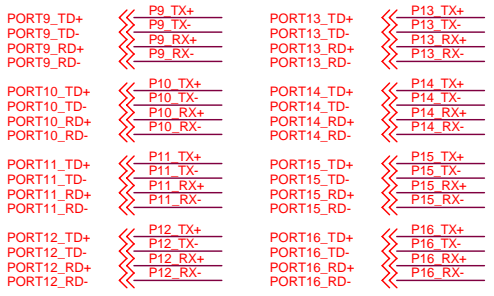
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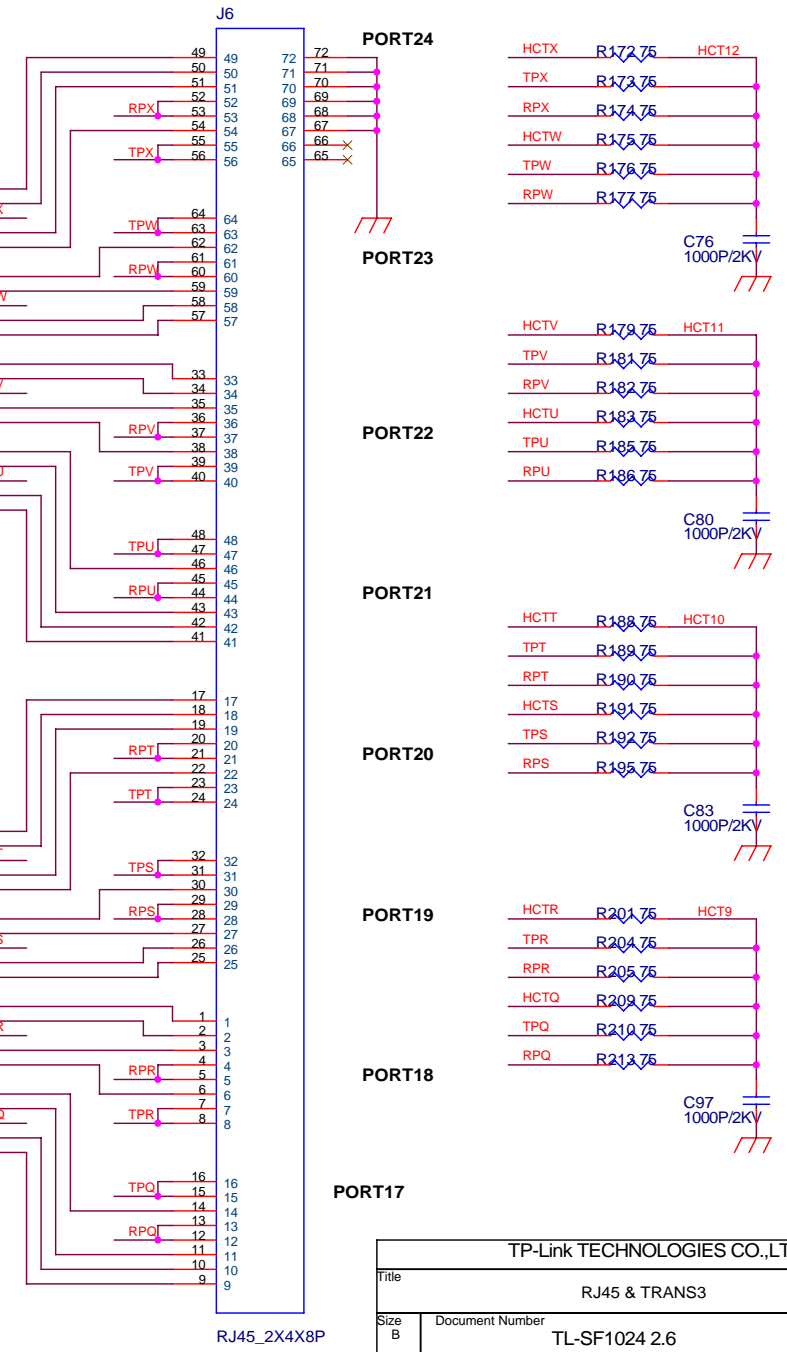
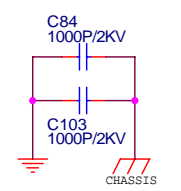
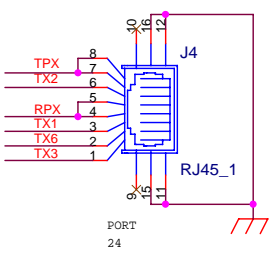
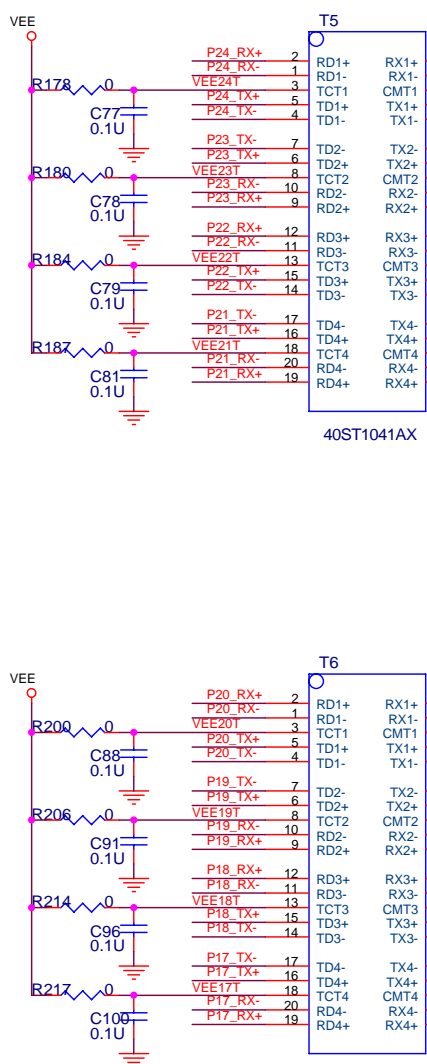
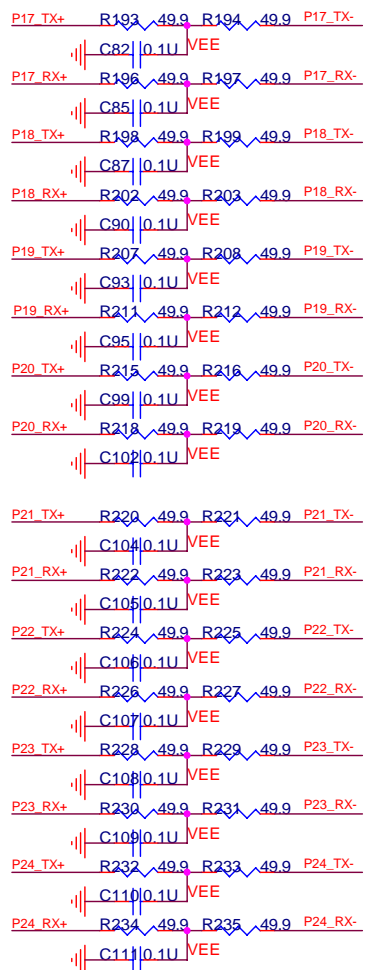
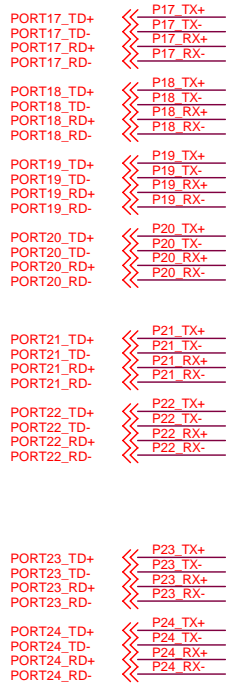
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