



# N-Channel Depletion-Mode DMOS FET

## Features

- ▶ Free from secondary breakdown
- ▶ Low power drive requirement
- ▶ Ease of paralleling
- ▶ Excellent thermal stability
- ▶ Integral source-drain diode
- ▶ High input impedance and low  $C_{ISS}$
- ▶ ESD gate protection

## Applications

- ▶ Solid state relays
- ▶ Normally-on switches
- ▶ Converters
- ▶ Power supply circuits
- ▶ Constant current sources
- ▶ Input protection circuits

## General Description

The LND150 is a high voltage N-channel depletion mode (normally-on) transistor utilizing Supertex's lateral DMOS technology. The gate is ESD protected.

The LND150 is ideal for high voltage applications in the areas of normally-on switches, precision constant current sources, voltage ramp generation and amplification.

## Ordering Information

Device	Package Options			$BV_{DSX}/BV_{DGX}$ (V)	$R_{DS(ON)}$ (max) (K $\Omega$ )	$I_{DSS}$ (min) (mA)
	TO-236AB (SOT-23)	TO-92	TO-243AA (SOT-89)			
LND150	LND150K1-G	LND150N3-G	LND150N8-G	500	1.0	1.0

-G indicates package is RoHS compliant ('Green')



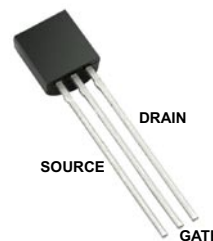
## Absolute Maximum Ratings

Parameter	Value
Drain-to-source	$BV_{DSX}$
Drain-to-gate	$BV_{DGX}$
Gate-to-source	$\pm 20V$
Operating and storage temperature	$-55^{\circ}C$ to $+150^{\circ}C$
Soldering temperature*	$300^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

\* Distance of 1.6mm from case for 10 seconds.

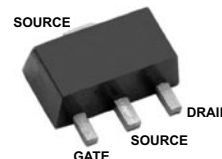
## Pin Configurations



TO-92 (N3)



TO-236AB (SOT-23) (K1)



TO-243AA (SOT-89) (N8)

## Product Marking

**NDEW** W = Code for Week Sealed  
\_\_\_\_\_ = "Green" Packaging

TO-236AB (SOT-23) (K1)

**SiLN** YY = Year Sealed  
**D 1 5 0** WW = Week Sealed  
**YYWW** \_\_\_\_\_ = "Green" Packaging

TO-92 (N3)

**LN1EW** W = Code for Week Sealed  
\_\_\_\_\_ = "Green" Packaging

TO-243AA (SOT-89) (N8)

Packages may or may not include the following marks: Si or

### Thermal Characteristics

Package	$I_D$ (continuous) <sup>†</sup> (mA)	$I_D$ (pulsed) (mA)	Power Dissipation @ $T_A = 25^\circ\text{C}$ (W)	$\theta_{jc}$ ( $^\circ\text{C}/\text{W}$ )	$\theta_{ja}$ ( $^\circ\text{C}/\text{W}$ )	$I_{DR}$ (mA)	$I_{DRM}$ <sup>†</sup> (mA)
TO-236AB (SOT-23)	13	30	0.36	200	350	13	30
TO-92	30	30	0.74	125	170	30	30
TO-243AA (SOT-89)	30	30	1.6 <sup>‡</sup>	15	78	30	30

**Notes:**

- <sup>†</sup>  $I_D$  (continuous) is limited by max rated  $T_f$ .
- <sup>‡</sup> Mounted on FR4 board, 25mm x 25mm x 1.57mm

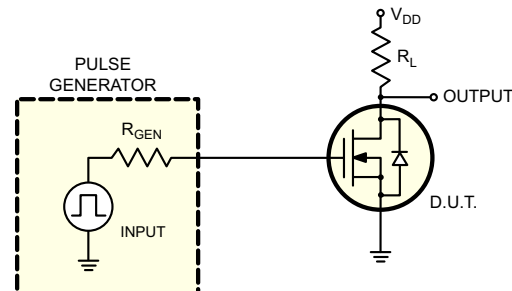
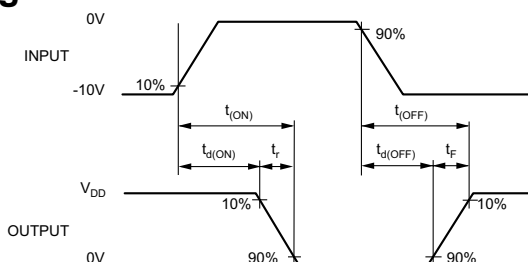
### Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$BV_{DSX}$	Drain-to-source breakdown voltage	500	-	-	V	$V_{GS} = -10\text{V}, I_D = 1.0\text{mA}$
$V_{GS(OFF)}$	Gate-to-source off voltage	-1.0	-	-3.0	V	$V_{GS} = 25\text{V}, I_D = 100\text{nA}$
$\Delta V_{GS(OFF)}$	Change in $V_{GS(OFF)}$ with temperature	-	-	5.0	mV/ $^\circ\text{C}$	$V_{GS} = 25\text{V}, I_D = 100\text{nA}$
$I_{GSS}$	Gate body leakage current	-	-	100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
$I_{D(OFF)}$	Drain-to-source leakage current	-	-	100	nA	$V_{GS} = -10\text{V}, V_{DS} = 450\text{V}$
		-	-	100	$\mu\text{A}$	$V_{DS} = 0.8\text{V Max Rating}, V_{GS} = -10\text{V}, T_A = 125^\circ\text{C}$
$I_{DSS}$	Saturated drain-to-source current	1.0	-	3.0	mA	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	850	1000	$\Omega$	$V_{GS} = 0\text{V}, I_D = 0.5\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.2	%/ $^\circ\text{C}$	$V_{GS} = 0\text{V}, I_D = 0.5\text{mA}$
$G_{FS}$	Forward transconductance	1.0	2.0	-	m $\Omega$	$V_{DS} = 0\text{V}, I_D = 1.0\text{mA}$
$C_{ISS}$	Input capacitance	-	7.5	10	pF	$V_{GS} = -10\text{V}, V_{DS} = 25\text{V}, f = 1.0\text{MHz}$
$C_{OSS}$	Common source output capacitance	-	2.0	3.5		
$C_{RSS}$	Reverse transfer capacitance	-	0.5	1.0		
$t_{d(ON)}$	Turn-on delay time	-	0.09	-	$\mu\text{s}$	$V_{DD} = 25\text{V}, I_D = 1.0\text{mA}, R_{GEN} = 25\Omega$
$t_r$	Rise time	-	0.45	-		
$t_{d(OFF)}$	Turn-off delay time	-	0.1	-		
$t_f$	Fall time	-	1.3	-		
$V_{SD}$	Diode forward voltage drop	-	-	0.9	V	$V_{GS} = -10\text{V}, I_{SD} = 1.0\text{mA}$
$t_{rr}$	Reverse recovery time	-	200	-	ns	$V_{GS} = -10\text{V}, I_{SD} = 1.0\text{mA}$

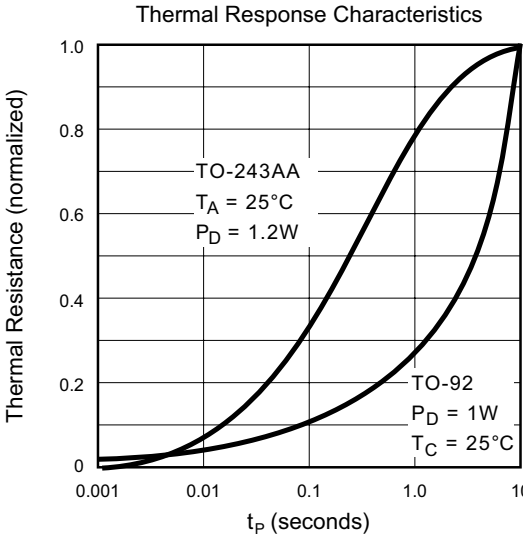
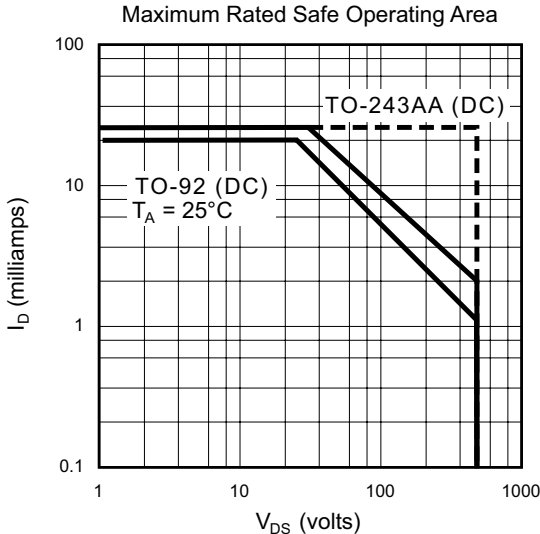
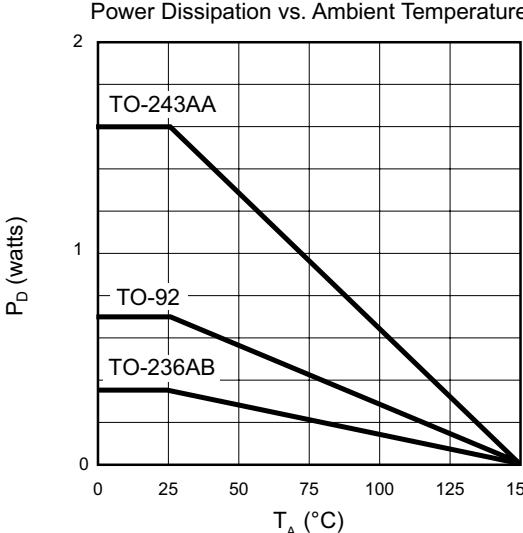
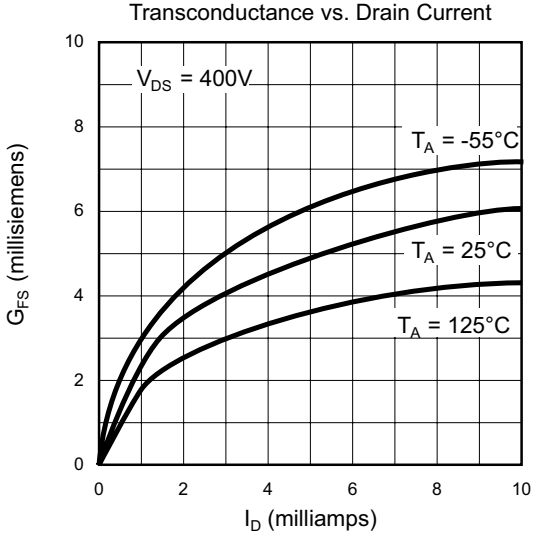
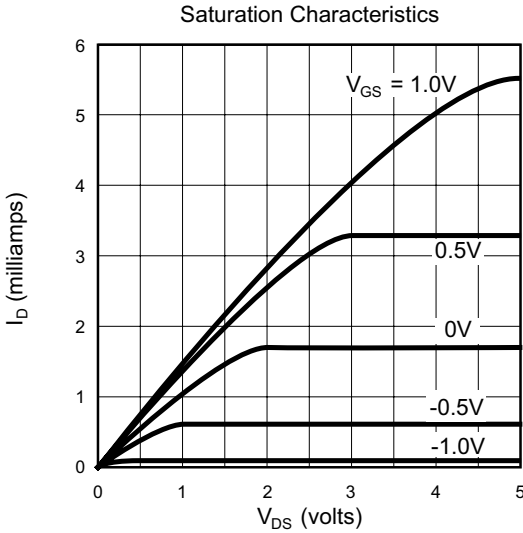
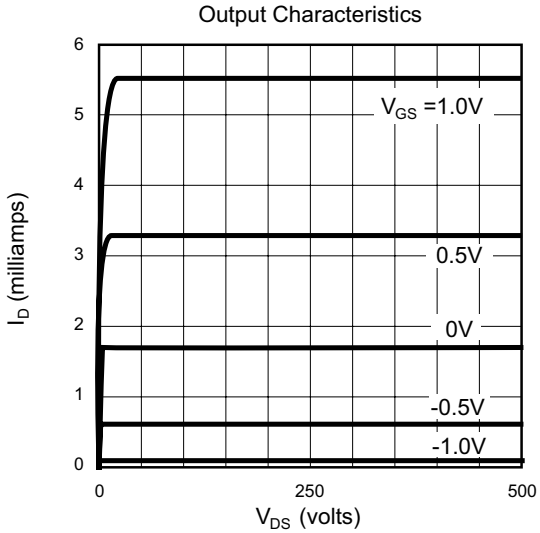
**Notes:**

1. All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test: 300 $\mu\text{s}$  pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

### Switching Waveforms and Test Circuit

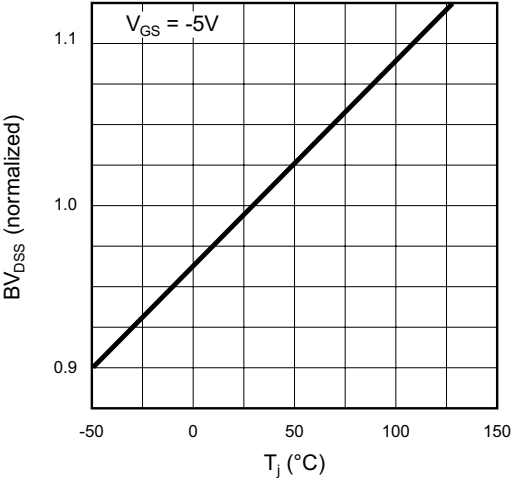


# Typical Performance Curves

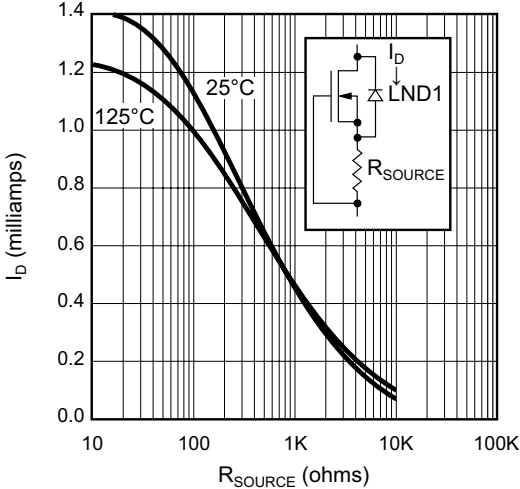


Typical Performance Curves (cont.)

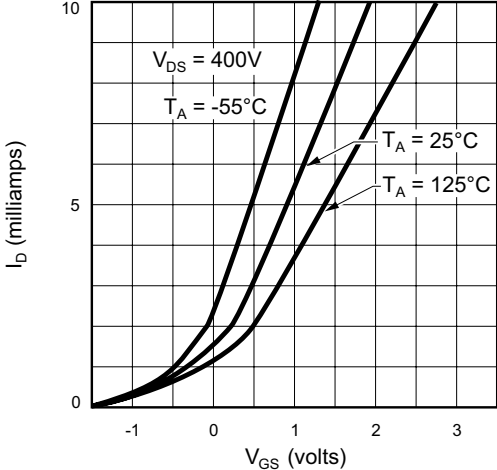
BV<sub>DSS</sub> Variation with Temperature



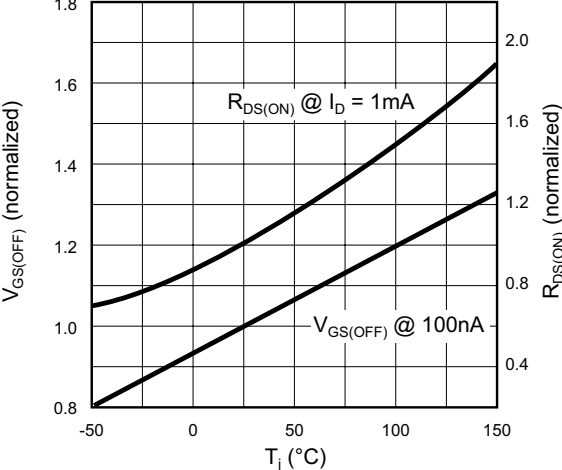
I<sub>D</sub> vs. R<sub>SOURCE</sub>



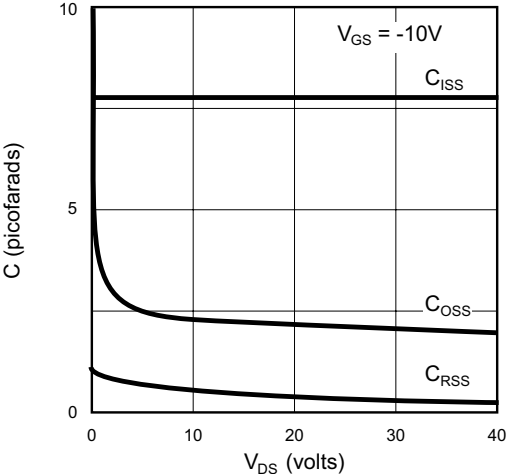
Transfer Characteristics



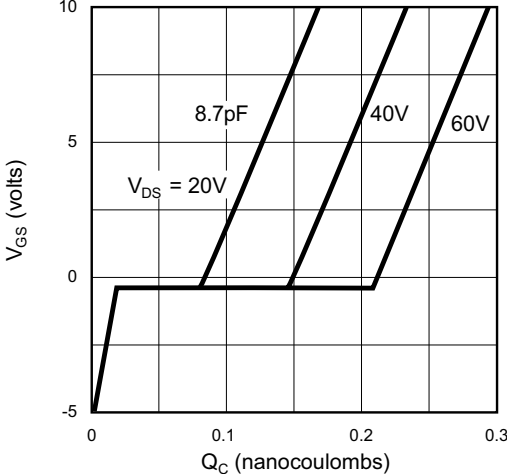
V<sub>GS(OFF)</sub> and R<sub>DS</sub> Variation with Temperature



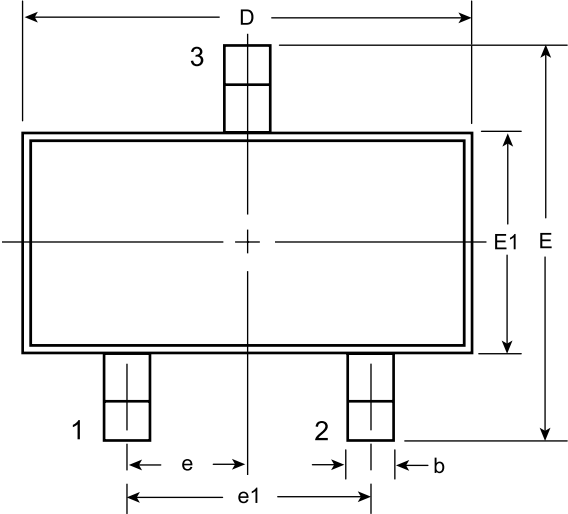
Capacitance vs. Drain-to-Source Voltage



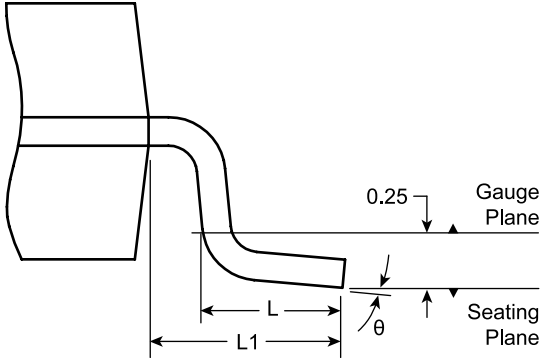
Gate Drive Dynamic Characteristics



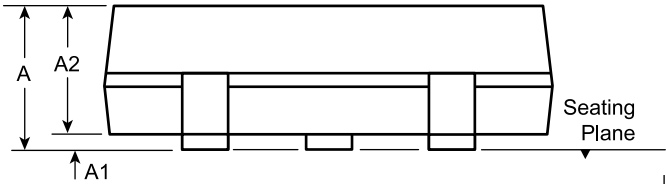
**3-Lead TO-236AB (SOT-23) Package Outline (K1)**  
**2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch**



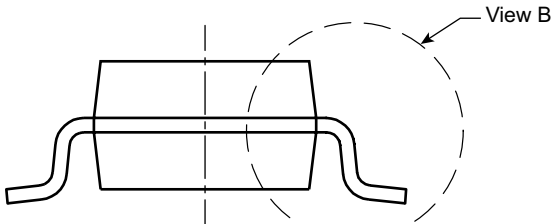
**Top View**



**View B**



**Side View**



**View A - A**

Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	$\theta$
Dimension (mm)	MIN	0.89	0.01	0.88	0.30	2.80	2.10	1.20	0.95 BSC	1.90 BSC	0.20 <sup>†</sup>	0.54 REF	0°
	NOM	-	-	0.95	-	2.90	-	1.30			0.50		-
	MAX	1.12	0.10	1.02	0.50	3.04	2.64	1.40			0.60		8°

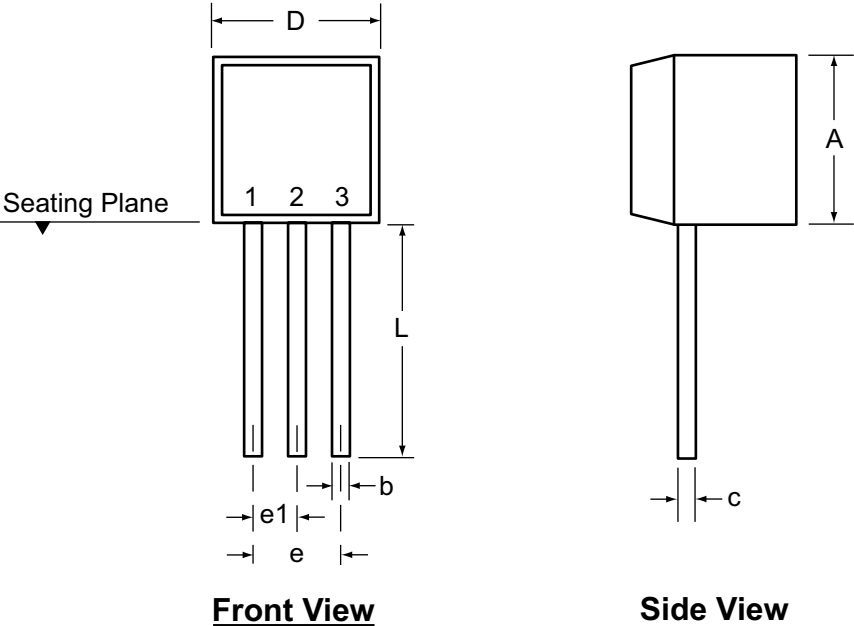
JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999.

<sup>†</sup> This dimension is a non-JEDEC dimension.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO236ABK1, Version B072208.

### 3-Lead TO-92 Package Outline (N3)



Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014 <sup>†</sup>	.014 <sup>†</sup>	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 <sup>†</sup>	.022 <sup>†</sup>	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

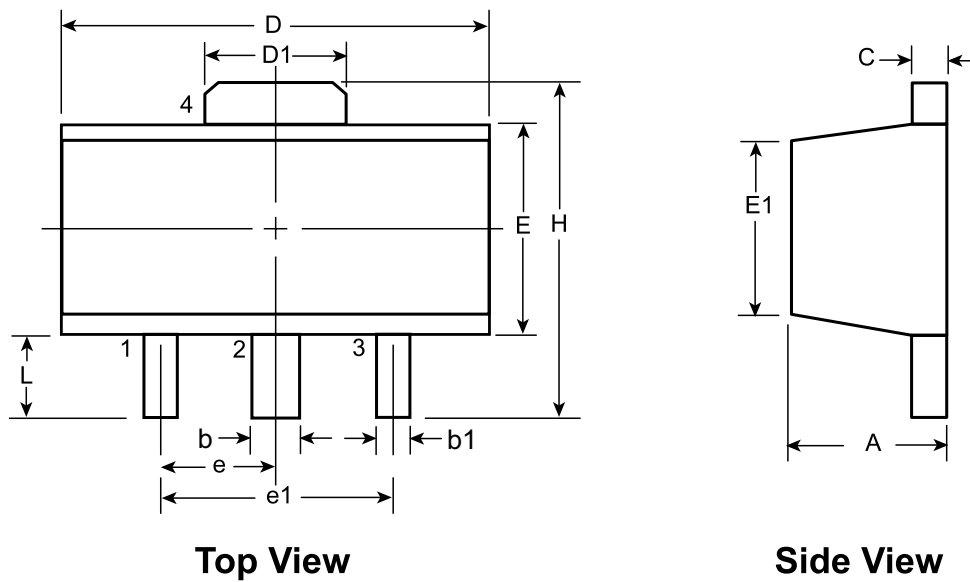
\* This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.

† This dimension is a non-JEDEC dimension.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO92N3, Version D080408.

### 3-Lead TO-243AA (SOT-89) Package Outline (N8)



**Top View**

**Side View**

Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L	
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.13	1.50 BSC	3.00 BSC	3.94	0.89	
	NOM	-	-	-	-	-	-	-	-			-	-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20	

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.

Drawings not to scale.

Supertex Doc. #: DSPD-3TO243AAN8, Version D070908.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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