CDMA DATA TERMINAL

DTGS-800 Reference Manual
Application Information

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It is advised for the customers to contact our engineers for more information with respect to Keypad, audio interface, RF interface and input power supply before they start an actual design.

Contents

Figures

Tables

1. Introduction

1.1 Purpose

This manual provides hardware interface and programming information for the DTGS-800 CDMA Wireless Data Module.

1.2 Organization

This manual will discuss the interface and operation of the module and is divided into the following subsections:

- Section 2 – Introduces users to the DTGS-800 CDMA Wireless Data Module's basic features and general specifications.
- Section 3 – Lists each DTGS-800 pin and its function within the device. The pin-out for the module is listed in numeric sequence.
- Section 4 – Shows how the subsystem or block interfaces with external peripherals
- Section 5 – Specifies the recommended operating conditions, DC voltage characteristics, I/O timing, and power estimations for the module. Timing diagrams are also included.
- Section 6 – Provides mechanical dimensions and RF connector for the module.

1.3 Revision History

The revision history for this document is shown in Table 1-1.

Table 1-1 Revision History

Version	Date	Description
V1_X1	Dec. 2002	Initial Release
V1_X2	Feb. 2003	1st Revision - 100 pin map - RF connector - Keypad & DTMF
V1_X3	Oct. 2003	2'nd Revision - 100 pin map - Electrical specifications
V1_X4	Jan. 2004	3'rd Revision - External Hardware Reset

1.4 References

1. QUALCOMM Incorporated. MSM6050 Mobile Station Modem™: Component Supply Specification. 80-V2466-1, April 13, 2002.
2. QUALCOMM Incorporated. MSM6050™ Mobile Station Modem: Device Specification (Preliminary Information). 93-V3185-1, March 29, 2002.
3. QUALCOMM Incorporated. SURF6050 User Manual. 80-V2551-40, March 29, 2002.

1.5 Acronym List

Term	Definition
CDMA	Code-Division Multiple Access
CODEC	Coder-Decoder
GPIO	General-purpose Input/Output
JTAG	Joint Test Action Group (ANSI/ICEEE Std. 1149.1-1990)
LCD	Liquid Crystal Display
LDO	Voltage Regulator
LED	Light Emitting Diode
PCB	Printed Circuit Board
PCM	Pulse Coded Modulation
PCS	Personal Communications Service
RF	Radio Frequency
Rx	Receive
TCXO	Temperature-Controlled Crystal Oscillator
Tx	Transmit
UART	Universal Asynchronous Receiver Transmitter

2. Overview

2.1 Application Descriptions

The CDMA Wireless Data Module is a complex consumer communications instrument that relies heavily on both digital signal and embedded processor technologies. The Wireless Data Modules manufactured by AnyDATA.NET support Code-Division Multiple Access (CDMA). This operates in the cellular spectrum band.

In a continuing effort to simplify the design and to reduce the size and production cost of the Wireless Data Module, AnyDATA.NET has successfully developed the DTG series. The DTGS-800 is AnyDATA.NET's latest compact Wireless Data Module operating in the Cellular spectrum band. The DTGS-800 contains not only a complete digital modulation and demodulation system for CDMA standards as specified in IS-95 A/B and IS-2000, but also GPSOne position location solution which offers wireless callers their location wherever and whenever they need it.

GPSOne is QUALCOMM CDMA Technologies' position location solution. It offers the availability of position location determination in hostile environments (such as indoors) where conventional GPS receivers do not work well.
GPSOne uses a hybrid approach that utilizes signals from the GPS satellite constellation and from CDMA cell sites to determine location. Using the hybrid approach, GPSOne enhances location services availability, accelerates the location determination process, and provides improved accuracy.
The hybrid mode approach for position location uses signals from CDMA cell stations and GPS satellites to compute the user's location. This approach basically takes advantage of an accurate knowledge of GPS system timing on a CDMA mobile station. The knowledge of system timing allows the GPSOne solution to use both the CDMA signal measurements and GPS signal measurements collectively to compute the user's location. It also allows for a central entity, named Position Determination Entity (PDE), to send estimated signal phases to the mobile. This knowledge reduces the time to search the satellite pseudo ranges on the mobile, thus improving the time taken to determine the user's position.

The subsystem in the DTGS-800 includes a CDMA processor (MSM6050), an integrated CODEC with an ear piece and microphone amplifiers, and an RS-232 serial interface supporting forward link data

communications at a rate of 153kbps.

The DTGS-800 provides an external interface that includes the standard RS-232, Digital Audio, External reset control, parallel LCD Display, Keypad, Ringer extension ports and R-UIM for China market.

The DTGS-800 has the capability to power down unused circuits in order to dynamically minimize power consumption.

2.2 Technical Specifications

2.2.1 General Specifications

Parameters	Descriptions
External Access	Code-Division-Multiple-Access (CDMA)
CDMA Protocol	IS-95 A/B, IS-98A, IS-126, IS-637A, IS-707A, IS-2000
Data Rate	153.6Kbps max
Transmit/Receive Frequency Interval	45MHz for Cellular
Vocoder	EVRC, 13kQCELP
RF technology	Zero Intermediate Frequency
Number of Channel	832 for Cellular
Operating Voltage	VBATT_INT : +4.0V ±10%
	VEXT_DC : +4.5V±10%
Current Consumption	Stand by mode: Idle (90mA), Sleep (less than 1mA) Busy mode: About 520mA
Operating Temperature	-30ºC ~ +60ºC
Frequency Stability	±300Hz for Cellular
Antenna	GSC Connector, 50ohm
Size	53 X 33 X 2.7mm with case
Weight	About 15g
External Interface	RS-232s, Digital/Analog Audios, LCD, Keypad, Ringer External Reset Control, R-UIM, MP3, MIDI, GPIOs, USB
User Interface Software	BREW support
Additional Function	GPSOne position location solution

2.2.2 Receive Specifications

Parameters	Descriptions
Frequency Range	869.04 ~ 893.97 MHz for Cellular
Sensitivity	Below –104 dBm
Interference Rejection	Single tone (-30dBm @900KHz): Below –101dBm Two tone (-43 dBm @900KHz and 1700KHz): Below –101dBm Two tone (-32 dBm @900KHz and 1700KHz): Below –90dBm Two tone (-21 dBm @900KHz and 1700KHz): Below –79dBm
Spurious Wave Suppression	Below –80dBc
Input Dynamic Range	-25 dBm ~ -104dBm

2.2.3 Transmit Specifications

Parameters	Descriptions
Frequency Range	824.04 ~ 848.97 MHz for Cellular
Nominal Power	0.32 W (25.0dBm)
Minimum Controlled Output Power	Below –50dBm

Max Power Spurious	900KHz: Below –42dBc/30KHz 1.98MHz: Below –54dBc/30KHz

2.2.4 Standards

IS-95 A/B: Protocol Between MS & BTS

IS-96A: Voice Signal Coding

IS-98A: Base MS Function

IS-126: Voice Loop-Back

IS-637: Short Message Service

IS-707: Data Service

Built-in TCP/IP : AnyDATA proprietary software

IS-657 : packet data

2.3 Interface Diagram

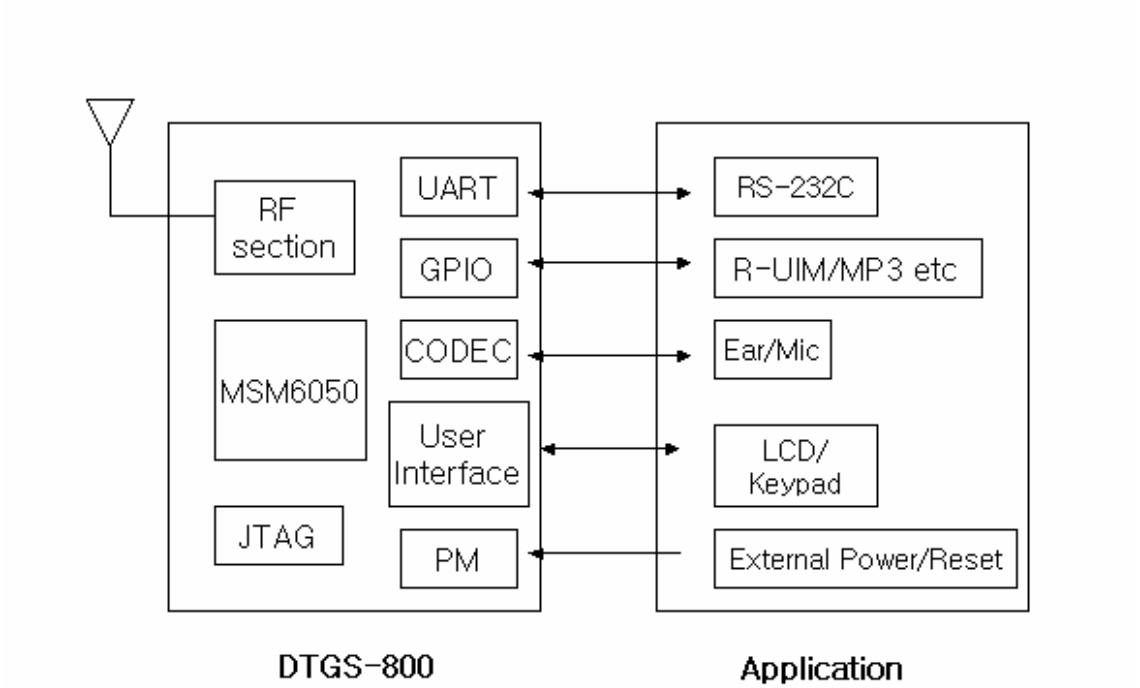


Figure 2-1 Interface Block Diagram

3. PIN Description

3.1 I/O Description Parameters

Symbol	Description
I	CMOS Input
O	Output
B	Bi-directional
N	Voltage or Current Level
IS	Input with Schmitt Trigger
BS	Bi-directional Schmitt Trigger
PU	Internal Pull-Up
PD	Internal Pull-Down

3.2 PIN Names and Pinouts

3.2.1 100-Pin Connector

PIN	NAME	TYPE	DESCRIPTION
1	D15	B-K3	Data line
2	AGND	AGND	Analog Ground
3	D14	B-K3	Data line
4	AGND	AGND	Analog Ground
5	D12	B-K3	Data line
6	D13	B-K3	Data line
7	D10	B-K3	Data line
8	D11	B-K3	Data line
9	D08	B-K3	Data line
10	D09	B-K3	Data line
11	GND	GND	Signal ground
12	GND	GND	Signal ground
13	MSM_DP_DCD/ (GPIO_INIT44)	BS-PD	Data carrier detect (UART1)
14	MSM_DP_RI/ (GPIO_INIT54)	BS-PD	Ring indicator (UART1)
15	MSM_DP_RFR/	O	Ready for Receive (UART1)
16	MSM_DP_TXD	O	Transmit data (UART1)
17	MSM_DP_DTR/ (GPIO_INIT50)	BS-PU	Data terminal ready (UART1)
18	MSM_DP_RXD	IS-PD	Receive data (UART1)
19	MSM_DP_CTS/	IS-PD	Clear to send (UART1)
20	MSM_DP_RXD2 (GPIO_INT29)	BS_PD3	General Purpose Input Output, Receive data (UART2)
21	MSM_DP_TXD2 (GPIO_INT28)	BS_PD3	General Purpose Input Output, Transmit data (UART2)
22	MSM_DP_CTS2/ (GPIO_INT30)	BS_PD3	General Purpose Input Output, Clear to send (UART2)
23	MSM_DP_RFR2/ (GPIO_INT31)	BS_PD3	General Purpose Input Output, Ready for Receive(UART2)
24	UART_EN (GPIO_INT15)	BS_PU3	General Purpose Input Output
25	AUX_PCM_CLK	BS_PD3	External CODEC PCM clock
26	AUX_PCM_DOUT	BS_PU3	External CODEC PCM data output

PIN	NAME	TYPE	DESCRIPTION
27	AUX_PCM_SYNC	BS_PD3	External CODEC PCM data strobe
28	AUX_PCM_DIN	IS-PD	External CODEC PCM data input
29	GPIO_INT49	BS_HK2	General Purpose Input Output
30	POWER_ON	BS_PU3	POWER_ON INPUT
31	EX_RESET	-	External Reset (LOW Enable)
32	GPIO_INT18	BS_PD3	General Purpose Input Output
33	GPIO_INT45 (USB_SUSPEND)	BS_PD3	General Purpose Input Output
34	GPIO_INT33 (IDLE)	BS_PD3	General Purpose Input Output
35	GPIO_INT47 (BUSY)	BS_PU3	General Purpose Input Output
36	GND	GND	Signal ground
37	GND	GND	Signal ground
38	D00	B-K3	Data line
39	D01	B-K3	Data line
40	D02	B-K3	Data line
41	D03	B-K3	Data line
42	D04	B-K3	Data line
43	D05	B-K3	Data line
44	D06	B-K3	Data line
45	D07	B-K3	Data line
46	A02	B-K3	Address line
47	A01	B_K3	Address line
48	RESET_OUT/	O	Reset Out
49	GPIO_INT37(LCD_CS/)	BS_PU3	General Purpose Input Output (lcd chip select)
50	GPIO_INT36(LCD_EN)	BS_PU3	General Purpose Input Output (lcd enable)
51	OE/	O-3	Output Enable Signal
52	WE/	O-3	Write Enable Signal
53	KEYSENSE0/ (GPIO_INT62)	IS_PU3	Key sense input
54	KEYSENSE1/ (GPIO_INT63)	IS_PU3	Key sense input
55	KEYSENSE2/ (GPIO_INT64)	IS_PU3	Key sense input
56	KEYSENSE3/ (GPIO_INT65)	IS_PU3	Key sense input
57	KEYSENSE4/ (GPIO_INT66)	IS_PU3	Key sense input
58	GPIO_INT61 (KEYPAD00)	BS_PD3	General Purpose Input Output, Keypad input
59	GPIO_INT60 (KEYPAD01)	BS_PD3	General Purpose Input Output, Keypad input
60	GPIO_INT59 (KEYPAD02)	BS_PD3	General Purpose Input Output, Keypad input
61	GPIO_INT58 (KEYPAD03)	BS_PD3	General Purpose Input Output, Keypad input
62	GPIO_INT57 (KEYPAD04)	BS_PD3	General Purpose Input Output, Keypad input
63	GPIO_INT56 (KEYPAD05)	BS_PD3	General Purpose Input Output, Keypad input
64	GPIO_INT48 (ON_SW_SENSE/)	BS_PU3	General Purpose Input Output, On Switch Sensor
65	GPIO_INT09 (UIM_RESET)	BS_HK2	General Purpose Input Output, UIM Reset Output
66	GPIO_INT10 (UIM_PWR_EN)	BS_HK2	General Purpose Input Output, UIM Power Enable
67	GPIO_INT42 (SMS)	BS_HKP2	General Purpose Input Output,
68	GPIO_INT17	BS_PU3	General Purpose Input Output
69	GPIO_INT04	BS_PD3	General Purpose Input Output
70	GPIO_INT16	BS_PU3	General Purpose Input Output
71	VIBRATOR_DRV	-	VIBRATOR_DRV output
72	PS_HOLD	-	PS_HOLD output
73	AUXON (MELODY-)	OA	Auxiliary output (-)
74	SPKER/RINGER	-	Speaker/Ringer output
75	AUXOP (MELODY+)	OA	Auxiliary output (+)

PIN	NAME	TYPE	DESCRIPTION
76	GND	GND	Signal ground
77	GND	GND	Signal ground
78	GPIO_INT19 (EAR_DET1)	BS_PD3	General Purpose Input Output, Ear Jack Detector Input
79	EAR2O (EAR_JACK+)	OA	Ear_Jack(+) output
80	EAR1O_P	OA	External Receiver(+) output
81	EAR1O_N	OA	External Receiver(-) output
82	MIC1P	IA	External Mic(+) input
83	MIC2P	IA	Ear_Mic(+) input
84	GND	GND	Signal Ground
85	GND	GND	Signal ground
86	+VBATT	IA	Battery Gauge input
87	+VEXT_DC	V	External DC input
88	VBATT_INT	V	Battery input
89	+VEXT_DC	V	External DC input
90	VBATT_INT	V	Battery input
91	GPIO_INT11	BS_PD3	General Purpose Input Output (UART3)
92	GPIO_INT12	BS_PD3	General Purpose Input Output (UART3)
93	GPIO_INT13	BS_PD3	General Purpose Input Output (UART3)
94	GPIO_INT14	BS_PD3	General Purpose Input Output (UART3)
95	GPIO_INT02	BS_PU3	General Purpose Input Output
96	GP_ADC_DET	IA	General Purpose Analog to Digital Converter Input
97	GPIO_INT34 (GP_CS0/)	BS_PU3	General Purpose Input Output, Chip Select0
98	GPIO_INT35 (GP_CS1/)	BS_PU3	General Purpose Input Output, Chip Select1
99	GND	GND	Signal ground
100	GND	GND	Signal ground

3.3 100-PIN Connect Pinouts (Topview)

Table 3-1 100-PIN Connector Pinouts

1	D15	2	AGND
3	D14	4	AGND
5	D12	6	D13
7	D10	8	D11
9	D08	10	D09
11	GND	12	GND
13	MSM_DP_DCD/ (GPIO_INT44)	14	MSM_DP_RI/ (GPIO_INT54)
15	MSM_DP_RFR/	16	MSM_DP_TXD
17	MSM_DP_DTR/ (GPIO_INT50)	18	MSM_DP_RXD
19	MSM_DP_CTS/	20	MSM_DP_RXD2 (GPIO_INT29)
21	MSM_DP_TXD2 (GPIO_INT28,UIM_DATA)	22	MSM_DP_CTS2/ (GPIO_INT30)
23	MSM_DP_RFR2/ (GPIO_INT31, UIM_CLK)	24	UART_EN (GPIO_INT15)
25	AUX_PCM_CLK	26	AUX_PCM_DOUT
27	AUX_PCM_SYNC	28	AUX_PCM_DIN
29	GPIO_INT49	30	POWER_ON
31	EX_RESET	32	GPIO_INT18
33	GPIO_INT45	34	IDLE (GPIO_INT33)
35	BUSY (GPIO_INT47)	36	GND
37	GND	38	D00
39	D01	40	D02
41	D03	42	D04
43	D05	44	D06
45	D07	46	A02
47	A01	48	RESET_OUT
49	LCD_CS/ (GPIO_INT37)	50	LCD_EN (GPIO_INT36)
51	OE/	52	WE/
53	KEYSENSE0/ (GPIO_INT62)	54	KEYSENSE1/ (GPIO_INT63)
55	KEYSENSE2/ (GPIO_INT64)	56	KEYSENSE3/ (GPIO_INT65)
57	KEYSENSE4/ (GPIO_INT66)	58	KEYPAD00 (GPIO_INT61)
59	KEYPAD01 (GPIO_INT60)	60	KEYPAD02 (GPIO_INT59)
61	KEYPAD03 (GPIO_INT58)	62	KEYPAD04 (GPIO_INT57)
63	KEYPAD05 (GPIO_INT56)	64	GPIO_INT48 (ON_SW_SENSE/)
65	GPIO_INT09 (UIM_RESET)	66	GPIO_INT10 (UIM_PWR_EN)
67	SMS (GPIO_INT42)	68	GPIO_INT17
69	GPIO_INT04	70	GPIO_INT16
71	VIBRATOR_DRV	72	PS_HOLD
73	AUXON (MELODY-)	74	SPKER/RINGER
75	AUXOP (MELODY+)	76	GND
77	GND	78	GPIO_INT19 (EAR_DET1)
79	EAR2O	80	EAR1O_P

81	EAR1O_N	82	MIC1P
83	MIC2P	84	GND
85	GND	86	+VBATT
87	+VEXT_DC	88	VATT_INT
89	+VEXT_DC	90	VATT_INT
91	GPIO_INT11 (MSM_DP_RXD3)	92	GPIO_INT12 (MSM_DP_TXD3)
93	GPIO_INT13 (MSM_DP_CTS3/)	94	GPIO_INT14 (MSM_DP_RFR3)
95	GPIO_INT02	96	GP_ADC_DET
97	GPIO_INT34 (GP_CS0/)	98	GPIO_INT35 (GP_CS1/)
99	GND	100	GND

Notes:

* We strongly recommend that the user has a 3-pin connector or 3 test points on their board, so that one can easily monitor and diagnose their module.

** If the user wants the module to monitor battery voltage and the user is using a regulator in conjunction with a battery, whose maximum voltage exceeds 4.3 V, to drive the module, then the user should please contact our engineers.

4. Interface Descriptions

4.1 Overview

This chapter covers information required to convert the DTGS-800 into a subscriber unit application. In addition, some of the internal blocks of the device are described. Understanding these internal blocks is necessary for one to completely grasp the functions of the various interfaces.

This chapter discusses the interface to the major blocks of the DTGS-800 as shown in the following figure. These blocks include:

- CODEC Interface
- UART Interface
- General Purpose Interface
- External Hardware Reset
- User Interface

4.2 CODEC Interface

With the integrated microphone and earpiece amplifier including CODEC, the DTGS-800 module interfaces directly, either differential or single-ended, to the microphone and earpiece.

The audio features in the module are

- Two microphone inputs
- Two earphone outputs and one auxiliary audio output.

4.2.1 Internal CODEC Interface

The module contains analog audio interface circuitry. The contained audio interface supports all of the required conversation and amplification stages for the audio front end.

The audio interface includes the amplification stages for both the microphone and earphone.

The EAR10 and MIC1P are typically used for the handset microphone,

The EAR_JACK+ and MIC2P are typically used for the ear-jack.

Table 4-1 Analog Audio Pinouts

NAME	DESCRIPTION	CHARACTERISTIC
MIC2P	Mic Jack Input	Analog Input (Pin No. 83, for Ear-Mic Jack) *

NAME	DESCRIPTION	CHARACTERISTIC
EAR_DET1	EAR/MIC Set Detect	Logic Input (Pin No. 78) **
EAR_JACK+	Earphone Output	Analog Output (Pin No. 79 for Ear-Mic Jack)
GND_A	Audio Ground	Audio Ground (Pin No. 2, 4)
EAR10_N	Speaker Output -	Analog Output (Pin No. 81)
EAR10_P	Speaker Output +	Analog Output (Pin No. 80)
MIC1P	Mic Input	Analog Input (Pin No. 82)
AUXON	Auxiliary Output -	Analog Output (Pin No. 73)
AUXOP	Auxiliary Output +	Analog Output (Pin No. 75)

Note:

* MIC2, along with being a microphone input, checks to see if the user has pressed the headset key, which allows the user to connect to or disconnect from a call. This pin is internally pulled high and is therefore normally in the high state. To activate this input and connect to or disconnect from a call, the user must set the MIC2 pin to a low state for 100ms to 200ms.

** EAR_DET1 checks to see if a headset has been connected to the ear-jack. When there is no headset connected to the ear-jack, the audio path is disconnected. When a headset is connected to the ear-jack an audio path is opened. To simulate a headset connected to the ear-jack, the user must apply a low signal to the EAR_DET1 pin for as long as the user wants the audio path to be kept open.

4.2.2 Extended CODEC Interface

The PCM CODEC interface is used for the car-kit audio system. This interface is optional.

External CODEC interface signals are listed below:

Table 4-2 Digital CODEC Pinouts

NAME	DESCRIPTION	PINOUTS
AUX_PCM_CLK	PCM Clock	Pin No. 25
AUX_PCM_DIN	PCM Data Input	Pin No. 28
AUX_PCM_DOUT	PCM Data Output	Pin No. 26
AUX_PCM_SYNC	PCM Sync.	Pin No. 27

4.3 UART Interface

The Universal Asynchronous Receiver Transmitter (UART) communicates with serial data that conforms to the RS-232 Interface protocol. The module has 3 UARTs which provides 3.0V CMOS level outputs and 3.0V CMOS input levels. All the control signals of the RS-232 are active low, however the data signals, RXD and TXD, are active high.

UART1 which has 512 bytes for Tx and Rx FIFO, supports high speed data communication up to 230.4kbps, program download and diagnostic monitor function.

UART2 and 3 which 64 bytes for T/Rx FIFO, support low speed data communication up to 115.2kbps, program download and diagnostic monitor function.

The UART features hardware handshaking, programmable data sizes, programmable stop bits, and odd, even, no parity.

4.3.1 UART1 interface

Table 4-3 UART1 Interface Pinouts

NAME	DESCRIPTION	PIN NUNBER	CHARACTERISTIC
DP_DCD/	Data Carrier Detect	13	Network connected from the module
DP_RI/	Ring Indicator	14	Output to host indicating coming call
DP_RFR/	Ready for Receive	15	Ready for receive from host
DP_TXD	Transmit Data	16	Output data from the module
DP_DTR/	Data Terminal Ready	17	Host ready signal
DP_RXD	Receive Data	18	Input data to the module
DP_CTS/	Clear to Send	19	Clear to send to the host
GND	Signal Ground	11, 12	Signal ground

4.3.2 UART2 interface

The UART2 supports not only UART function, but also R-UIM interface for China market.

Table 4-4 UART2 Interface Pin outs

NAME	DESCRIPTION	PIN NUMBER	CHARACTERISTIC
DP_RXD2	Receive Data	20	Input data to the module
DP_TXD2	Transmit Data	21	Output data from the module
DP_CTS2/	Clear to Send	22	Clear to send to the host
DP_RFR2/	Ready for Receive	23	Ready for receive from host
GND	Signal Ground	11, 12	Signal ground

Table 4-5 R-UIM Interface Pin outs

NAME	DESCRIPTION	PIN NUMBER	CHARACTERISTIC
DP_RXD2	UIM_PWR_EN	20	Output UIM power enable
DP_TXD2	UIM_DATA	21	Intput data from R-UIM
DP_CTS2/	UIM_RESET	22	R-UIM reset
DP_RFR2/	UIM_CLK	23	R-UIM clock
GND	Signal Ground	11, 12	Signal ground

4.3.3 UART3 interface

The UART3 is used to monitor and diagnose the status of the DTGS-800. It is strongly recommended for the user to have the following UART3 pins connected to an extra connector or to test points, in order

to easily troubleshoot any problems with the module.

Table 4-5 UART3 Interface Pin-outs

NAME	DESCRIPTION	PIN NUMBER	CHARACTERISTIC
DP_RXD3	Receive Data	91	Input data to the module
DP_TXD3	Transmit Data	92	Output data from the module
DP_CTS3/	Clear to Send	93	Clear to send to the host
DP_RFR3/	Ready for Receive	94	Ready for receive from host
GND	Signal Ground	11, 12	Signal ground

4.4 General Purpose Interface

The general purpose interface consists of 11 user-definable bi-directional pins.

Each GPIO pin can be configured as an input interrupt source. In addition, some GPIO pins can be used as output control pins from the module. The user can define these pins properly as follows.

Table 4-6 General Purpose Interface Pin-outs

NAME	PIN NUMBER	CHARACTERISTIC
GPIO_INT15	24	Configured as a pull-up, Bi-directional
GPIO_INT45	33	Configured as a pull-up, Bi-directional
GPIO_INT33	35	Configured as a pull-down, Bi-directional
GPIO_INT17	68	Configured as a pull-up, Bi-directional
GPIO_INT04	69	Configured as a pull-down, Bi-directional
GPIO_INT16	70	Configured as a pull-down, Bi-directional
GPIO_INT11	91	Configured as a pull-down, Bi-directional
GPIO_INT12	92	Configured as a pull-up, Bi-directional
GPIO_INT13	93	Configured as a pull-up, Bi-directional
GPIO_INT14	94	Configured as a pull-down, Bi-directional
GPIO_INT02	95	Configured as a pull-down, Bi-directional

4.5 External Hardware Reset and Power Down Registration

4.5.1 External Hardware Reset (Pin #31)

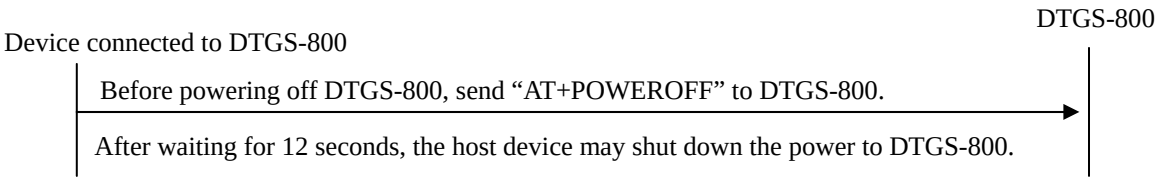
There are two types of resets that the user can employ to restart the module. The first type will reset the MSM and the memory and is performed when the user gives the AT command, AT+RESET, to the MSM. Another way to reset the module is by using the external hardware reset. This type of reset will reset the hardware as well as the MSM and the memory. The flash memory will be the only information that is kept. To perform an external hardware reset, make sure the module has powered on and is not in the initialization stage, and then apply a low signal of almost 0V to the external hardware reset pin (Pin #31) for 200ms to 500ms. Keep the external hardware reset pin high when the module is initializing as well as during normal operation.

4.5.2 Power Down Registration

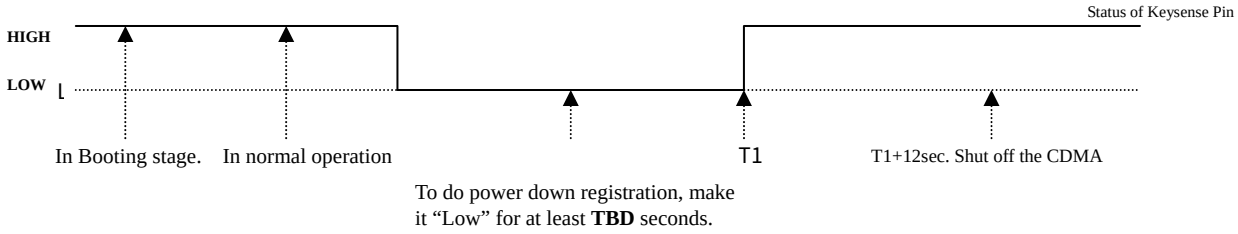
Before DTGS-800 is powered off, it has to send power down registration message to the CDMA base station to help the base station to maximize its capacity. Depending on air interface environment, it may take 12 seconds at maximum according to CDMA technical standard.

4.5.2.1 Power Down Registration Protocol for CDMA device

4.5.2.1.1 Using AT command – most convenient method



4.5.2.1.2 Using Keysense Pin (Pin # 30 is TBD)



4.6 User Interface

4.6.1 Keypad

The keypad interface consists of a 5 X 6 matrix pattern. The 5-KEYSENSE/[4:0] pins are used to connect a matrix keypad to the module. The KEYSENSE/ pins are active low.

The 6-KEYPAD pins are necessary to construct the other side of the matrix. These KEYPAD pins must be active high in order for the keypad matrix to work properly. The general keypad matrix is shown below:

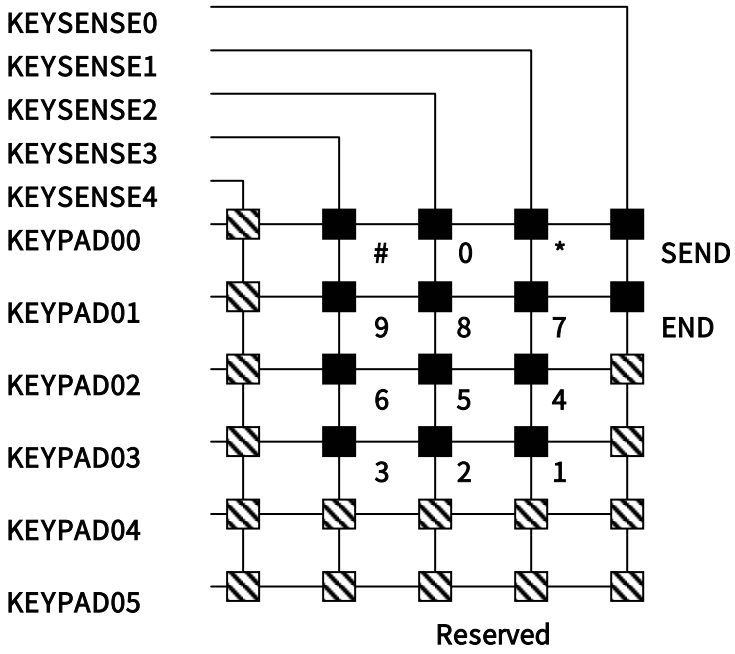


Figure 4-1 Keypad Matrix

DTMF

When key is pressed, CDMA Module generates standard DTMF tone and sends it to the local audio path (speaker). If the Mobile station is in traffic state, the CDMA Module sends DTMF Message to the Base Station and to the local audio path (speaker) at the same time. The network will deliver the analog DTMF tone or DTMF Message to its final destination.

4.6.2 LCD

The module supports the 16 bits parallel LCD interface as well as the 8 bits. The LCD interface is composed of 23-signals. Direct access to the LCD driver is not applicable.

Table 4-7 LCD Interface Signals

NAME	TYPE	CHARACTERISTIC
LWR/	BS_PU	LCD RW pin out from the module
LCD_EN	BS	LCD E pin out from the module
A01	B	LCD RS pin out from the module
LCD_CS/	O	LCD Chip Select pin out from the module
RES_OUT/	O	LCD Reset from the module
D00 ~ D015	O	LCD Data Lines from the module
VDD		LCD Power Supply
GND		LCD Signal Ground

4.6.3 Ringer

The Ringer pin provides the output to drive the sound transducer on the host. It alerts the user of a voice call event and outputs key tones if the keypad is connected.

The DTGS-800 module includes Ringer Driver and drives Buzzer directly.

Table 4-8 Ringer/Buzzer Driver Output Spec.

PARAMETER	TEST CONDITION	TYPICAL VALUE
Drive Frequency		Max 8kHz
Load Current	R_load=10 ohm	Min 300mA
Load Resistance		Typ 10 ohm

5. Electrical Specifications

5.1 DC Electrical Specifications

5.1.1 Absolute Maximum Ratings

Operating the module under conditions that exceed those listed in the Absolute Maximum Ratings table may result in damage to the module.

Absolute Maximum Ratings should be considered as limiting values. The module may not function properly and should not be operated if any one of the parameters is not within its specified operating range.

Table 5-1 Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS
Storage Temperature	-50	+85	ºC
Voltage On Any Input or Output Pin	-0.8	+3.5	V
Supply Voltage	-1.0	+5.0	V
Initializing Current	170		mA
Drop	No damages after 60-Inch drop over concrete floor		

5.1.2 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNITS
Supply Voltage	VBATT_INT	+3.6	+4.0	+4.4	V
	VEXT_DC	+4.0	+4.5	+5.0	
Operating Temperature		-30		+60	ºC
Operating Humidity		95% (50°C) Relative Humidity			

5.1.3 Power Consumption

CONVERSATION (Busy)	STANDBY	
	Idle	Sleep
About 520mA (Max power)	90mA	Less than 1mA

5.1.4 Serial Interface Electrical Specifications

PARAMETER	MIN	TYP (NO LOAD)	MAX	UNITS
Input High Voltage	+2.0	+3	+3.3	V
Input Low Voltage	-0.5	0	+0.8	V
Output High Voltage	+2.4	+2.7		V
Output Low Voltage		0	+0.4	V

5.2 Timing characteristics

5.2.1 External CODEC Timing

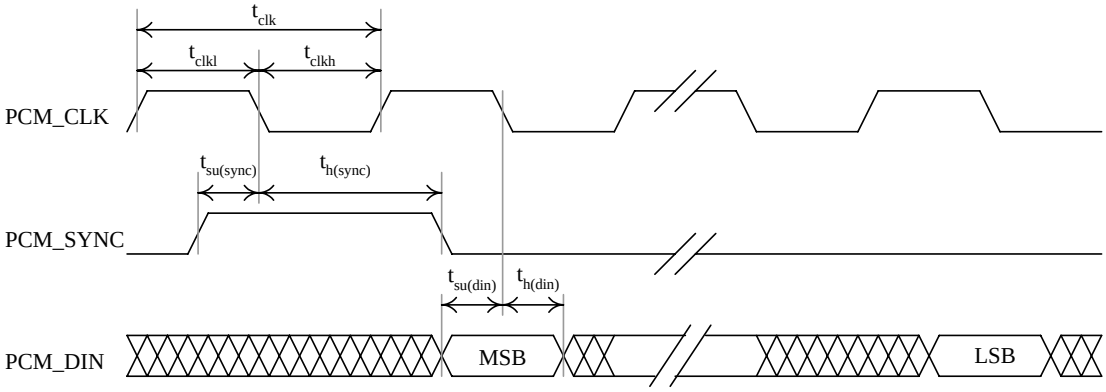


Figure 5-1 External PCM CODEC to Module timing

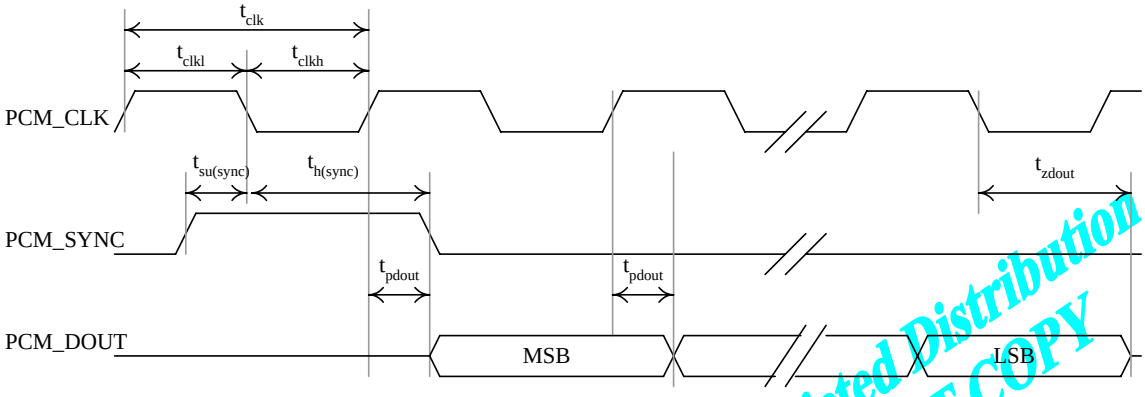


Figure 5-2 Module to External PCM CODEC timing

Table 5-2 External PCM CODEC Parameters

PARAMETER	DESCRIPTION	MIN	TYP.	MAX	UNIT
t_{clk}	PCM-CLK cycle time	400	500		ns
t_{clkl}	PCM-CLK low time	200	250		ns
t_{clkh}	PCM-CLK high time	200	250		ns
$t_{su(sync)}$	PCM_SYNC setup time to PCM_CLK falling		150		ns
$t_{h(sync)}$	PCM_SYNC hold time after PCM_CLK falling		350		ns
$t_{su(din)}$	PCM_DIN setup time to PCM_CLK falling	50			ns
$t_{h(din)}$	PCM_DIN hold time after PCM_CLK falling	10			ns
t_{pdout}	Delay from PCM_CLK falling to PCM_DOUT			50	ns

5.2.2 LCD Timing

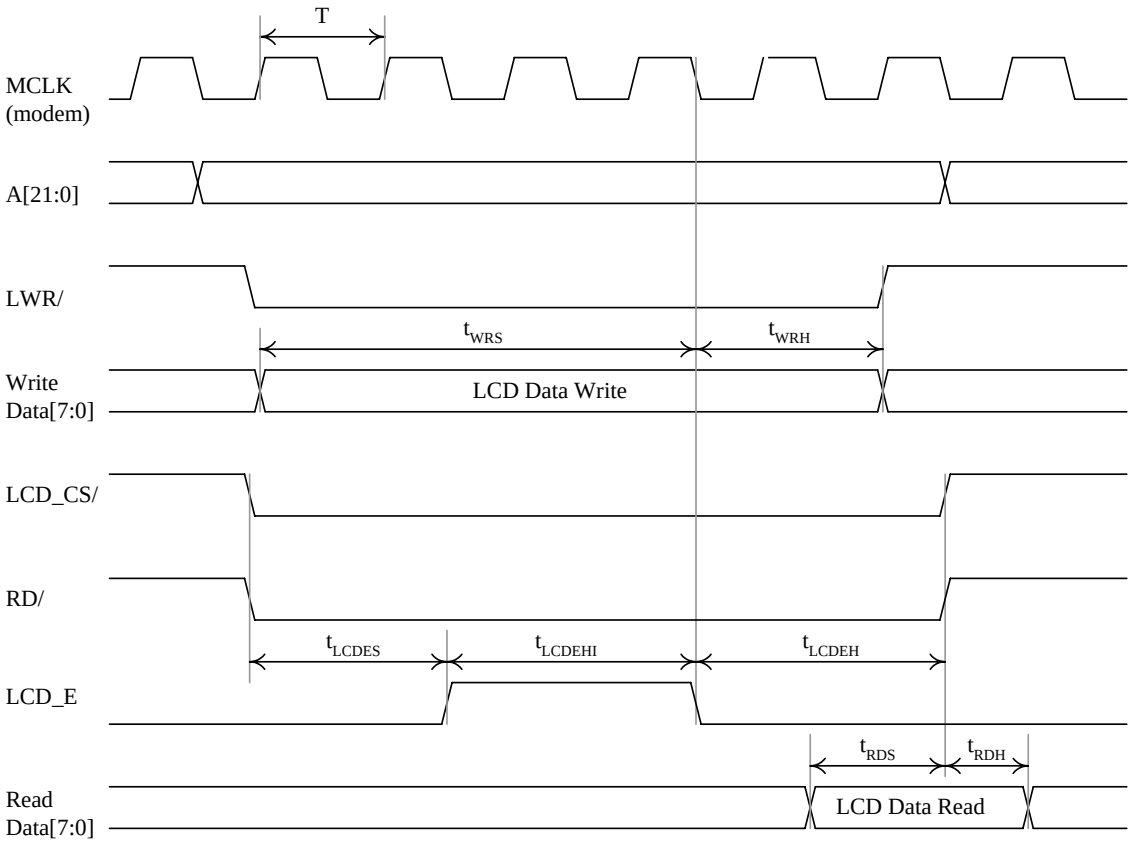


Figure 5-3 LCD Timing

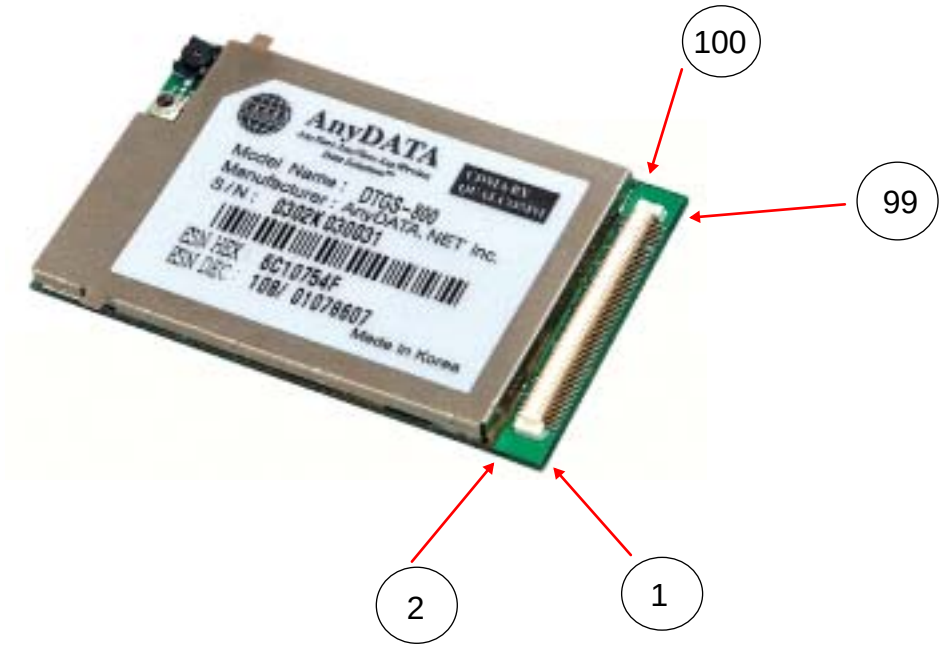
Table 5-3 LCD Timing Parameters

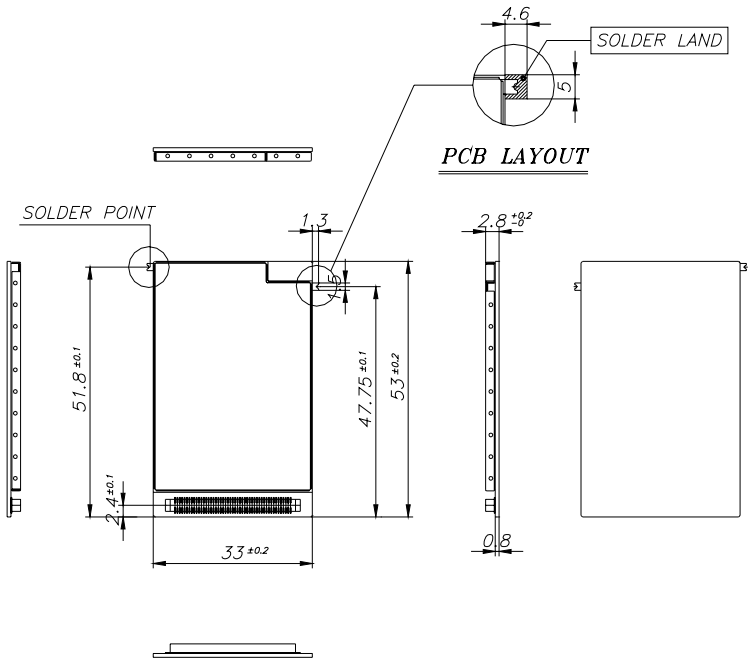
PARAMETER	DESCRIPTION	MIN	MAX	UNIT
t_{LCDES}	LCD_CS/ active to LCD_E active			ns
t_{LCDEHI}	Pulse width if LCD_E active			ns
t_{LCDEH}	LCD_E inactive to LCD_CS/ inactive (write)			ns
t_{LCDEHR}	LCD_E inactive to LCD_CS/ inactive (Read)			
t_{RDS}	Read data setup			ns
t_{RDH}	Read data hold			ns
t_{WRS}	Write data setup to LCD_E inactive			ns
t_{WRH}	Write data hold from LCD_E inactive			ns

- k, I, n is integer lower than 16, MCLK is internal Clock of module

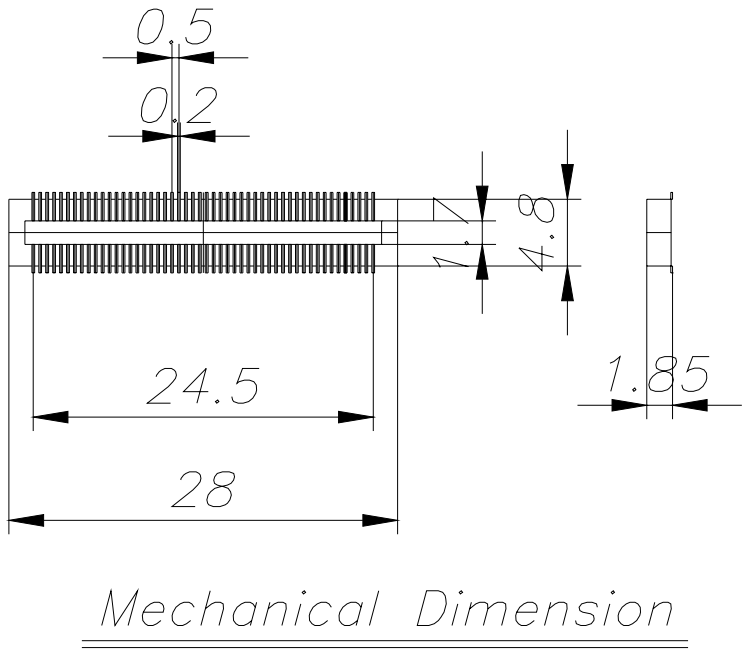
6. Mechanical Dimensions

6.1 DTGS-800 Outline





6.2 100-Pin Connector Mechanical Dimension



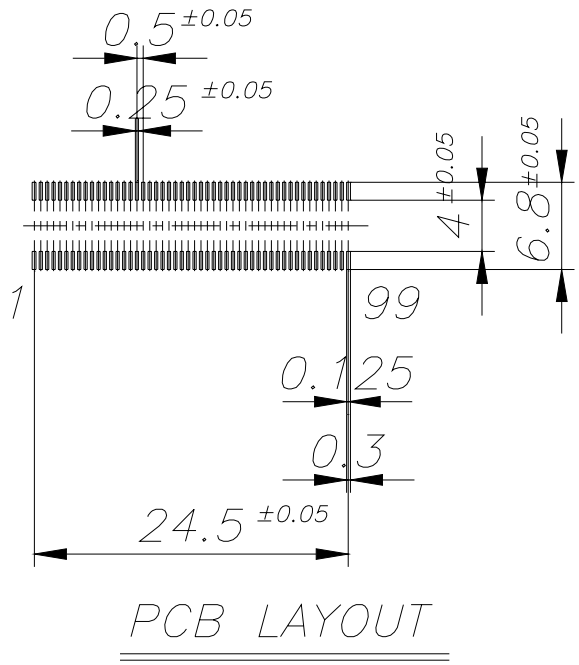


Figure 6-1 100pins Connector (Units: mm)

Counter-Part (the 100-pins socket connector (not on the DTGS-800)):

Part Name: Socket pin connector (0.5mm pitch, straight, dual row)

Part Number: AXK5F00545J

Manufacture : NAIS

Note: For more information on the 100-pins socket connector,

Please refer to: http://www.nais-e.com/ , click connector,

and then “NARROW PITCH(0.5mm) CONNECTORS P5 SERIES P5KF” .

6.3 RF Connector

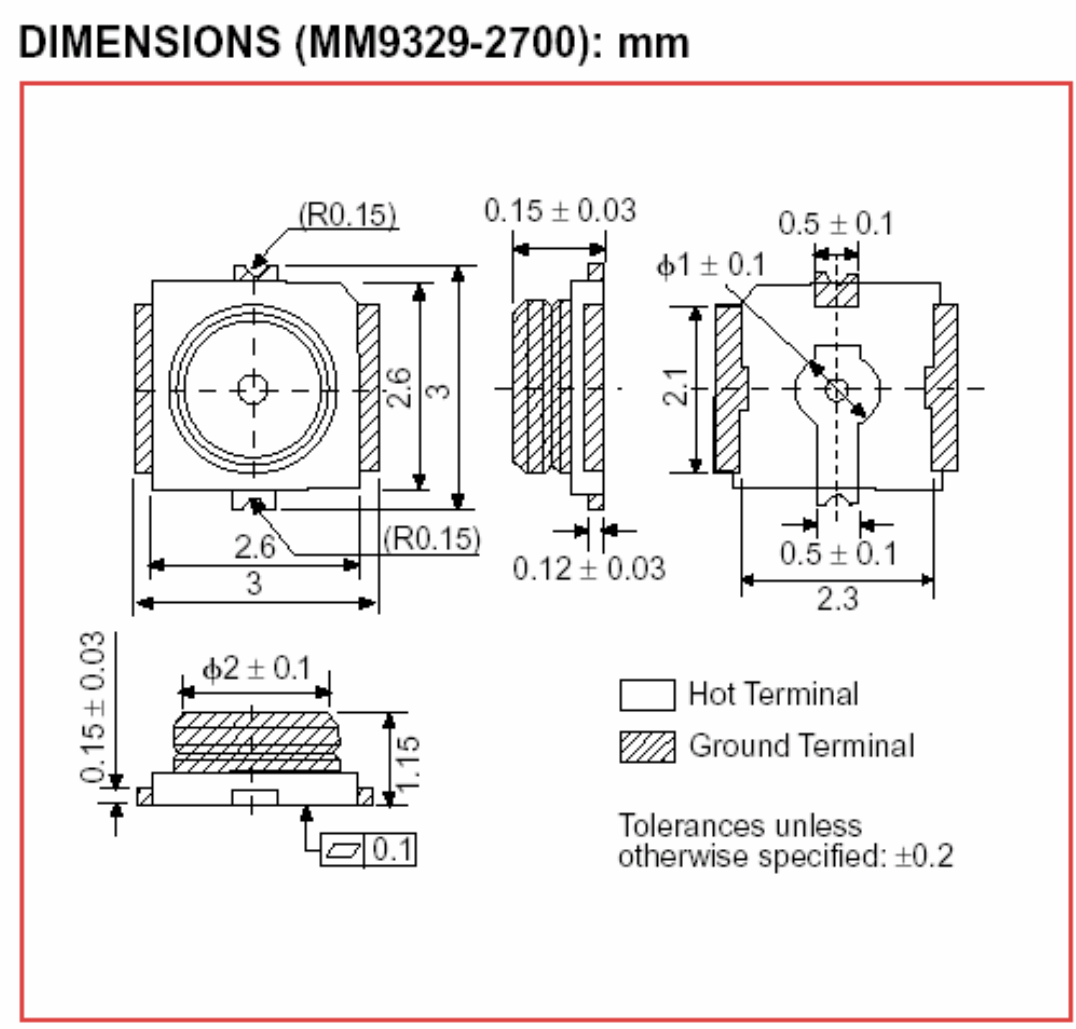


Figure 6-2 RF Connector (GSC type, Units: mm)

Counter-Part (not found on the DTGS-800) used to connect the RF connector to an antenna:

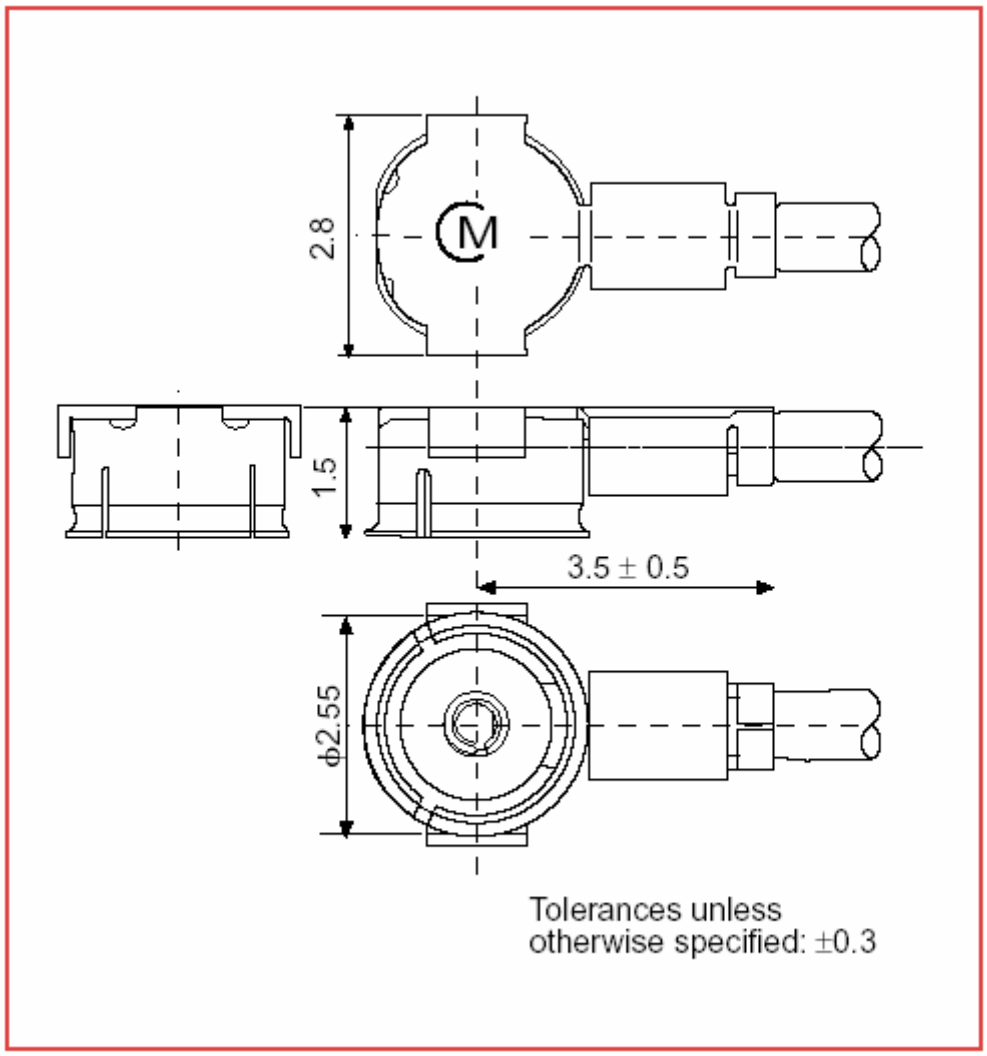


Figure 6-3 Mechanical Characteristics of Cable Harness Assembly (Units: mm)

Part name: Cable Harness Assembly

Note: For more information about the RF connector parts, please refer to the file found at http://www.murata.com/catalog/o30e5.pdf