

Intel (R) IXP435 Multi-Service Residential Gateway Reference Platform

| PAGE # | PAGE TITLE |
|--------|--------------------------------|
| 1 | PAGE 1 TITLE PAGE |
| 2 | PAGE 2 BLOCK DIAGRAM |
| 3 | PAGE 3 IXP435_ETH_SYS_SSP_JTAG |
| 4 | PAGE 4 IXP435_EXPB_USB20_HSS |
| 5 | PAGE 5 IXP435_PCI_GPIO |
| 6 | PAGE 6 IXP435_DDRII_URT |
| 7 | PAGE 7 IXP435_POWER |
| 8 | PAGE 8 NAND_NOR_LED |
| 9 | PAGE 9 DDRII RAM |
| 10 | PAGE10 DDRII TERMINATIONS |
| 11 | PAGE11 MINI PCI_1_2 |
| 12 | PAGE12 PCI SLOT |
| 13 | PAGE13 PCI CLK_RESET |
| 14 | PAGE14 SLIC A_B |
| 15 | PAGE15 FXO |
| 16 | PAGE16 POWER |
| 17 | PAGE17 ETH_CONNECTORS |
| 18 | PAGE18 LAN |
| 19 | PAGE19 MII UTOPIA CONNECTORS |
| 20 | PAGE20 UART_IR-JTAG |
| 21 | PAGE21 PNX POWER |
| 22 | PAGE22 PNX PCI & XIO |
| 23 | PAGE23 PNX DDR_MEM |
| 24 | PAGE24 PNX ETHERNET_GPIO |
| 25 | PAGE25 PNX VIDEO_VIDEO OUT |
| 26 | PAGE26 PNX VIDEO_VIDEO IN |
| 27 | PAGE27 PNX AUDIO_AUDIO OUT |
| 28 | PAGE28 PNX AUDIO_AUDIO IN |

| REV | DATE | DESCRIPTION |
|-----|------------|-----------------|
| 0.1 | 2006-01-25 | Initial version |
| 0.2 | 2006-02-16 | Version 0.2 |
| 0.3 | 2006-03-21 | Version 0.3 |
| 0.4 | 2006-05-04 | Version 0.4 |
| 1.0 | 2006-08-22 | Version 1.0 |
| 1.1 | 2006-12-21 | Version 1.1 |


NOTE

(1) DNP means----> do not populate component

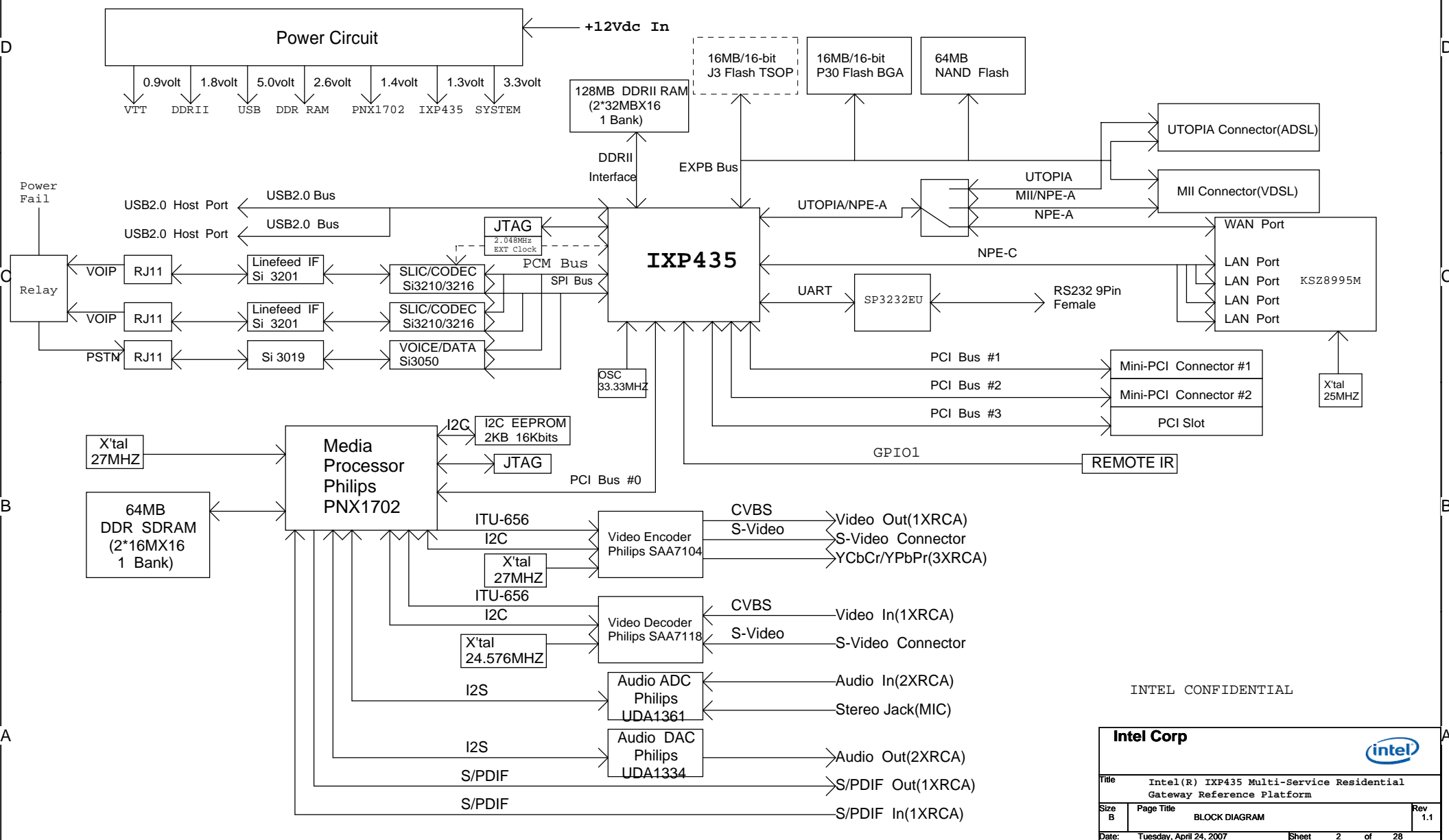
THIS DOCUMENT IS PROVIDED "AS IS" WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, NONINFRINGEMENT, FITNESS FOR ANY PARTICULAR PURPOSE, OR ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATION OR SAMPLE. INTEL DISCLAIMS ALL LIABILITY, INCLUDING LIABILITY FOR INFRINGEMENT OF ANY PROPRIETARY RIGHTS, RELATING TO USE OF INFORMATION IN THIS DOCUMENT AND NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED HEREIN. INTEL CORPORATION ASSUMES NO RESPONSIBILITY OR LIABILITY FOR ANY ERRORS OR INACCURACIES THAT MAY APPEAR IN THIS DOCUMENT OR ANY SOFTWARE THAT MAY BE PROVIDED IN ASSOCIATION WITH THIS DOCUMENT. THE INFORMATION IN THIS DOCUMENT IS FURNISHED FOR INFORMATIONAL USE ONLY, IS SUBJECT TO CHANGE WITHOUT NOTICE, AND SHOULD NOT BE CONSTRUED AS A COMMITMENT BY INTEL CORPORATION.

INTEL CONFIDENTIAL

INTEL CONFIDENTIAL

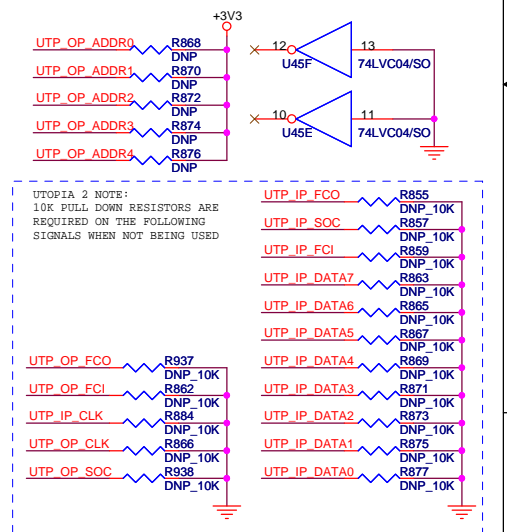
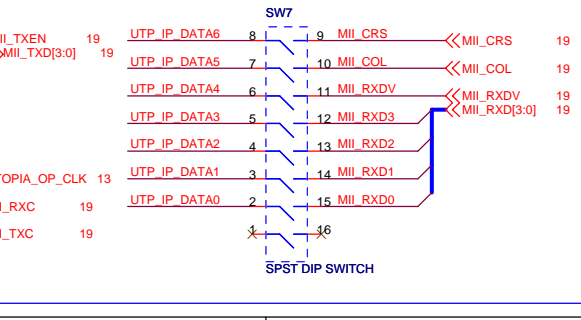
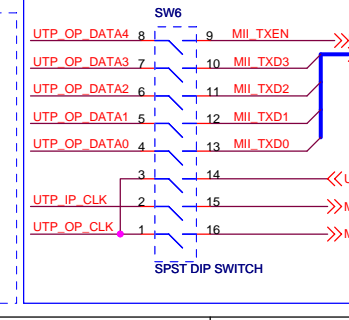
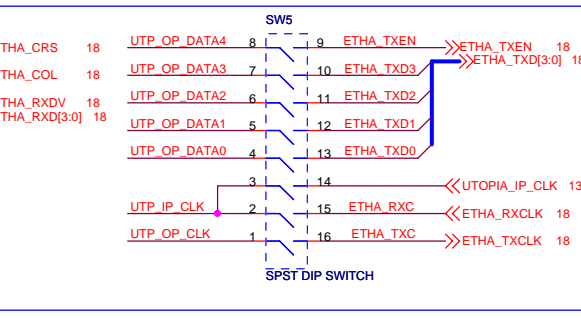
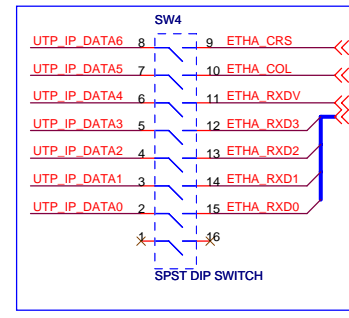
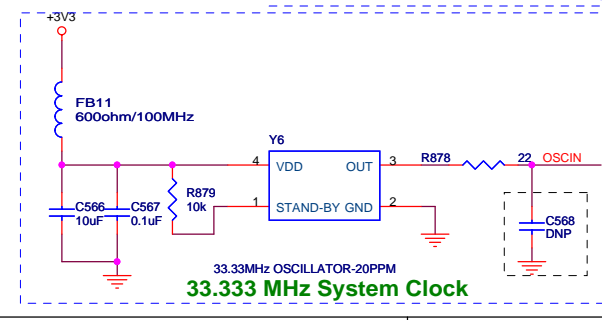
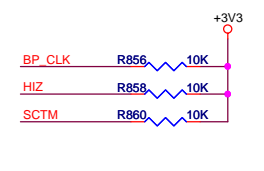
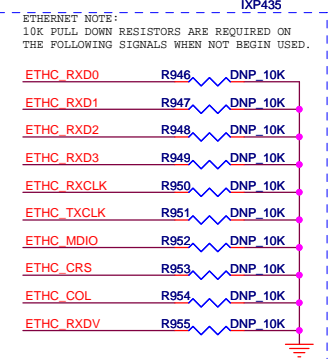
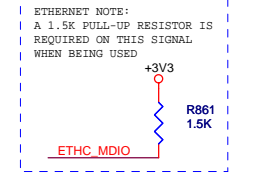
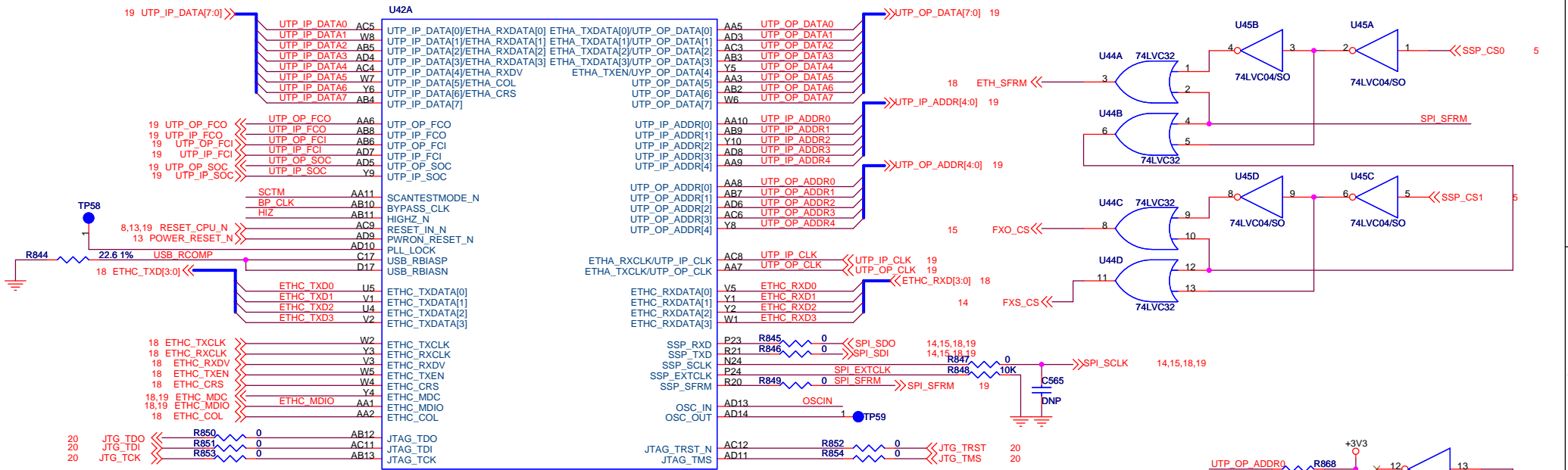
| | | |
|--|-----------------------|---|
| Intel Corp | |  |
| Title Intel(R) IXP435 Multi-Service Residential Gateway Reference Platform | | |
| Size B | Page Title TITLE PAGE | Rev 1.1 |
| Date: Tuesday, April 24, 2007 | Sheet 1 | of 28 |

Intel(R) IXP435 Multi-Service Residential Gateway Reference Platform



INTEL CONFIDENTIAL

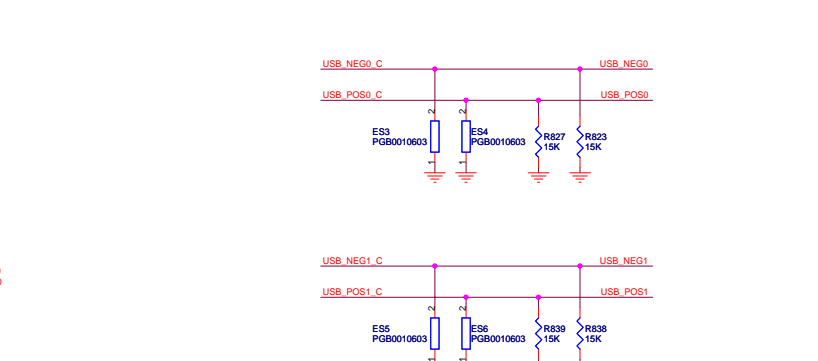
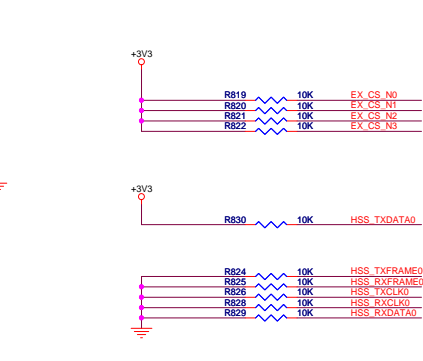
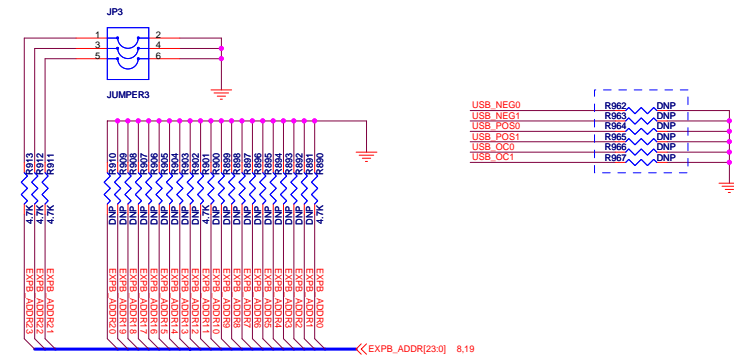
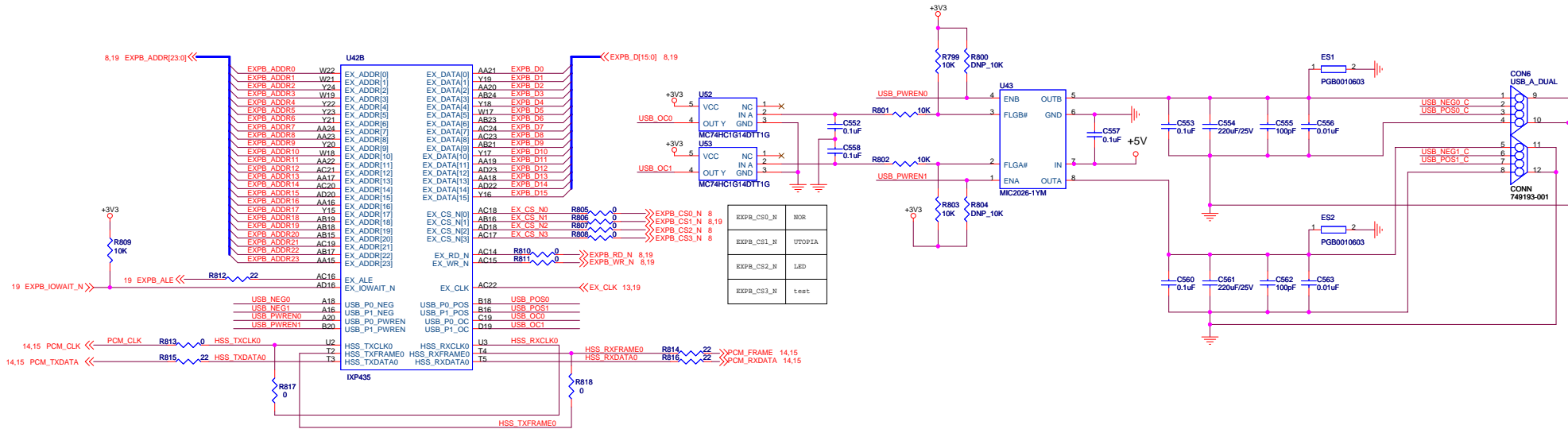
| | | |
|---|---------------------------|----------|
| Intel Corp | | |
| Title: Intel(R) IXP435 Multi-Service Residential Gateway Reference Platform | | |
| Size: B | Page Title: BLOCK DIAGRAM | Rev: 1.1 |
| Date: Tuesday, April 24, 2007 | Sheet: 2 of 28 | |



INTEL CONFIDENTIAL

Intel Corp

| | | |
|---|-------------------------------------|---------|
| Title: Intel(R) IXP435 Multi-Service Residential Gateway Reference Platform | | |
| Size B | Page Title: IXP435_ETH_SYS_SSP_UTAG | Rev 1.1 |
| Date: Tuesday, April 24, 2007 | Sheet 3 | of 28 |



| CHIP SPEED | A23 | A22 | A21 | Function: Clock set |
|------------|-----|-----|-----|---------------------|
| 667MHz | 0 | 0 | 0 | 667MHz |
| 667MHz | 0 | 0 | 1 | 533MHz |
| 667MHz | 0 | 1 | 1 | 400MHz |
| 667MHz | 0 | 1 | 0 | 266MHz |
| 533MHz | 0 | 0 | 1 | 533MHz |
| 533MHz | 0 | 1 | 1 | 400MHz |
| 533MHz | 0 | 1 | 0 | 266MHz |
| 400MHz | 0 | 0 | 1 | 400MHz |
| 400MHz | 0 | 1 | 0 | 266MHz |
| 266MHz | 0 | 0 | 0 | 266MHz |

| A0 | FLASH Width | A1 | PCI_HOST | A10 | IOWAIT_CS0 |
|-----|-----------------------|------------------------------|-------------------------------|--|---|
| 0 | 16 bit (default) | 0 | PCI as non-host | 0 | EX_IOWAIT_N is ignored for read and write cycles to Chip select 0 if EXP_TIMING_CS0 is configured to intel mode |
| 1 | 8bit | 1 | PCI as host (default) | 1 | EX_IOWAIT_N is sampled during the read/write Expansion bus cycles (default) |
| A11 | DDR1 or DDR2 mode | A2 | PCI_ARB | | |
| 0 | DDR1(400MHz)(default) | 0 | PCI arbiter disabled | | |
| 1 | DDR1(266MHz) | 1 | PCI arbiter enabled (default) | | |
| A9 | A5 | Expansion bus drive strength | A8 | USB CLOCK | |
| 0 | 0 | Reserved | 0 | USB Host clock 48MHz is generated from GP10[1] | |
| 0 | 1 | Medium Drive | 0 | USB Host clock is generated internally (default) | |
| 1 | 0 | Low Drive | 1 | | |
| 1 | 1 | High Drive (Default) | | | |

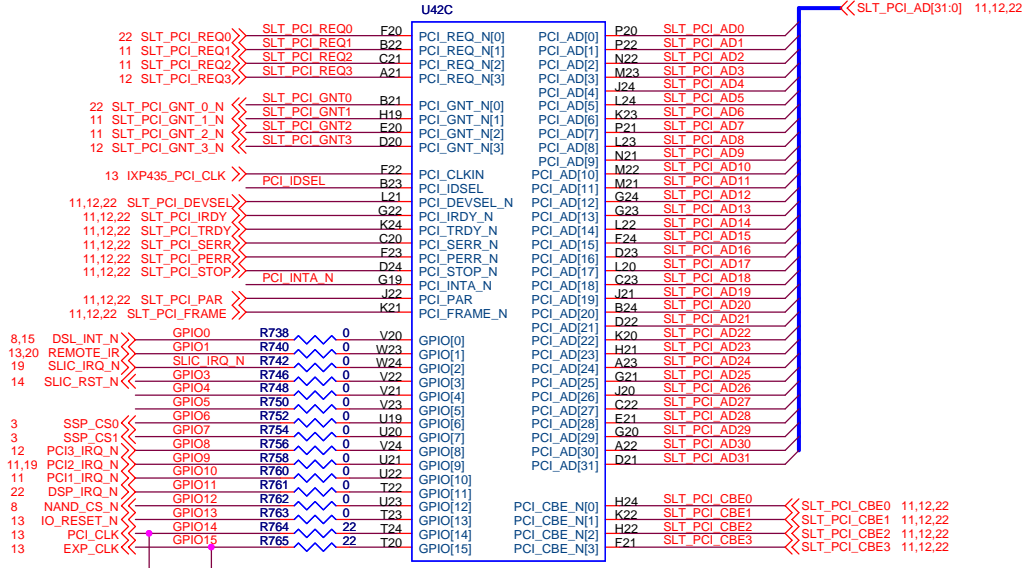
INTEL CONFIDENTIAL

Intel Corp

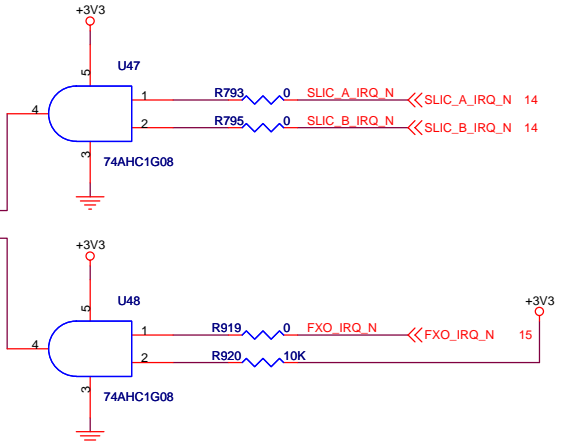
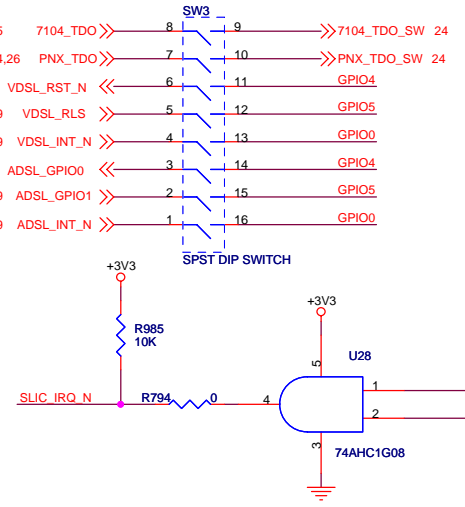
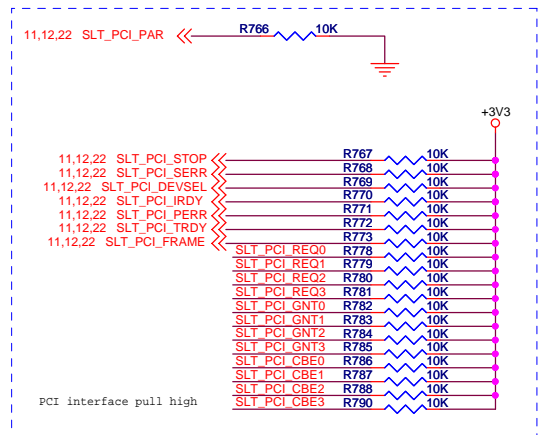
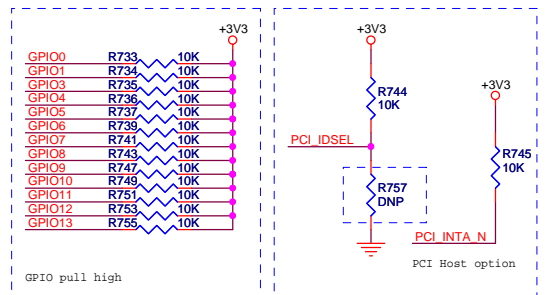
Title: Intel(R) IXP435 Multi-Service Residential Gateway Reference Platform

Size C Page Title: IXP435_EXP_USB20_HSS Rev 1.1

Date: Tuesday, April 24, 2007 Sheet 4 of 28



NOTES:
 USE ADSL MODULE:1,2,3 ON.(DEFAULT)
 USE VDSL MODULE:4,5,6 ON.
 USE PHILIPS TOOL:7 ON AND 8 OFF.(DEFAULT)
 USE CORELIS TOOL:7 OFF AND 8 ON.



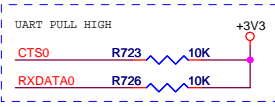
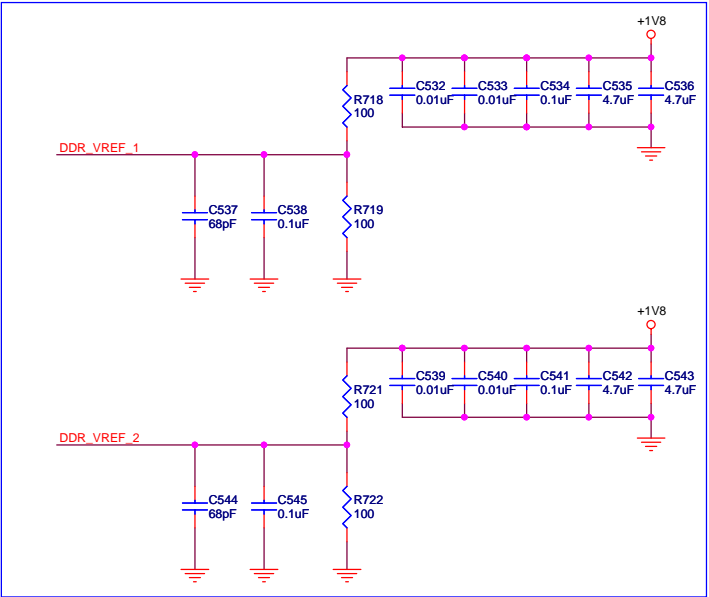
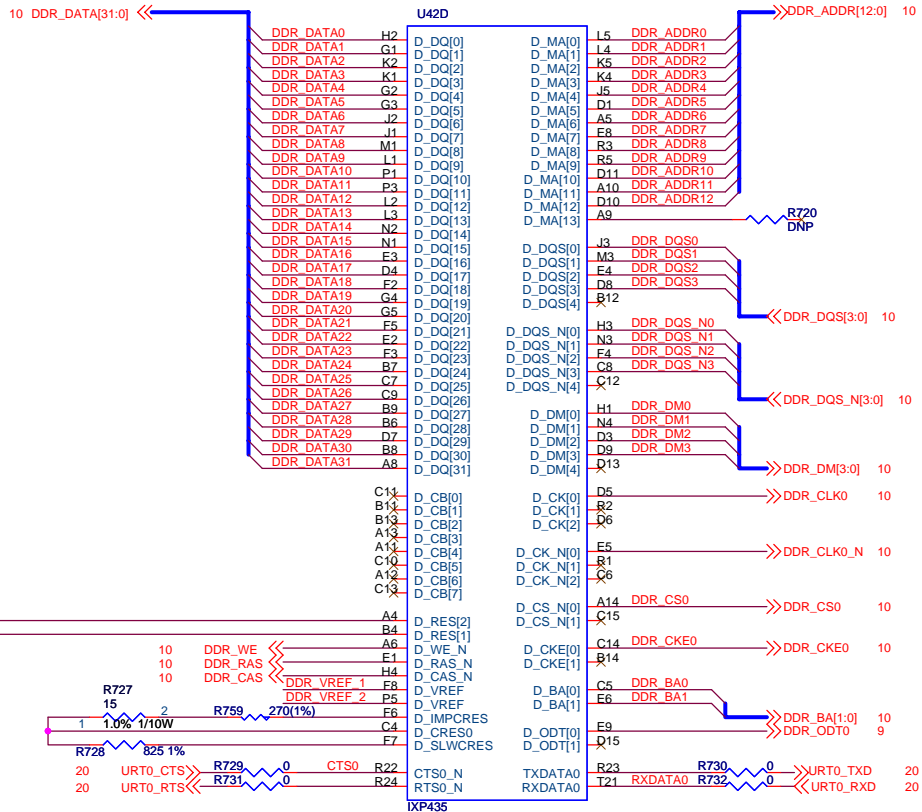
INTEL CONFIDENTIAL

Intel Corp

Title: Intel(R) IXP435 Multi-Service Residential Gateway Reference Platform

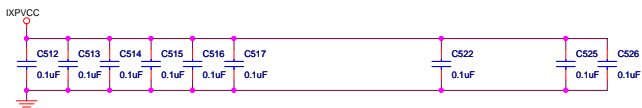
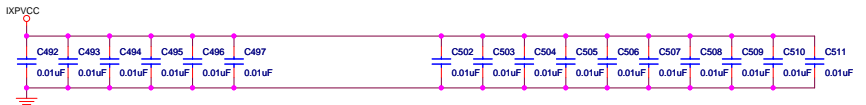
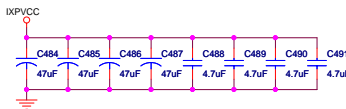
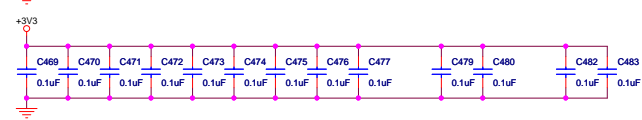
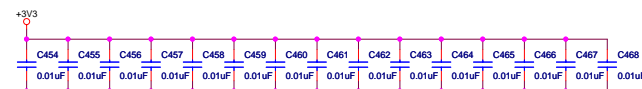
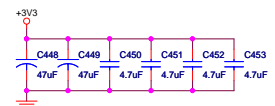
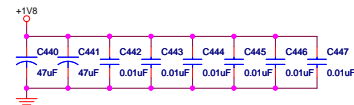
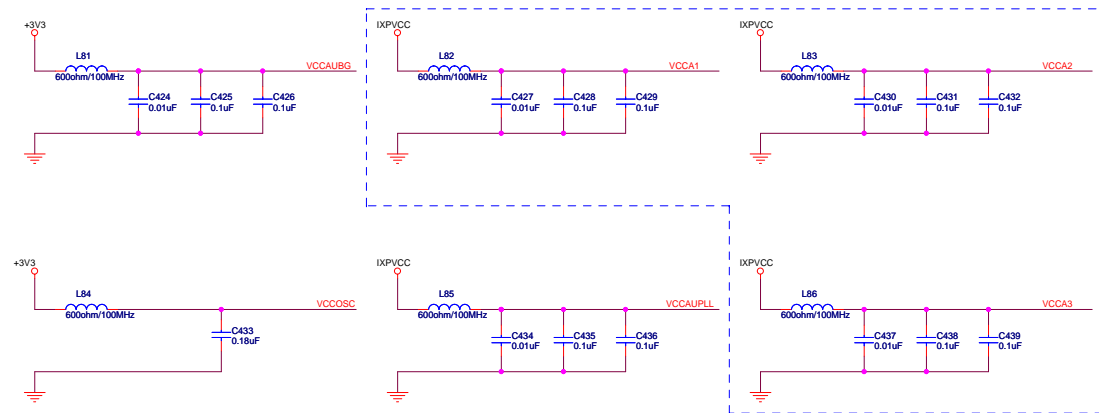
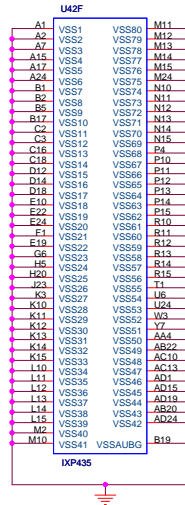
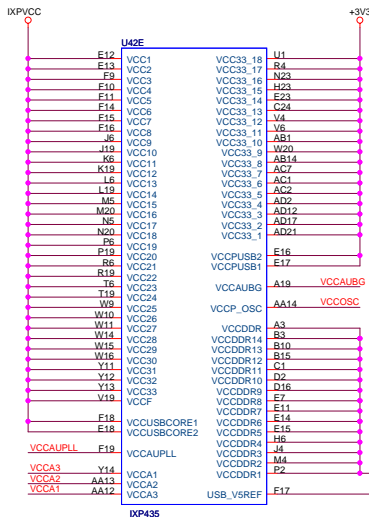
Size B Page Title: IXP435_PCI_GPIO Rev 1.1

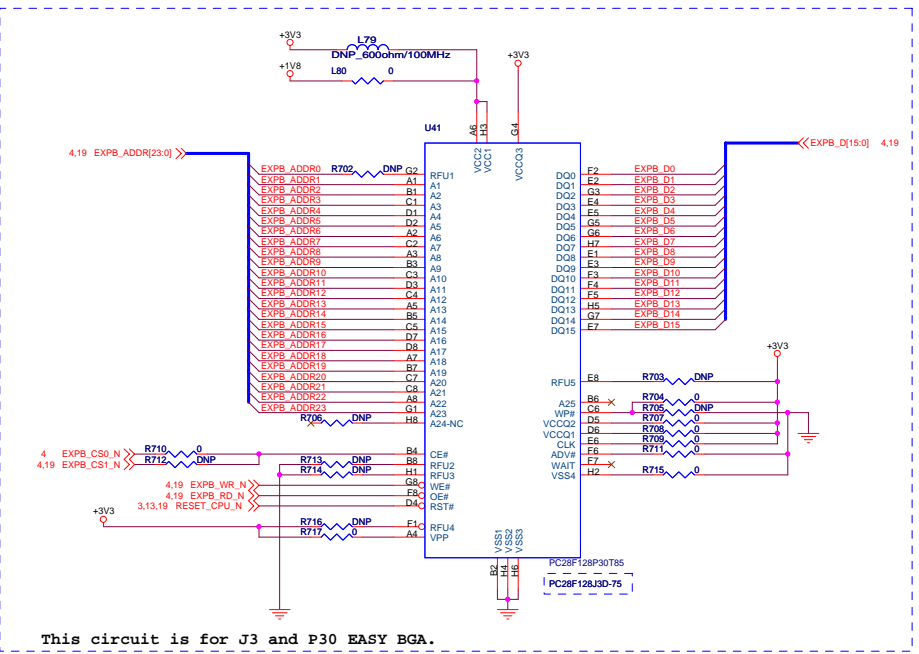
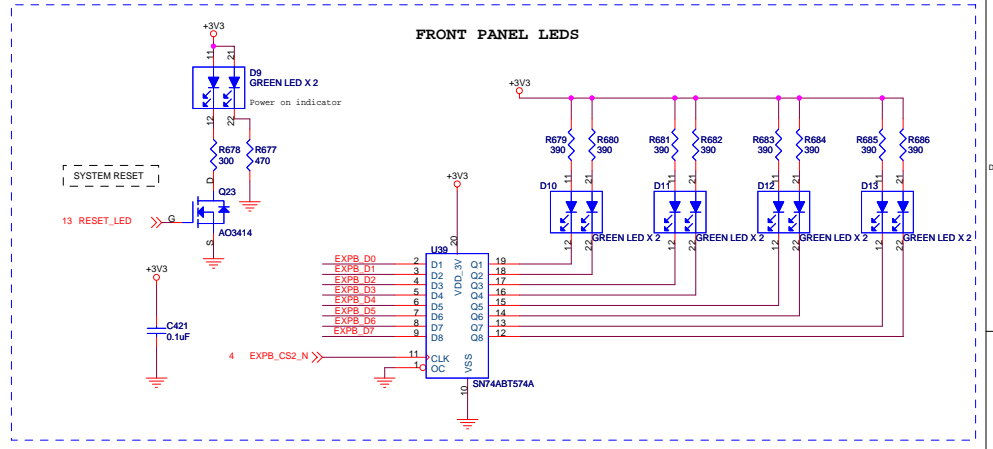
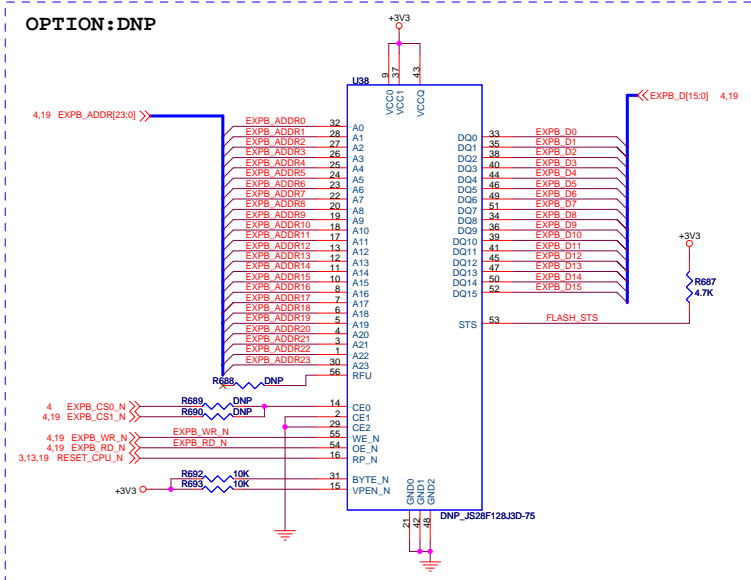
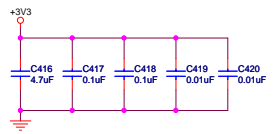
Date: Tuesday, April 24, 2007 Sheet 5 of 28



INTEL CONFIDENTIAL

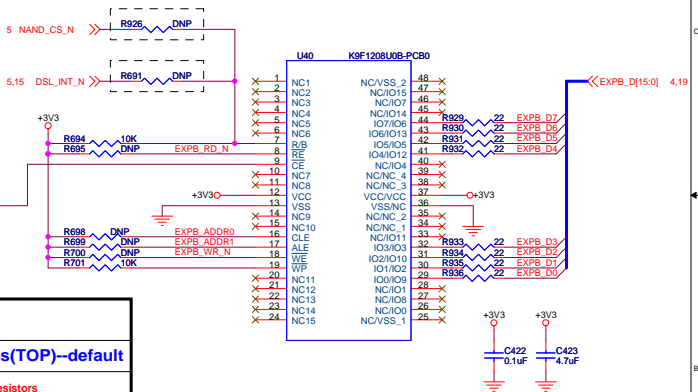
| | | |
|--|-----------------------------|---------|
| Intel Corp | | |
| Title Intel(R) IXP435 Multi-Service Residential Gateway Reference Platform | | |
| Size B | Page Title IXP435_DDRIL_URT | Rev 1.1 |
| Date: Tuesday, April 24, 2007 | Sheet 6 | of 28 |





Resistor Settings for Intel's Flash Memory

| J3 Strata Series | P30 Series(TOP)-default |
|---|--|
| Do not mount the following resistors R704,R705,R707,R708,R709,R711,R715 | Do not mount the following resistors R703,R713,R714,R716 |
| Resistors must be mounted : R703,R713,R714,R716 | Resistors must be mounted : R707,R708,R709,R711,R715 |
| Setting : L79 must be mounted and L80 must be DNP | Setting : L80 must be mounted and L79 must be DNP |
| HW Lock : Not supported | HW Lock : Unlock : R704 must be mounted, and R705 is left blank. Lock : R705 must be mounted, and R704 is left blank. |



This circuit is for J3 and P30 EASY BGA.

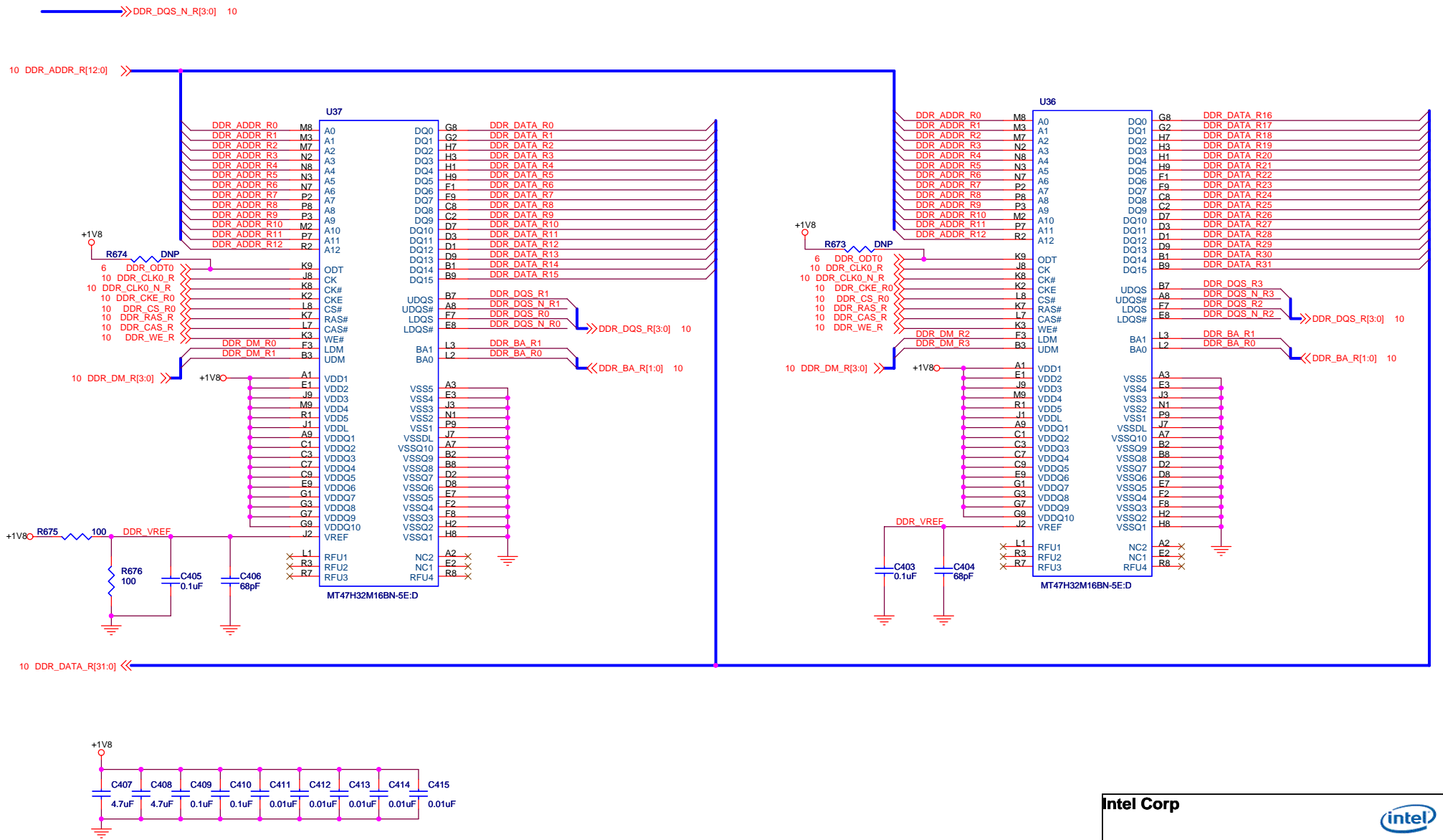
INTEL CONFIDENTIAL

Intel Corp

Title: Intel(R) IXP435 Multi-Service Residential Gateway Reference Platform

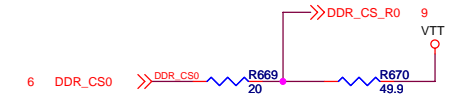
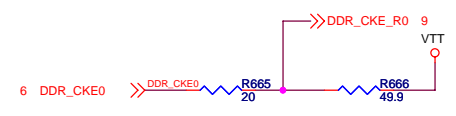
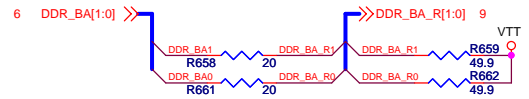
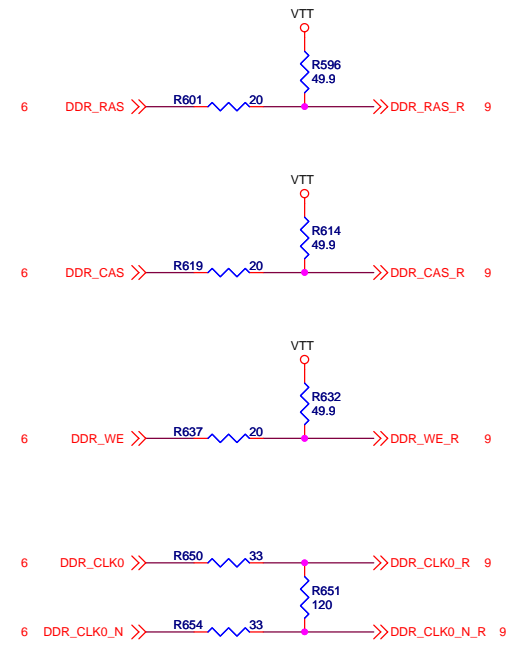
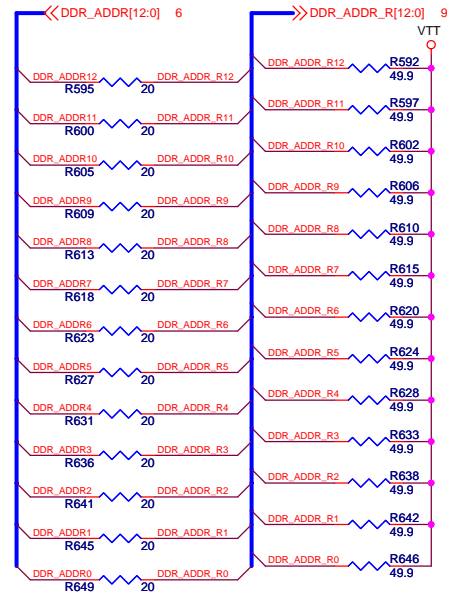
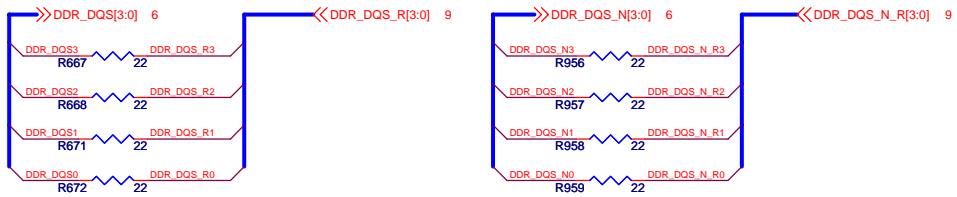
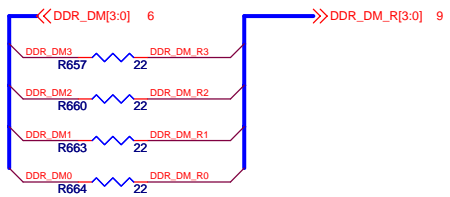
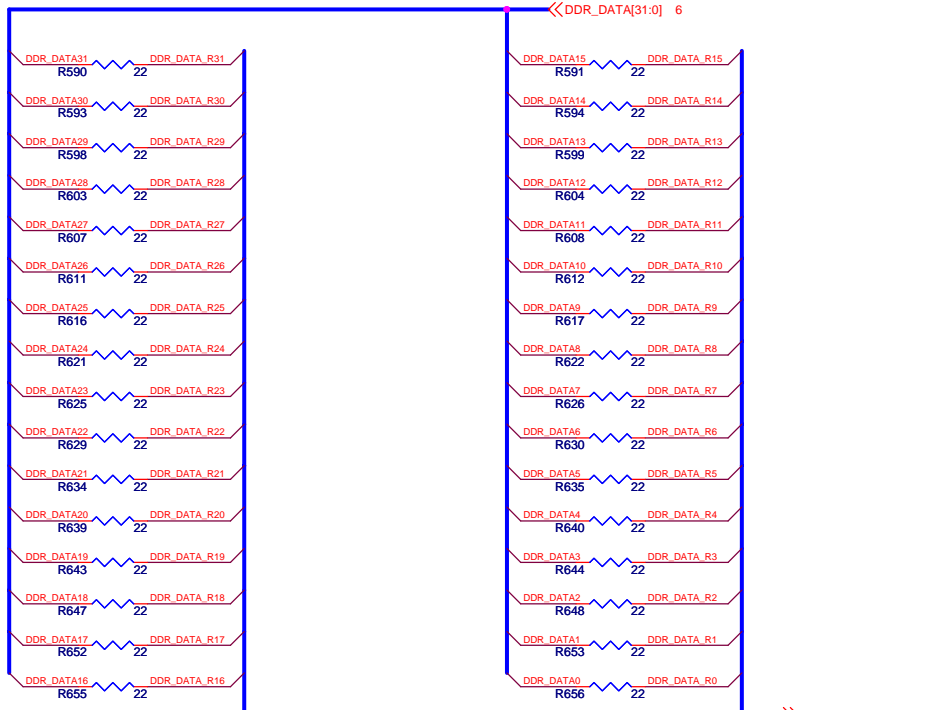
Size: Custom Page Title: NAND_NOR_LED Rev: 1.1

Date: Tuesday, April 24, 2007 ESheet: 8 of 28



INTEL CONFIDENTIAL

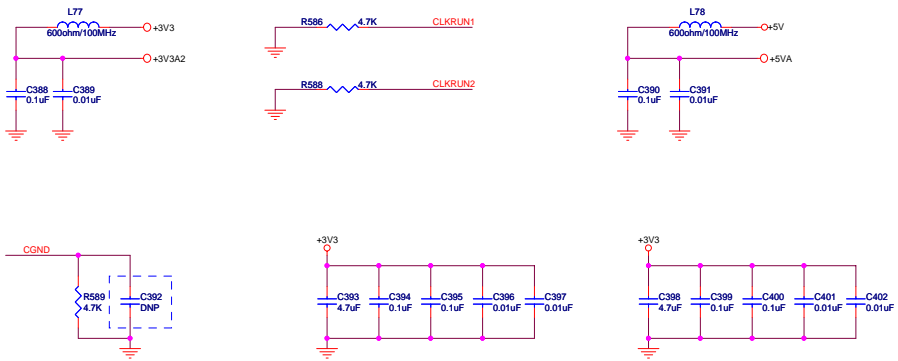
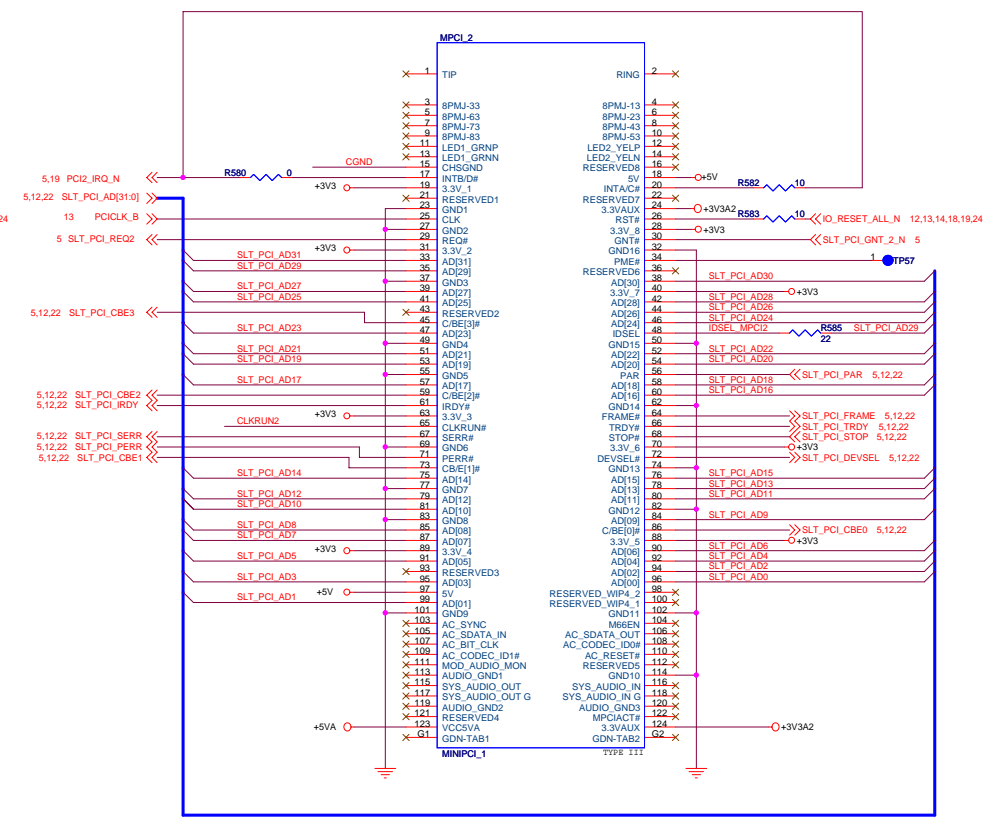
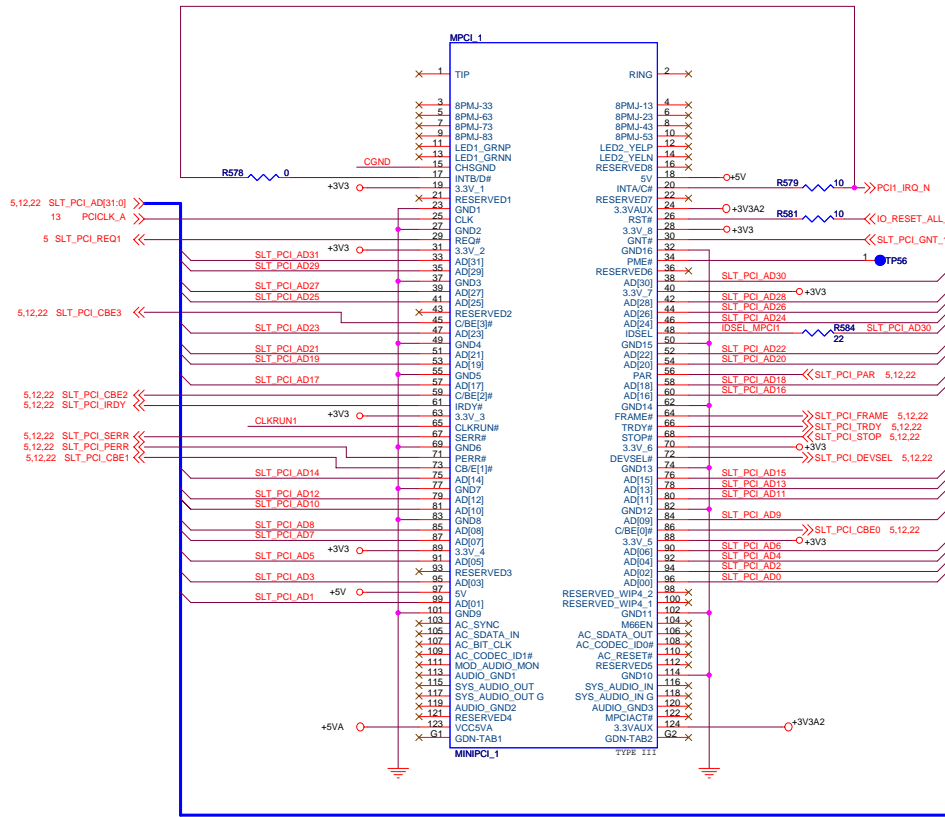
| | | |
|--|----------------------|---------|
| Intel Corp | | |
| Title Intel(R) IXP435 Multi-Service Residential Gateway Reference Platform | | |
| Size B | Page Title DDRII RAM | Rev 1.1 |
| Date: Tuesday, April 24, 2007 | Sheet 9 of 28 | |



DDRII TERMINATIONS

INTEL CONFIDENTIAL

| | | |
|--|-------------------------------|---------|
| Intel Corp | | |
| Title Intel(R) IXP435 Multi-Service Residential Gateway Reference Platform | | |
| Size B | Page Title DDRII TERMINATIONS | Rev 1.1 |
| Date: Tuesday, April 24, 2007 | Sheet 10 of 28 | |



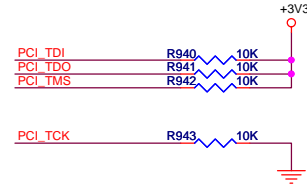
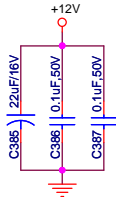
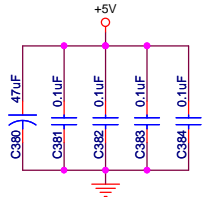
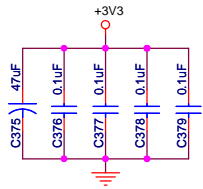
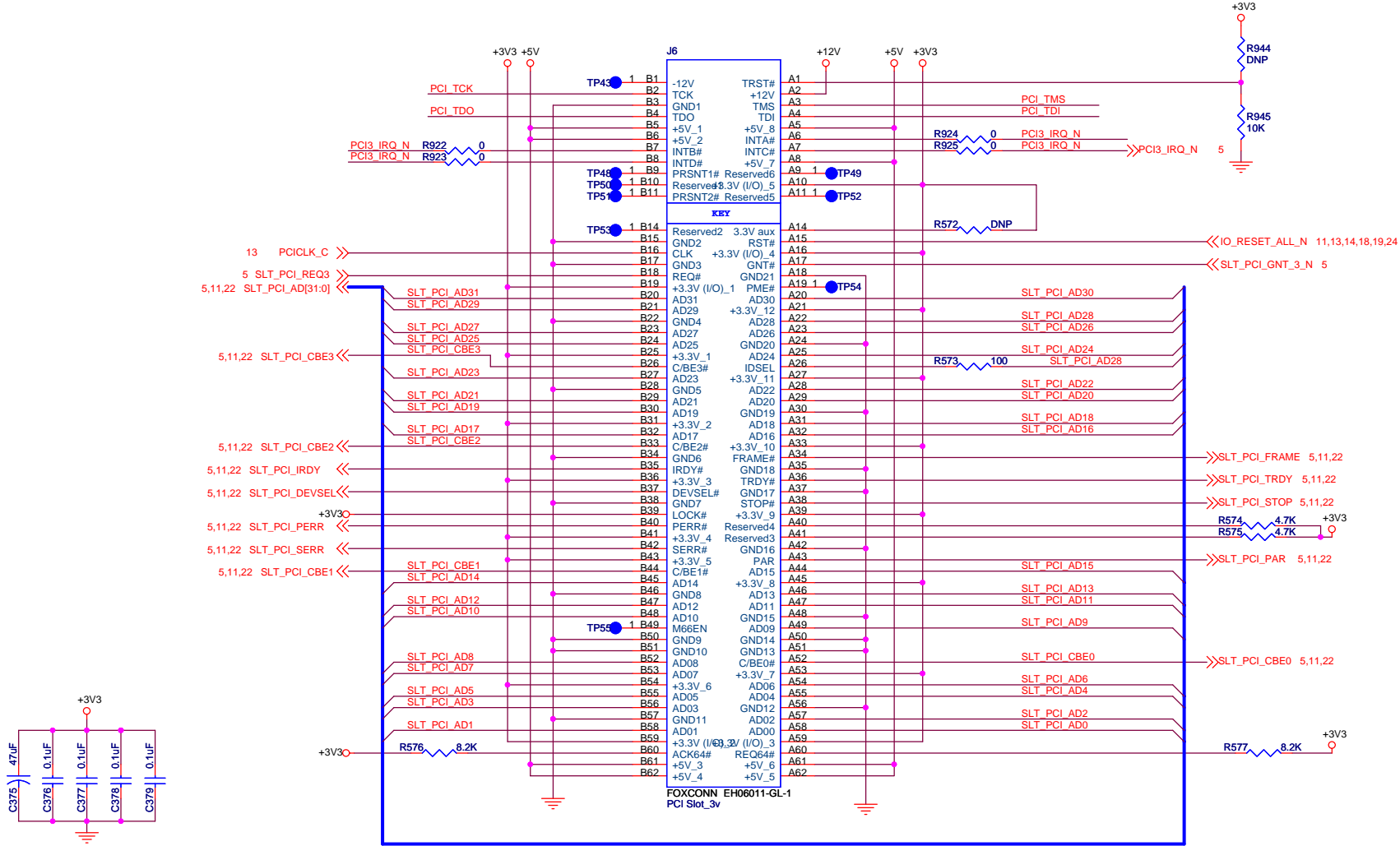
INTEL CONFIDENTIAL

Intel Corp

File: Intel(R) IXP435 Multi-Service Residential Gateway Reference Platform

Size: C Page Title: MINI PCI_1_2 Rev: 1.1

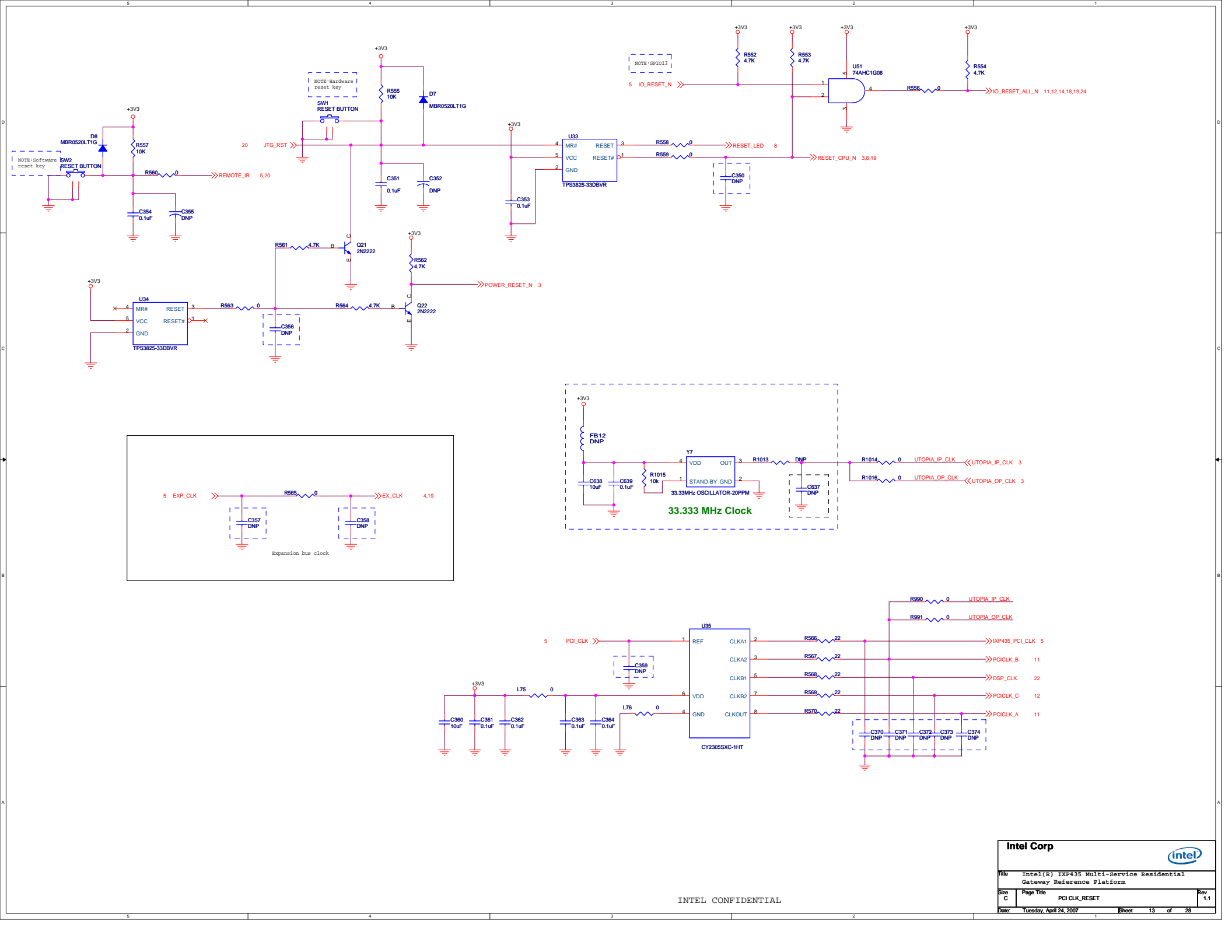
Date: Tuesday, April 24, 2007 Sheet: 11 of 28

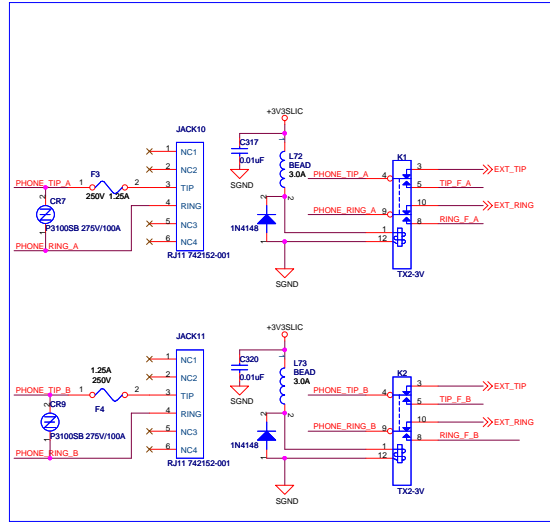
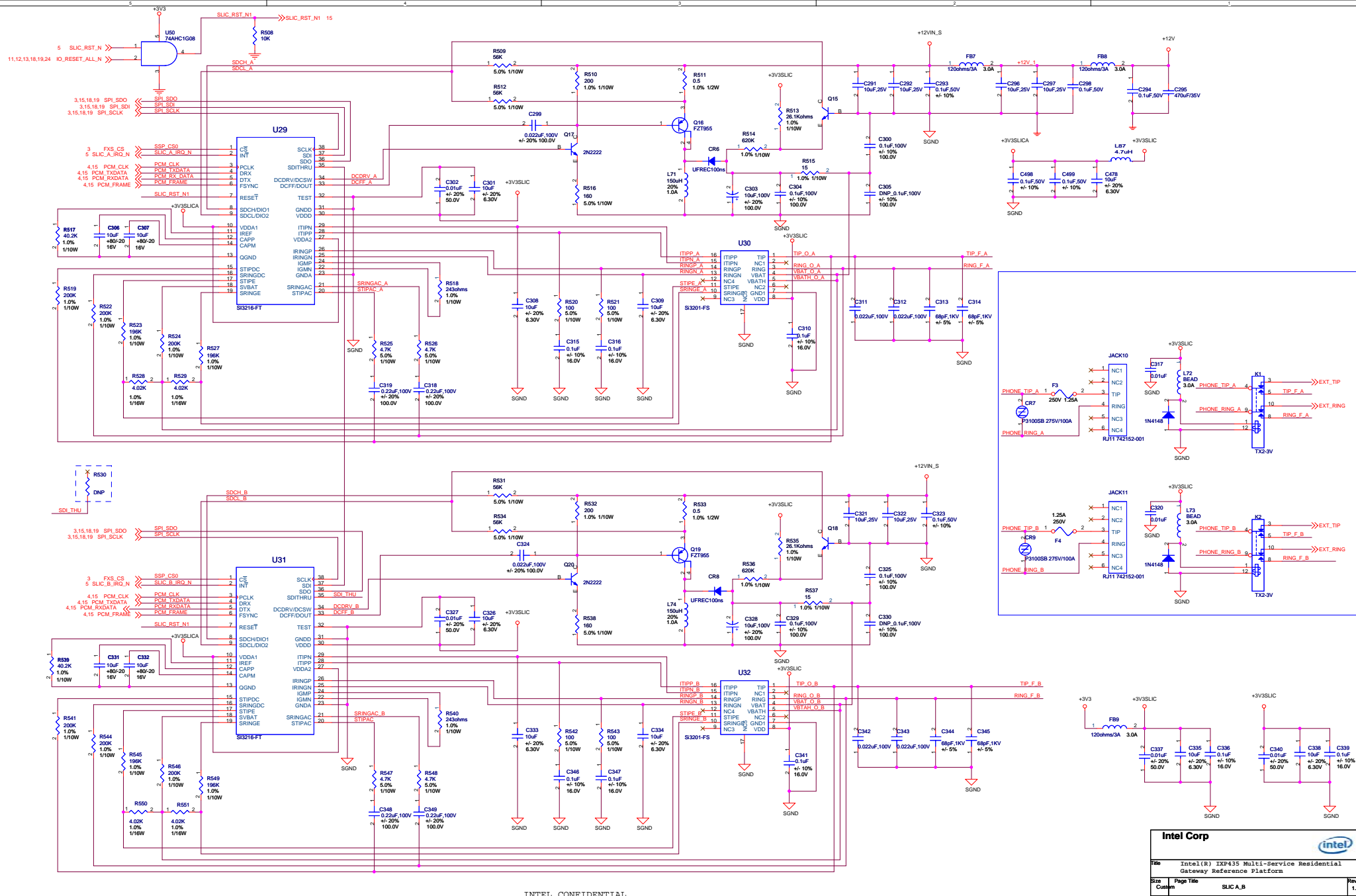


FOXCONN EH06011-GL-1
PCI Slot_3v

INTEL CONFIDENTIAL

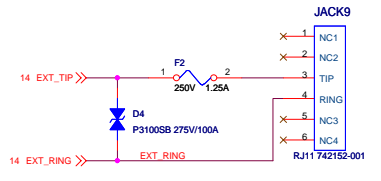
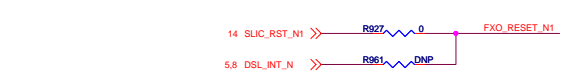
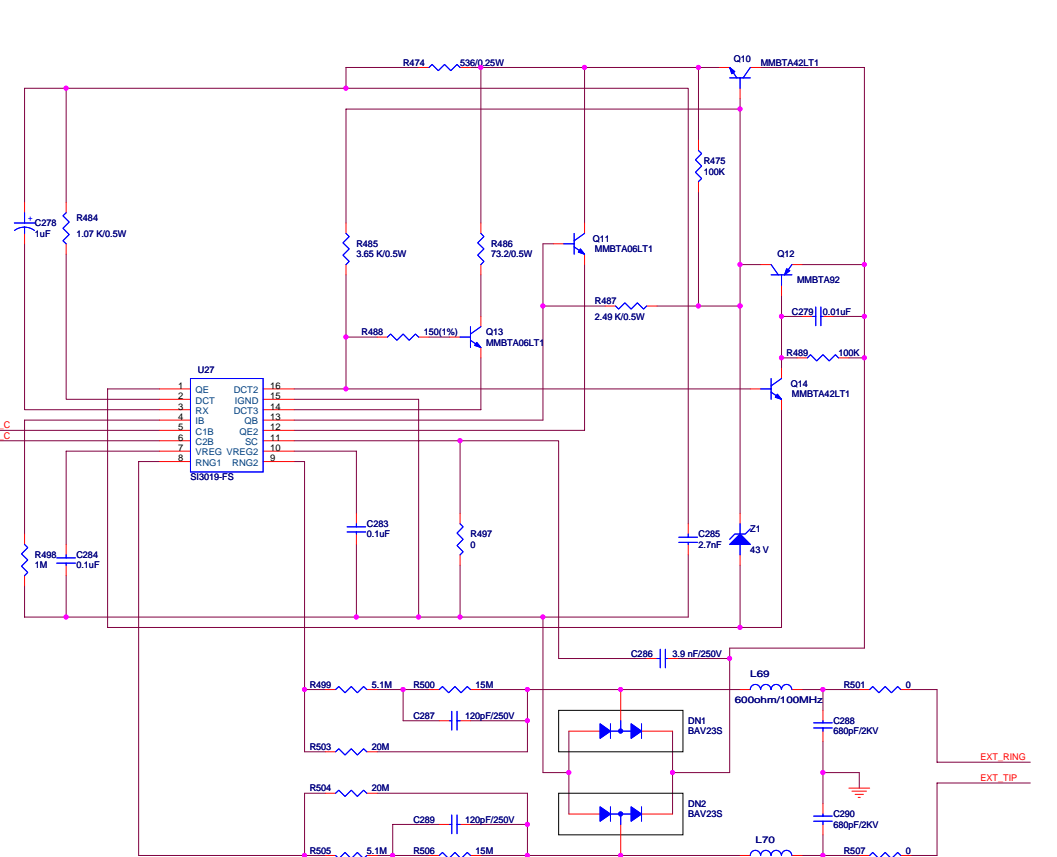
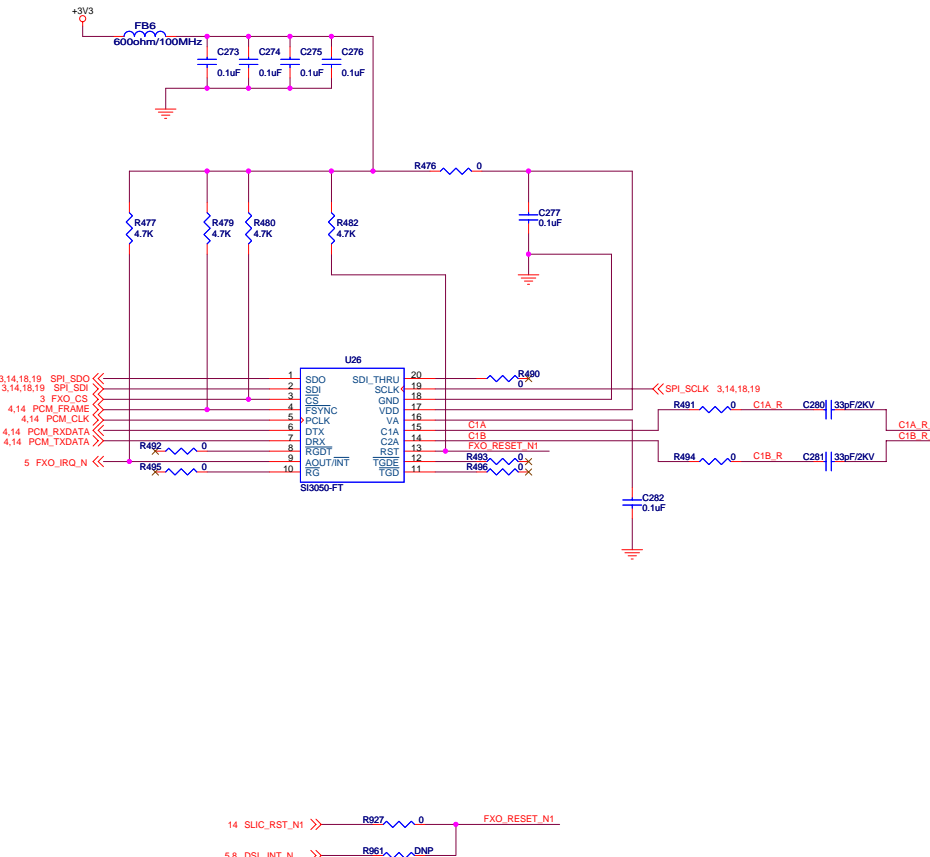
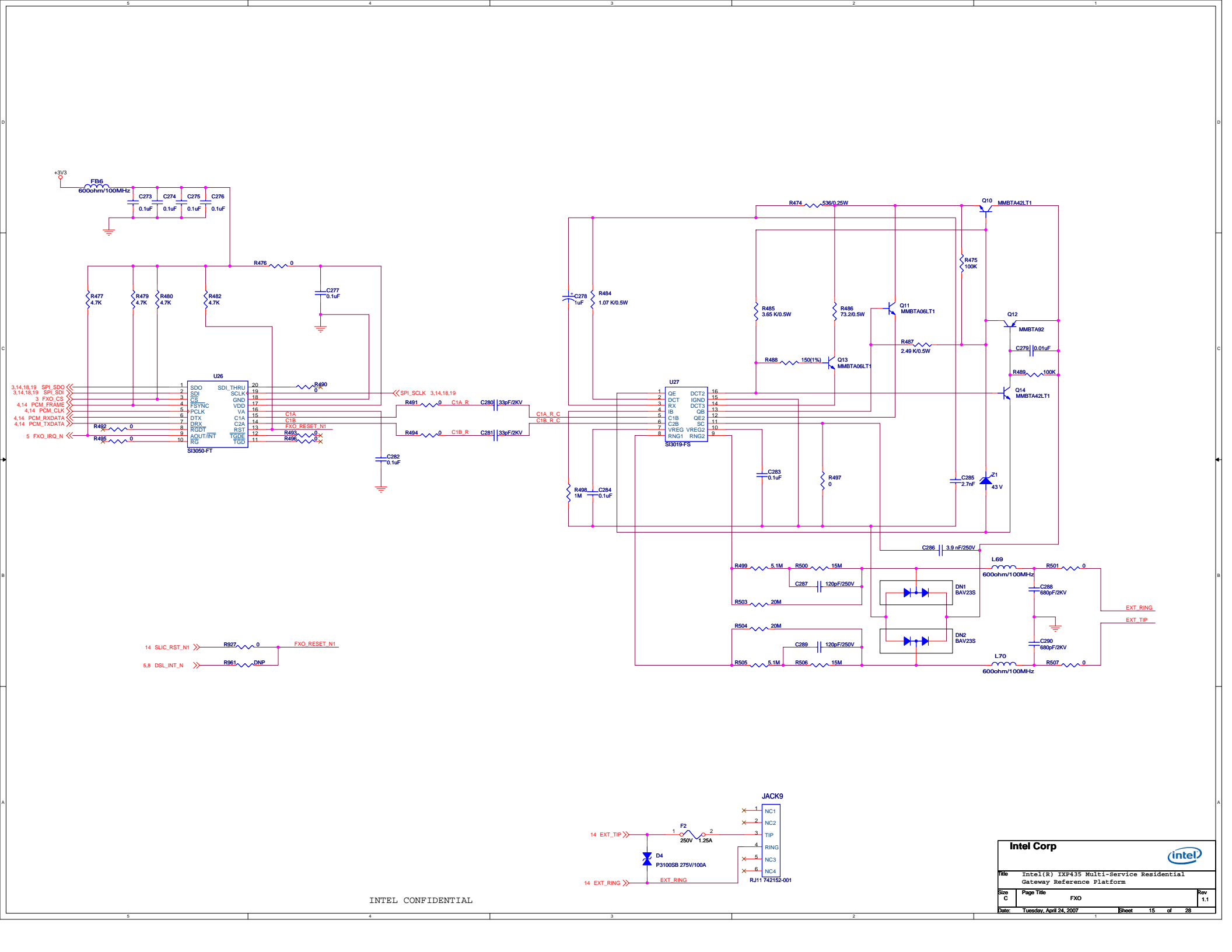
| | | | |
|--|-------------------------|----------|---------|
| Intel Corp | | | |
| Title Intel(R) IXP435 Multi-Service Residential Gateway Reference Platform | | | |
| Size B | Page Title | PCI SLOT | Rev 1.1 |
| Date: | Tuesday, April 24, 2007 | Sheet 12 | of 28 |





| | | | |
|--|------------|----------------|--|
| Intel Corp | | | |
| Title Intel(R) IXP435 Multi-Service Residential Gateway Reference Platform | | | |
| Size | Page Title | Rev | |
| Count | SLIC_A_B | 1.1 | |
| Date: Tuesday, April 24, 2007 | | Sheet 14 of 28 | |

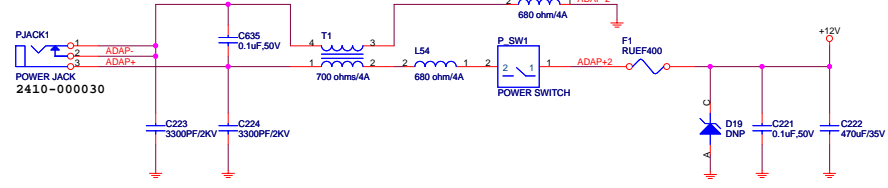
INTEL CONFIDENTIAL



INTEL CONFIDENTIAL

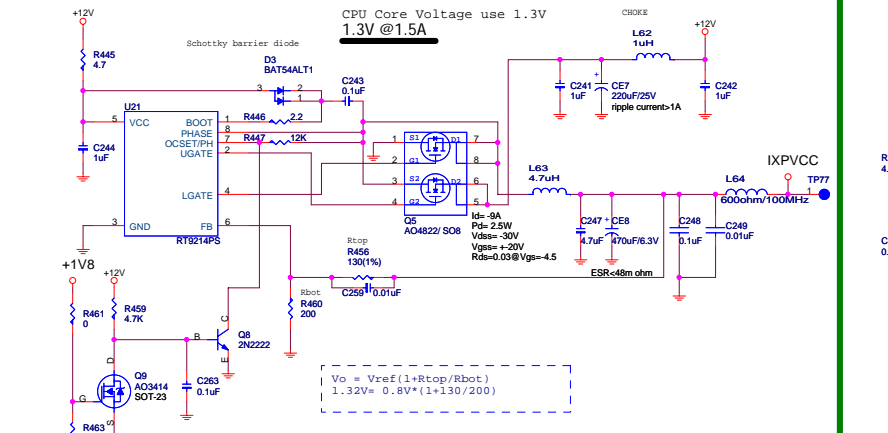
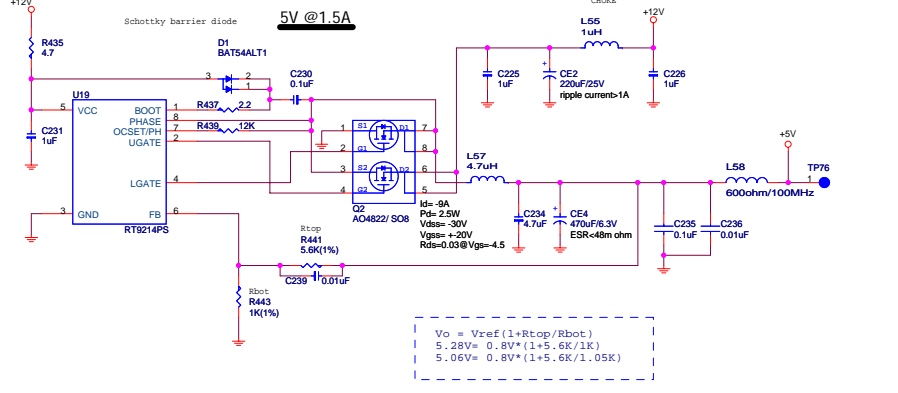
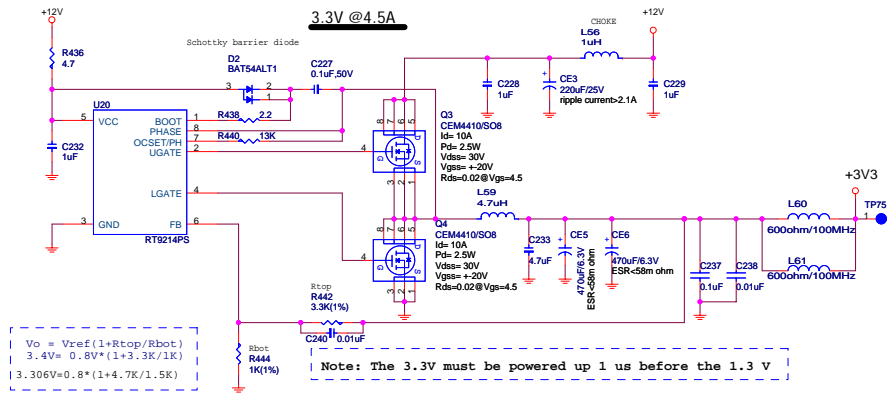
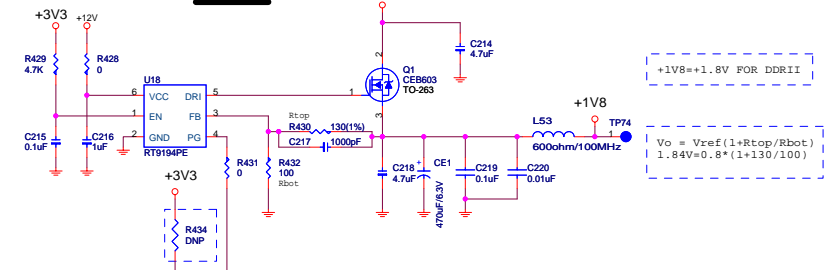
| | | |
|--|----------------|---------|
| Intel Corp | | |
| Title Intel(R) IXP435 Multi-Service Residential Gateway Reference Platform | | |
| Size C | Page Title FXO | Rev 1.1 |
| Date: Tuesday, April 24, 2007 | Sheet 15 | of 28 |

DC+12V/3.5A INPUT



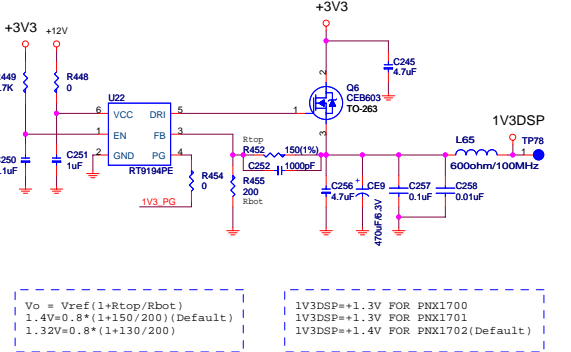
DDRII use 1.8V

1.8V @2A

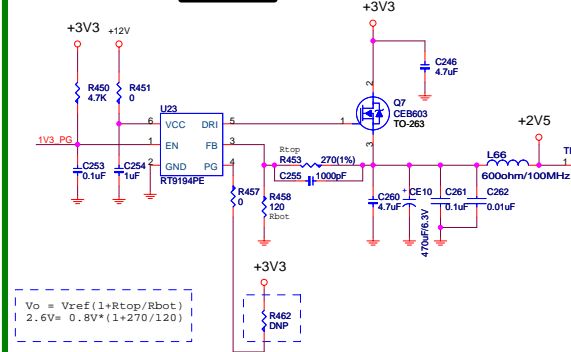


PNX170x use

1.3V @1.5A

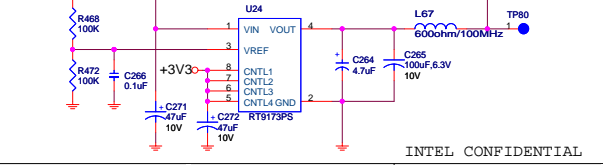


2.5V @1.5A



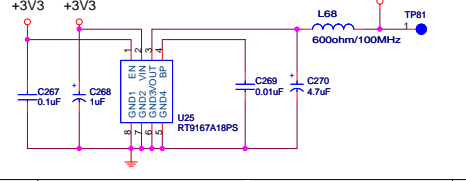
DDRII Termination use 0.9V

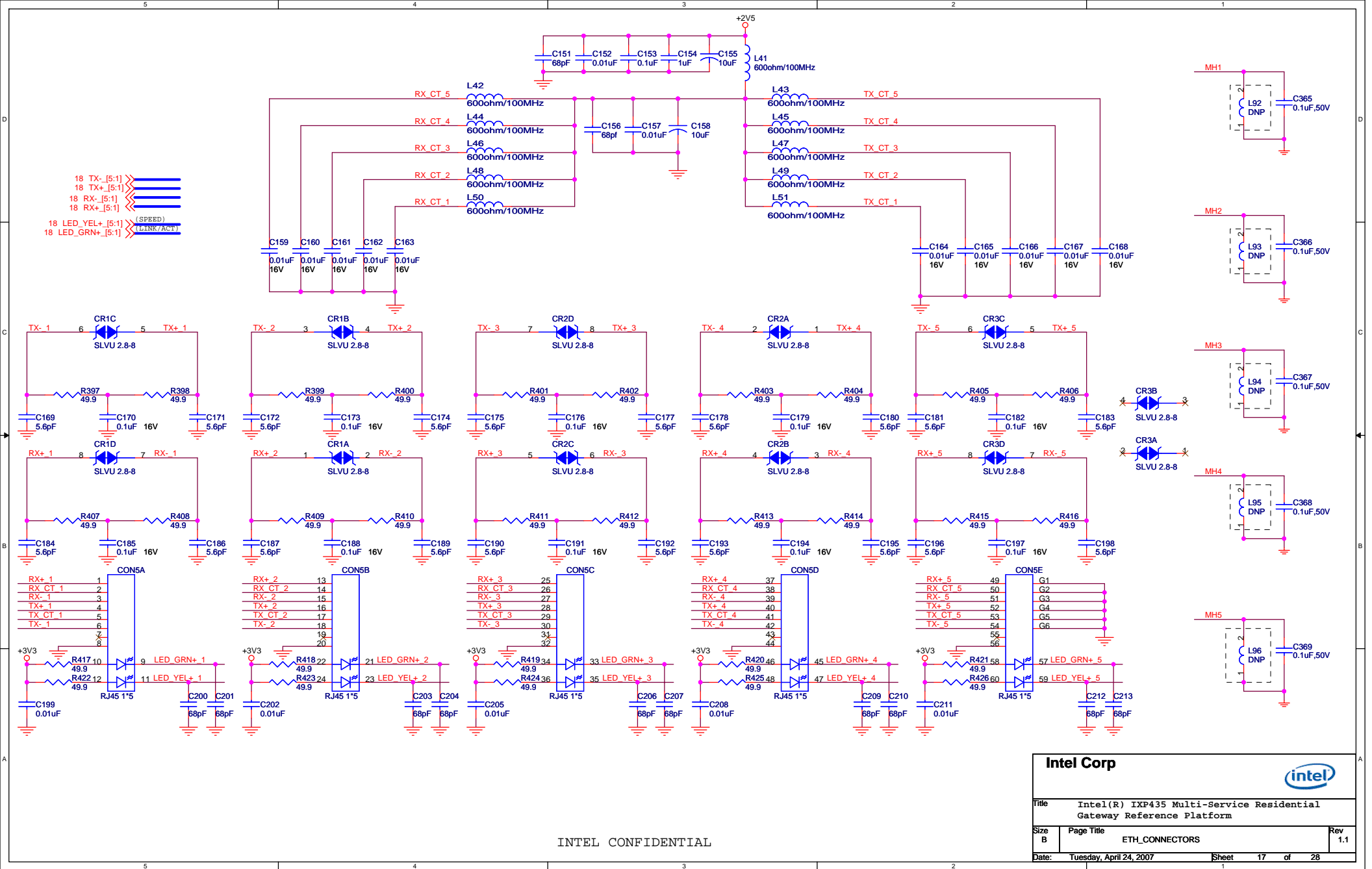
0.9V @1.5A



KENDIN use 1.8V

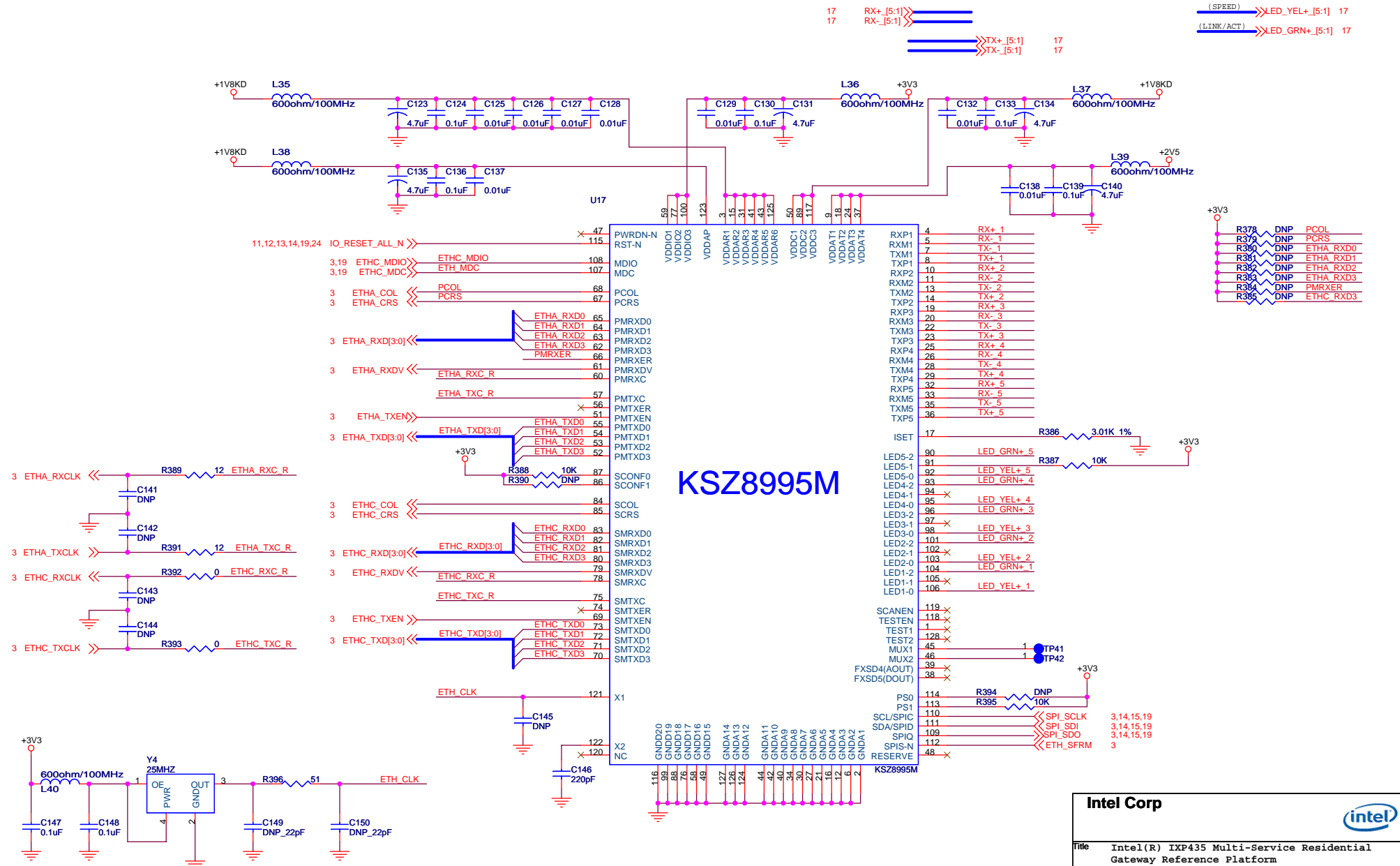
1.8V @500mA





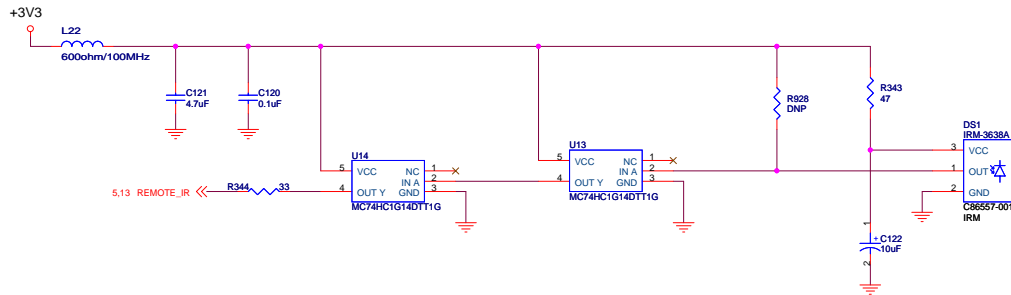
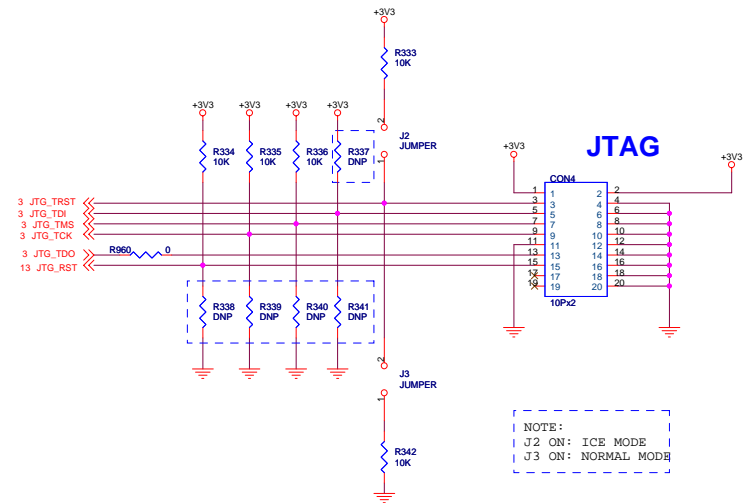
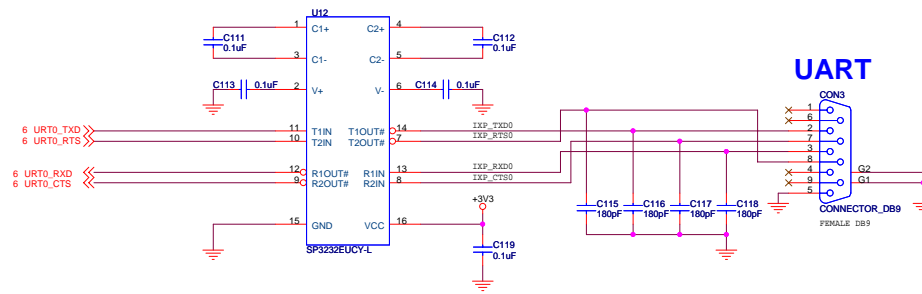
INTEL CONFIDENTIAL

| | | |
|--|---------------------------|---------|
| Intel Corp | | |
| Title Intel(R) IXP435 Multi-Service Residential Gateway Reference Platform | | |
| Size B | Page Title ETH_CONNECTORS | Rev 1.1 |
| Date: Tuesday, April 24, 2007 | Sheet 17 of 28 | |

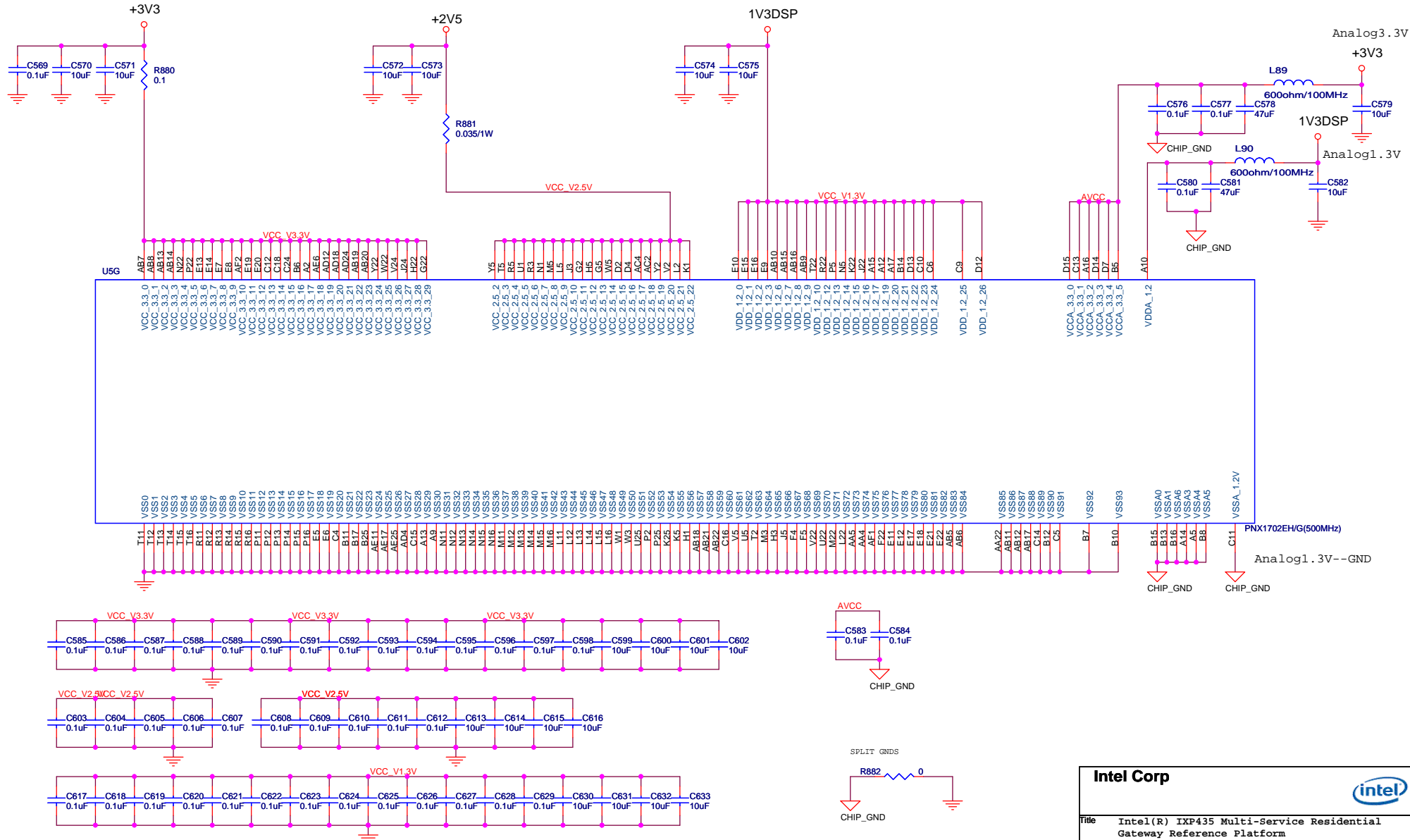


INTEL CONFIDENTIAL

| | | | |
|--|----------------|---------|--|
| Intel Corp | | | |
| Title Intel(R) IXP435 Multi-Service Residential Gateway Reference Platform | | | |
| Size B | Page Title LAN | Rev 1.1 | |
| Date: Tuesday, April 24, 2007 | Sheet 18 | of 28 | |

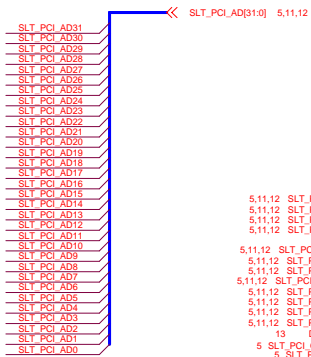
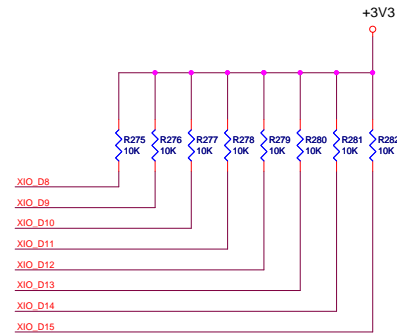
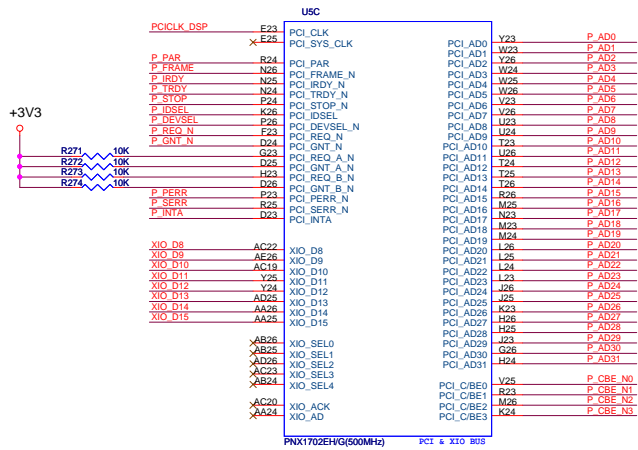


INTEL CONFIDENTIAL



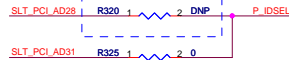
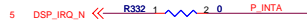
INTEL CONFIDENTIAL

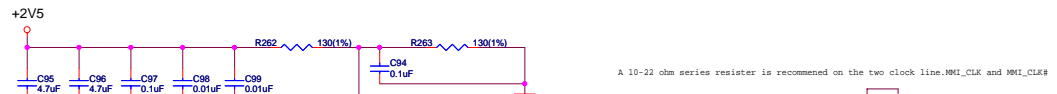
| | | |
|--|----------------------|---------|
| Intel Corp | | |
| Title Intel(R) IXP435 Multi-Service Residential Gateway Reference Platform | | |
| Size B | Page Title PNX POWER | Rev 1.1 |
| Date: Tuesday, April 24, 2007 | Sheet 21 | of 28 |



| | | | | | |
|--------------|------|---|---|---|--------|
| SLT PCI AD31 | R283 | 1 | 2 | 0 | P AD31 |
| SLT PCI AD30 | R294 | 0 | 2 | 0 | P AD30 |
| SLT PCI AD29 | R285 | 1 | 2 | 0 | P AD29 |
| SLT PCI AD28 | R286 | 1 | 2 | 0 | P AD28 |
| SLT PCI AD27 | R297 | 1 | 2 | 0 | P AD27 |
| SLT PCI AD26 | R288 | 1 | 2 | 0 | P AD26 |
| SLT PCI AD25 | R289 | 1 | 2 | 0 | P AD25 |
| SLT PCI AD24 | R290 | 1 | 2 | 0 | P AD24 |
| SLT PCI AD23 | R291 | 1 | 2 | 0 | P AD23 |
| SLT PCI AD22 | R292 | 1 | 2 | 0 | P AD22 |
| SLT PCI AD21 | R293 | 1 | 2 | 0 | P AD21 |
| SLT PCI AD20 | R294 | 1 | 2 | 0 | P AD20 |
| SLT PCI AD19 | R295 | 1 | 2 | 0 | P AD19 |
| SLT PCI AD18 | R296 | 1 | 2 | 0 | P AD18 |
| SLT PCI AD17 | R297 | 1 | 2 | 0 | P AD17 |
| SLT PCI AD16 | R298 | 1 | 2 | 0 | P AD16 |
| SLT PCI AD15 | R299 | 1 | 2 | 0 | P AD15 |
| SLT PCI AD14 | R300 | 1 | 2 | 0 | P AD14 |
| SLT PCI AD13 | R301 | 1 | 2 | 0 | P AD13 |
| SLT PCI AD12 | R302 | 1 | 2 | 0 | P AD12 |
| SLT PCI AD11 | R303 | 1 | 2 | 0 | P AD11 |
| SLT PCI AD10 | R304 | 1 | 2 | 0 | P AD10 |
| SLT PCI AD9 | R305 | 1 | 2 | 0 | P AD9 |
| SLT PCI AD8 | R306 | 1 | 2 | 0 | P AD8 |
| SLT PCI AD7 | R307 | 1 | 2 | 0 | P AD7 |
| SLT PCI AD6 | R308 | 1 | 2 | 0 | P AD6 |
| SLT PCI AD5 | R309 | 1 | 2 | 0 | P AD5 |
| SLT PCI AD4 | R310 | 1 | 2 | 0 | P AD4 |
| SLT PCI AD3 | R311 | 1 | 2 | 0 | P AD3 |
| SLT PCI AD2 | R312 | 1 | 2 | 0 | P AD2 |
| SLT PCI AD1 | R313 | 1 | 2 | 0 | P AD1 |
| SLT PCI AD0 | R314 | 1 | 2 | 0 | P AD0 |

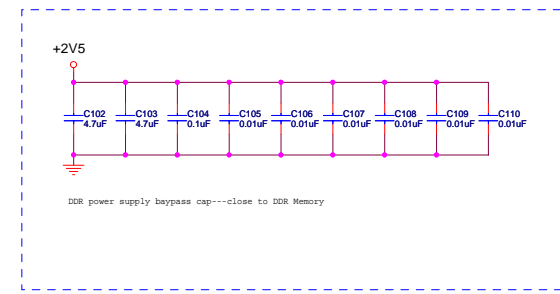
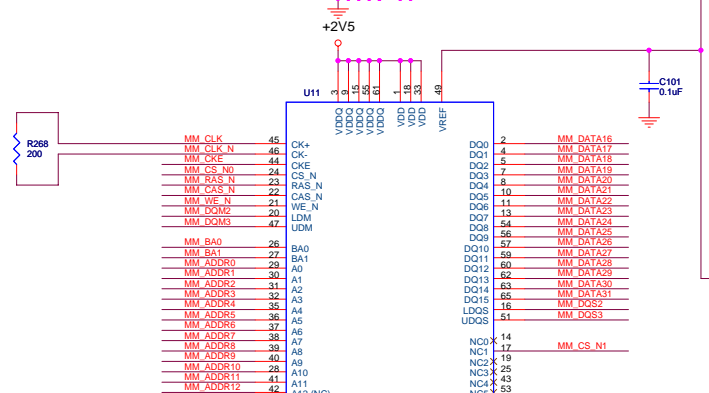
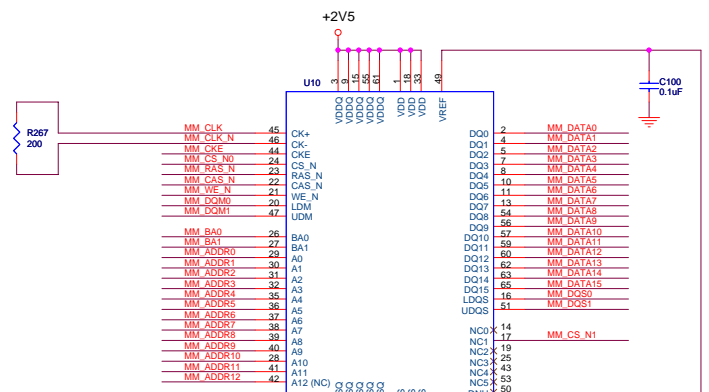
| | | | | | |
|------------------------|------|---|---|---|------------|
| 5,11,12 SLT_PCI_CBE0 | R315 | 1 | 2 | 0 | P_CBE_N0 |
| 5,11,12 SLT_PCI_CBE1 | R316 | 1 | 2 | 0 | P_CBE_N1 |
| 5,11,12 SLT_PCI_CBE2 | R317 | 1 | 2 | 0 | P_CBE_N2 |
| 5,11,12 SLT_PCI_CBE3 | R318 | 1 | 2 | 0 | P_CBE_N3 |
| 5,11,12 SLT_PCI_FRAME | R319 | 1 | 2 | 0 | P_FRAME |
| 5,11,12 SLT_PCI_IRDY | R321 | 1 | 2 | 0 | P_IRDY |
| 5,11,12 SLT_PCI_TRDY | R322 | 1 | 2 | 0 | P_TRDY |
| 5,11,12 SLT_PCI_DEVSEL | R323 | 1 | 2 | 0 | P_DEVSEL |
| 5,11,12 SLT_PCI_STOP | R324 | 1 | 2 | 0 | P_STOP |
| 5,11,12 SLT_PCI_PERR | R325 | 1 | 2 | 0 | P_PERR |
| 5,11,12 SLT_PCI_SERR | R327 | 1 | 2 | 0 | P_SERR |
| 5,11,12 SLT_PCI_PAR | R328 | 1 | 2 | 0 | P_PAR |
| 13 DSP_CLK | R329 | 1 | 2 | 0 | PCICLK_DSP |
| 5 SLT_PCI_GNT_0_N | R330 | 1 | 2 | 0 | P_GNT_N |
| 5 SLT_PCI_REQ0 | R331 | 1 | 2 | 0 | P_REQ_N |





| | | |
|-----------|-----|-----------|
| MM_DATA0 | C2 | MM_DATA0 |
| MM_DATA1 | C1 | MM_DATA1 |
| MM_DATA2 | E2 | MM_DATA2 |
| MM_DATA3 | D1 | MM_DATA3 |
| MM_DATA4 | E1 | MM_DATA4 |
| MM_DATA5 | E2 | MM_DATA5 |
| MM_DATA6 | F1 | MM_DATA6 |
| MM_DATA7 | H2 | MM_DATA7 |
| MM_DATA8 | H4 | MM_DATA8 |
| MM_DATA9 | G3 | MM_DATA9 |
| MM_DATA10 | G4 | MM_DATA10 |
| MM_DATA11 | E3 | MM_DATA11 |
| MM_DATA12 | E4 | MM_DATA12 |
| MM_DATA13 | D3 | MM_DATA13 |
| MM_DATA14 | D4 | MM_DATA14 |
| MM_DATA15 | C3 | MM_DATA15 |
| MM_DATA16 | A3 | MM_DATA16 |
| MM_DATA17 | AC3 | MM_DATA17 |
| MM_DATA18 | AS4 | MM_DATA18 |
| MM_DATA19 | AB3 | MM_DATA19 |
| MM_DATA20 | AA3 | MM_DATA20 |
| MM_DATA21 | Y4 | MM_DATA21 |
| MM_DATA22 | Y3 | MM_DATA22 |
| MM_DATA23 | W4 | MM_DATA23 |
| MM_DATA24 | W2 | MM_DATA24 |
| MM_DATA25 | AA1 | MM_DATA25 |
| MM_DATA26 | AA2 | MM_DATA26 |
| MM_DATA27 | AB1 | MM_DATA27 |
| MM_DATA28 | AC1 | MM_DATA28 |
| MM_DATA29 | AD1 | MM_DATA29 |
| MM_DATA30 | AD2 | MM_DATA30 |
| MM_DATA31 | AD2 | MM_DATA31 |
| MM_DQS0 | J1 | MM_DQS0 |
| MM_DQS1 | G1 | MM_DQS1 |
| MM_DQS2 | H1 | MM_DQS2 |
| MM_DQS3 | V1 | MM_DQS3 |

PX1702EHG(500MHz) DDR STREAM CONTROLLER



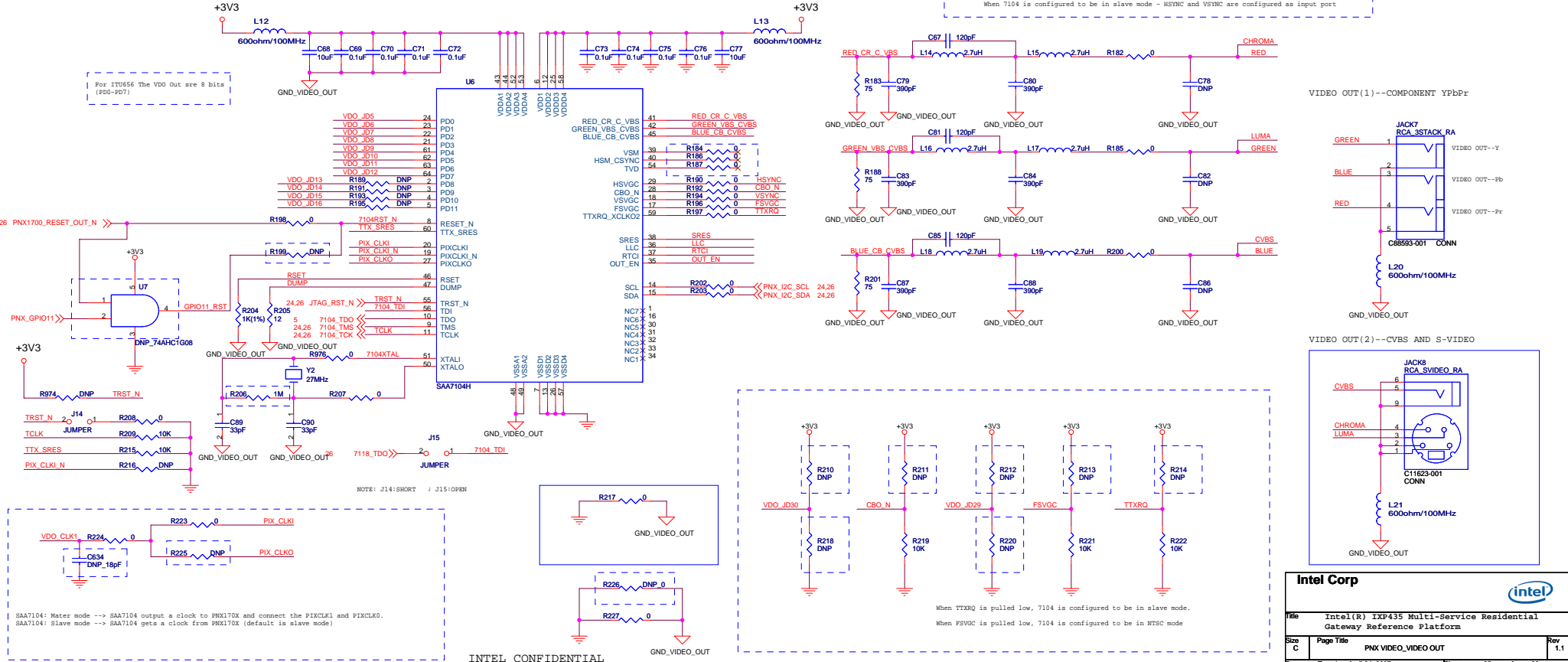
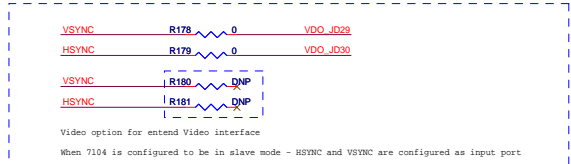
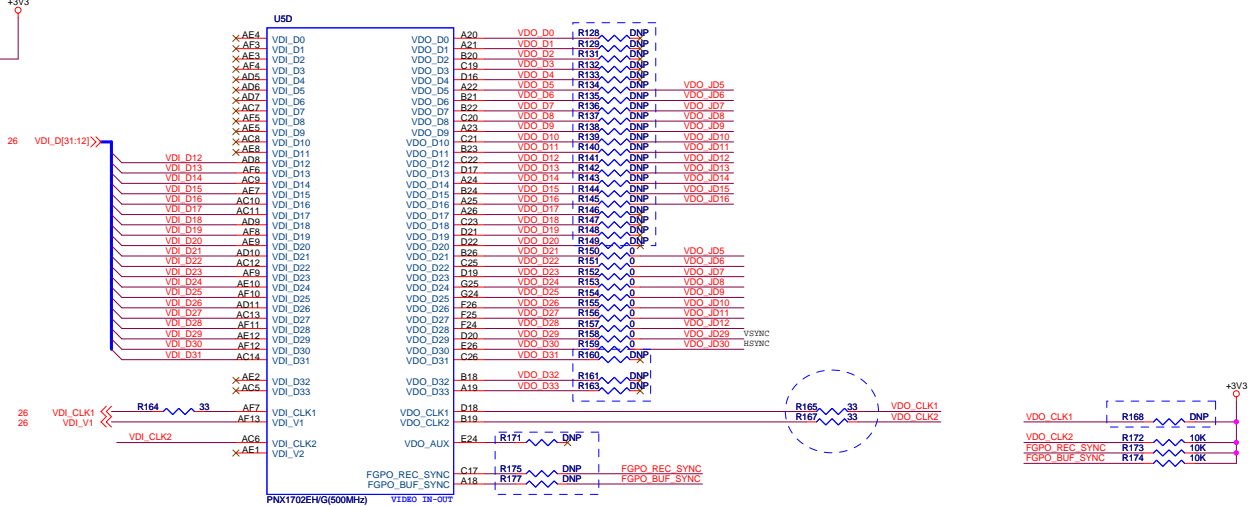
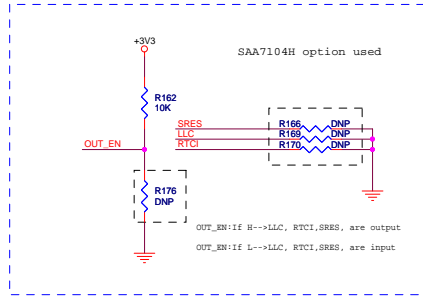
INTEL CONFIDENTIAL

Intel Corp

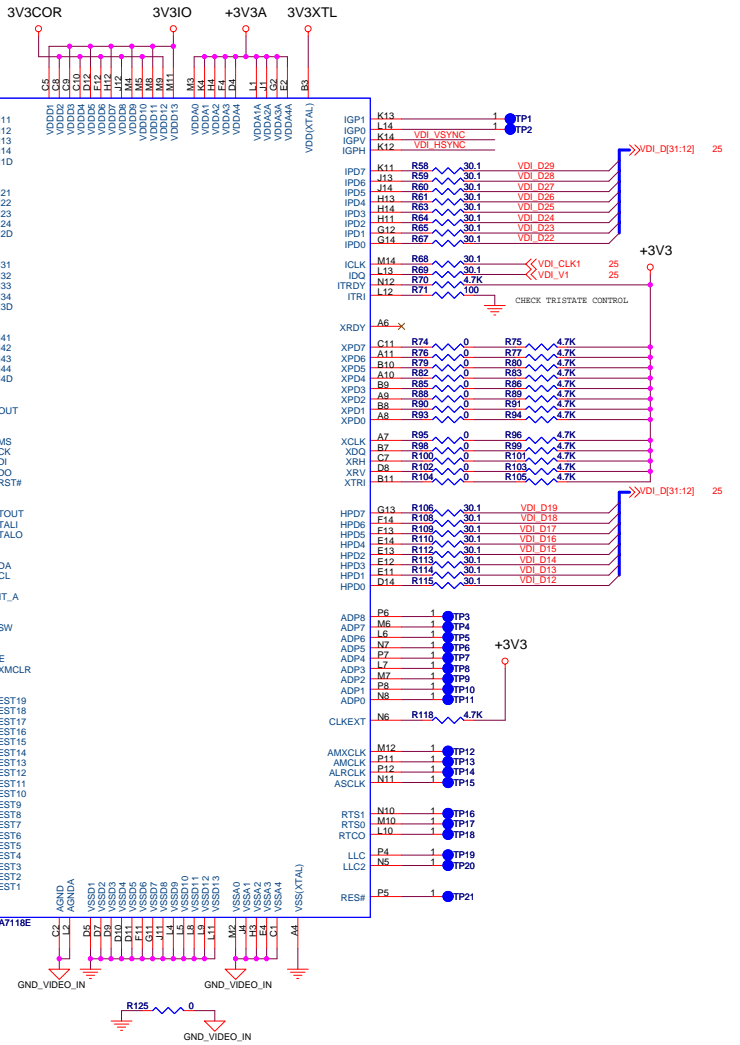
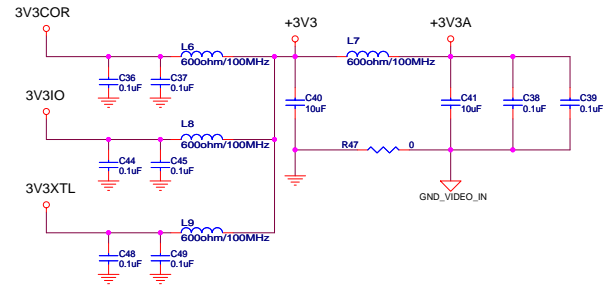
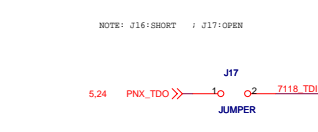
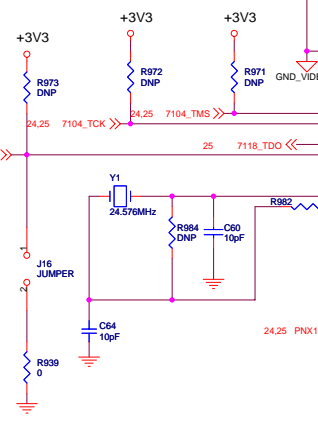
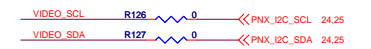
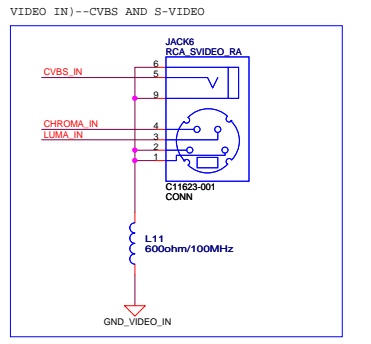
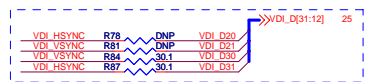
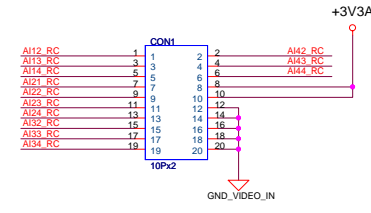
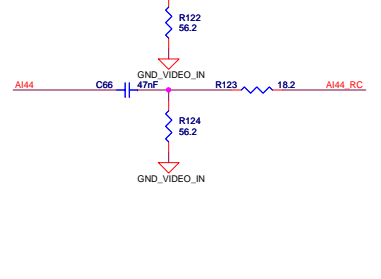
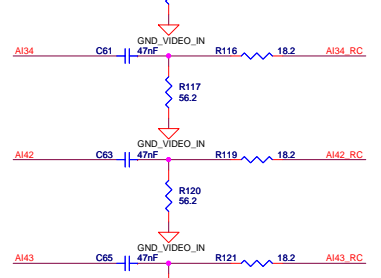
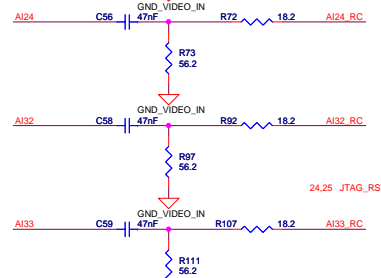
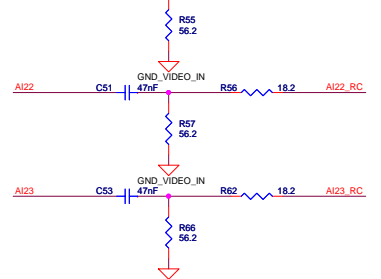
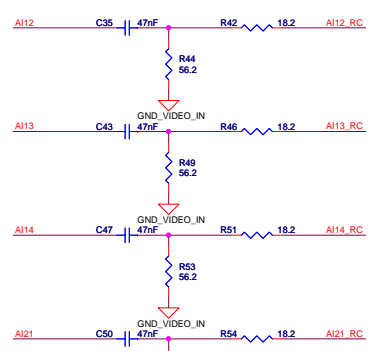
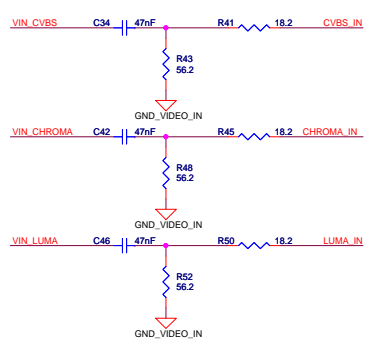
File Intel(R) IXP435 Multi-Service Residential Gateway Reference Platform

Size Page Title PNX DDR_MEM Rev 1.1

Date: Tuesday, April 24, 2007 Sheet 23 of 28



INTEL CONFIDENTIAL



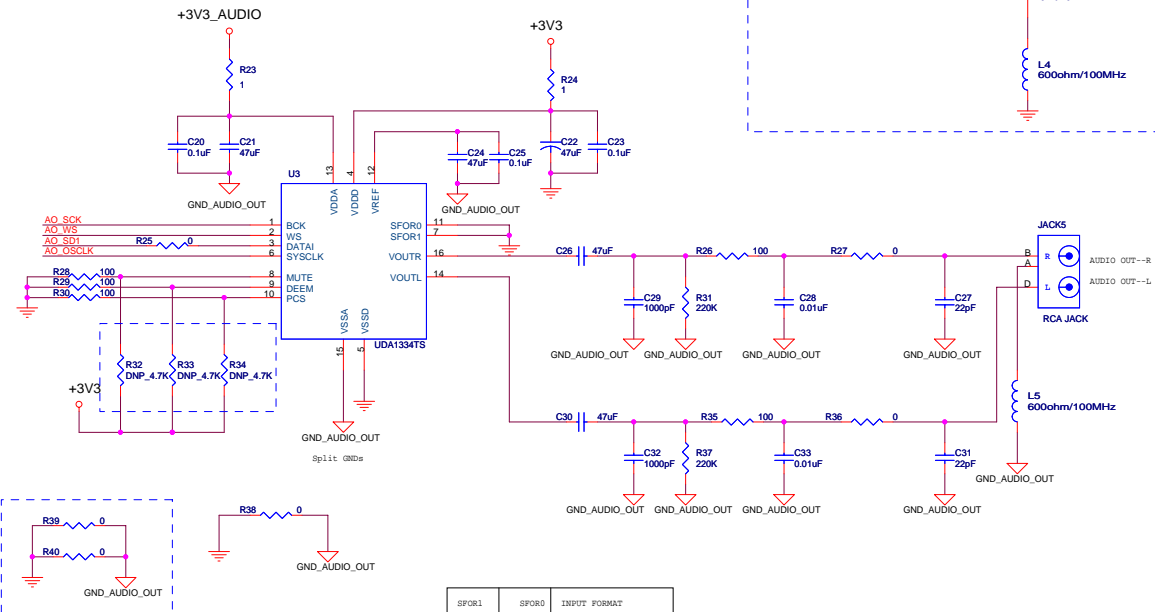
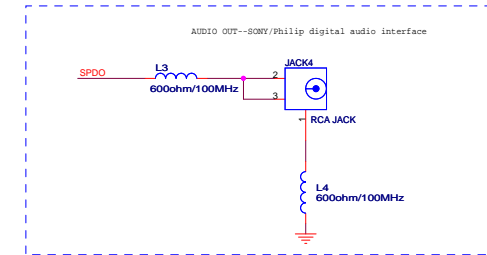
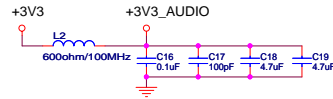
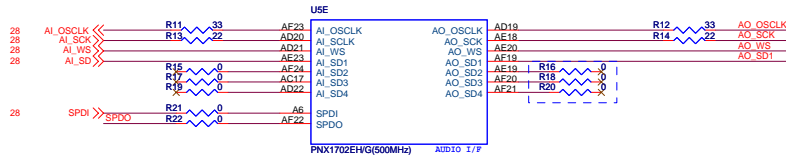
INTEL CONFIDENTIAL

Intel Corp

File: Intel(R) IXP435 Multi-Service Residential Gateway Reference Platform

Size C Page Title PNX_VIDEO_VIDEO_IN Rev 1.1

Date: Tuesday, April 24, 2007 Sheet 26 of 28



| SPOR1 | SPOR0 | INPUT FORMAT |
|-------|-------|------------------------|
| LOW | LOW | 1*2 S-BUS INPUT |
| LOW | HIGH | LSB-JUSTIFIED(16 BITS) |
| HIGH | LOW | LSB-JUSTIFIED(20 BITS) |
| HIGH | HIGH | LSB-JUSTIFIED(24 BITS) |

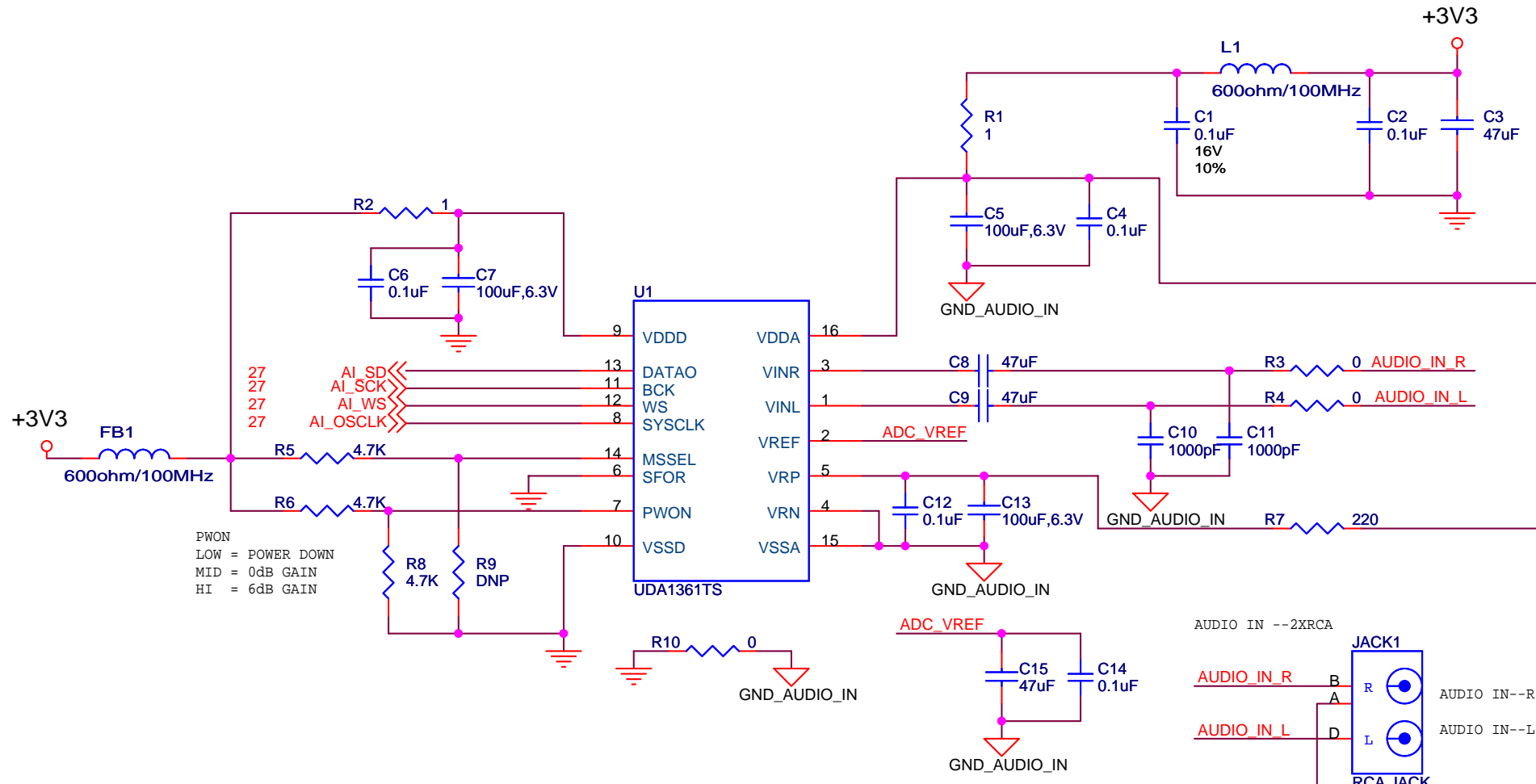
Intel Corp



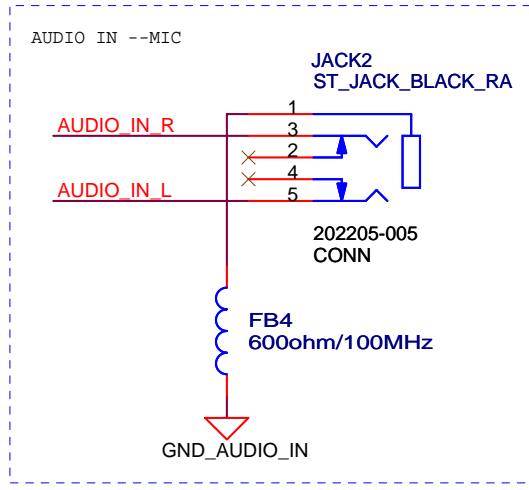
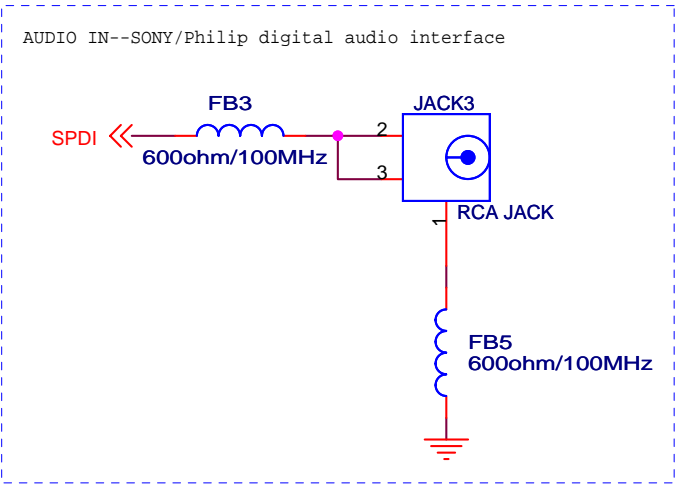
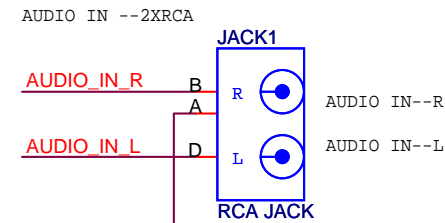
Title Intel(R) IXP435 Multi-Service Residential Gateway Reference Platform

Size C Page Title PNx AUDIO_AUDIO OUT Rev 1.1


Date: Tuesday, April 24, 2007 Sheet 27 of 28



PWON
 LOW = POWER DOWN
 MID = 0dB GAIN
 HI = 6dB GAIN



INTEL CONFIDENTIAL

| | | |
|---|-------------------------------|----------------|
| Intel Corp | | |
|  | | |
| Title Intel(R) IXP435 Multi-Service Residential Gateway Reference Platform | | |
| Size A | Page Title PNX AUDIO_AUDIO IN | Rev 1.1 |
| Date: Tuesday, April 24, 2007 | | Sheet 28 of 28 |