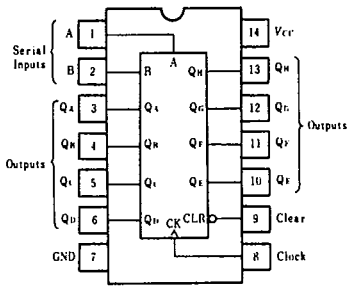
92D 10411 D T-46-09-05

HD74HC164 ● 8-bit Parallel-out Shift Register

This 8-bit shift register has gated serial inputs and clear. Each register bit is a D-type master/slave flip-flop. Inputs A & B permit complete control over the incoming data. A low at either or both inputs inhibits entry of new data and resets the first flip-flop to the low level at the next clock pulse. A high level on one input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-bit register during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the clear input.

■ PIN ARRANGEMENT

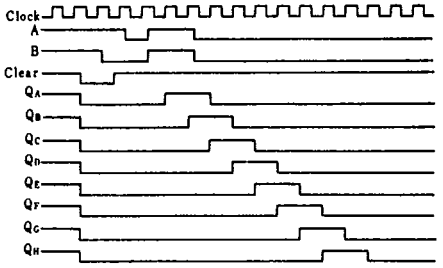


(Top View)

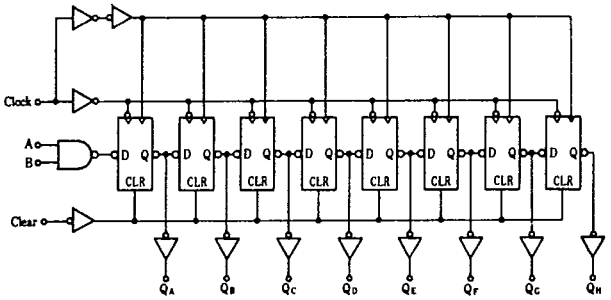
■ FEATURES

- High Speed Operation: t_{pd} (Clock to Q)=14.5ns typ. (C_L=50pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: Vcc=2~6V
- Low Input Current: 1μA max.
- Low Quiescent Supply Current: Icc (static)= 4μA max.

■ TIMING DIAGRAM



■ LOGIC DIAGRAM



■ FUNCTION TABLE

Inputs				Outputs		·····	
Clear	Clock	A	B	Q_A	Q_B	·····	Q_H
L	X	X	X	L	L	·····	L
H	↓	X	X	Q_{A_0}	Q_{B_0}	·····	Q_{H_0}
H	↑	L	X	L	Q_{A_n}	·····	Q_{G_n}
H	↑	X	L	L	Q_{A_n}	·····	Q_{G_n}
H	↑	H	H	H	Q_{A_n}	·····	Q_{G_n}

Q_{A_0} to Q_{H_0} = Outputs remain unchanged.
Q_{A_n} to Q_{G_n} = Data shifted from the previous stage on a positive edge at the clock input.

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■ DC CHARACTERISTICS

Item	Symbol	V_{CC}(V)	Test Conditions		Ta=25°C min	Ta=25°C typ	Ta=25°C max	Ta=−40~+85°C min	Ta=−40~+85°C max	Unit
Input Voltage	V_{IH}	2.0			1.5	—	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	
		6.0			4.2	—	—	4.2	—	
	V_{IL}	2.0			—	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	
Output Voltage	V_{OH}	2.0	$V_{in}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	1.9	2.0	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	
		4.5		$I_{OH}=-4mA$	4.18	—	—	4.13	—	
		6.0		$I_{OH}=-5.2mA$	5.68	—	—	5.63	—	
	V_{OL}	2.0	$V_{in}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	—	0.0	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	
		4.5		$I_{OL}=4mA$	—	—	0.26	—	0.33	
		6.0		$I_{OL}=5.2mA$	—	—	0.26	—	0.33	
Input Current	I_{in}	6.0	$V_{in}=V_{CC}$ or GND		—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	6.0	$V_{in}=V_{CC}$ or GND, $I_{out}=0\mu A$		—	—	4.0	—	40	μA

■ AC CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

Item	Symbol	V_{CC}(V)	Test Conditions	Ta=25°C min	Ta=25°C typ	Ta=25°C max	Ta=−40~+85°C min	Ta=−40~+85°C max	Unit
Maximum Clock Frequency	f_{max}	2.0		—	—	5	—	4	MHz
		4.5		—	—	25	—	20	
		6.0		—	—	29	—	24	
Propagation Delay Time	t_{PHL}	2.0	Clock to Q	—	—	160	—	200	ns
		4.5		—	14	32	—	40	
		6.0		—	—	27	—	34	
	t_{PLH}	2.0		—	—	160	—	200	ns
		4.5		—	15	32	—	40	
		6.0		—	—	27	—	34	
	t_{PHL}	2.0	Clear to Q	—	—	175	—	220	ns
		4.5		—	17	35	—	44	
		6.0		—	—	30	—	37	
Setup Time	t_{su}	2.0	A, B to Clock	100	—	—	125	—	ns
		4.5		20	1	—	25	—	
		6.0		17	—	—	21	—	
Hold Time	t_h	2.0	Clock to A, B	5	—	—	5	—	ns
		4.5		5	0	—	5	—	
		6.0		5	—	—	5	—	
Removal Time	t_{rem}	2.0	Clear to Clock	5	—	—	5	—	ns
		4.5		5	0	—	5	—	
		6.0		5	—	—	5	—	
Pulse Width	t_w	2.0	Clock	80	—	—	100	—	ns
		4.5		16	8	—	20	—	
		6.0		14	—	—	17	—	
		2.0	Clear	80	—	—	100	—	
		4.5		16	5	—	20	—	
		6.0		14	—	—	17	—	
Output Rise / Fall Time	t_{TLH} t_{THL}	2.0		—	—	75	—	95	ns
		4.5		—	5	15	—	19	
		6.0		—	—	13	—	16	
Input Capacitance	C_{in}	—		—	5	10	—	10	pF

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PACKAGE INFORMATION

T-90-20

In the HD74HC series of HS-CMOS logic, either of plastic DIP and small outline packages can be selected.
For your ordering, please refer to the following package code.

●Package code of HS-CMOS Logic

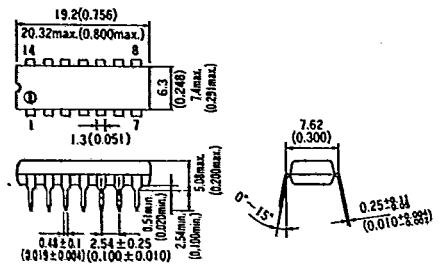
HD74HC XXXX P

- P : Package code (P : Plastic DIP, FP : Small outline package)
- XXXX : Individual device code
- HC : Series code of HS-CMOS logic
- HD74 : Initial code of Hitachi digital IC

■PLASTIC DIP PACKAGE [Unit: mm(inch), scale: 1/1]

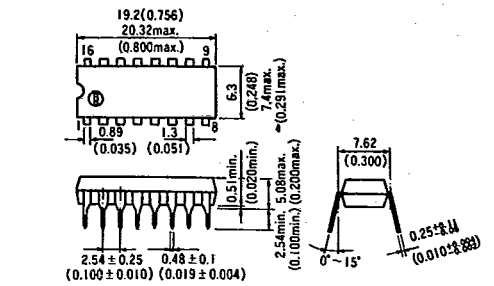
●14-pin type

DP-14



●16-pin type

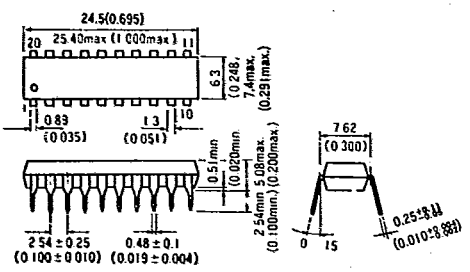
DP-16



Note) For the present, both packages of 0.89 and 1.3 can be used. Please refer to the Technical Marketing Dept. for further details.

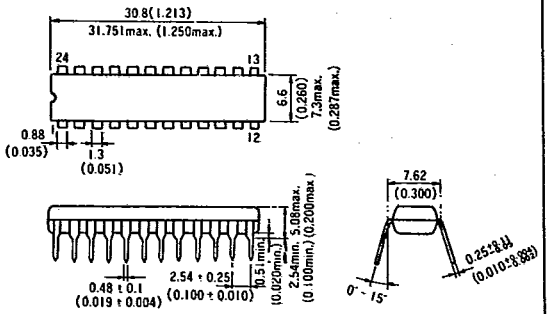
●20-pin type

DP-20N



●24-pin type

DP-24N



Note) Because this is under development, the dimentions may be changed partly.

0571 F-06

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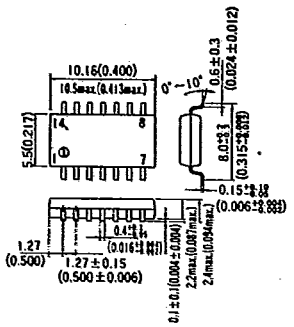
PACKAGE INFORMATION

■SMALL OUTLINE PACKAGE [Unit: mm(inch), scale: 1½]

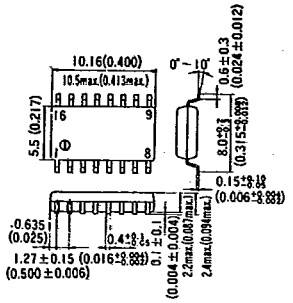
●14—pin type

FP—14D



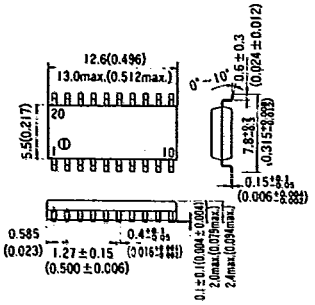
●16—pin type

FP—16D



●20—pin type

FP—20DN



Note) Preliminary

0572 F-07

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