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Digital Engineer to Signal Integrity Engineer In 28 Hours

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Abstract

This paper describes the development and delivery of a curriculum to cross train digital engineers in signal integrity (SI) design. Having digital engineers with extensive abilities in SI increases the integration of SI into the product development process, ensuring that SI is considered early on in the design process when selecting components, board stack-up, bus topologies, etc., potentially alleviating design problems before they become difficult to deal with. It also provides additional flexibility for project staffing. This paper goes into the details of a syllabus for the training class, textbook selection, and homework exercises. The class has been successfully implemented at Plexus across multiple design locations and would be appropriate for other digital design groups. A scaled back version could be used in a university setting.

Author(s) Biography

David Carney - Digital Design Engineer at Plexus Corp. Current responsibilities include board-level design, signal integrity design, design verification, and HDL logic design. Design experience includes PCI-X, Gigabit Ethernet, DDR SDRAM, HyperTransport, multi gigabit serial links, error correction coding, and SONET OC-192. Received BSCE from Milwaukee School of Engineering in 1997.

Josh Hinnendael - Digital Design Engineer at Plexus Corp. Current responsibilities include digital HDL logic design, board-level design, signal integrity design, design for test and design for manufacturing. Design experience includes PCI-Express and other multi-gigabit serial links, PCI-X, DDR SDRAM, system on a chip, and multi-million gate FPGA design and verification. Received BSCE from University of Wisconsin-Madison in 2001.

1 Introduction

Data rates in digital systems have been increasing at a quick pace. Digital systems architectures have evolved over the last few years from synchronous bus interconnections, to source synchronous interconnections, and most recently to clock embedded serial interconnections. With the increasing data rate and changes in interconnection architecture, design issues now include signal integrity issues such as timing analysis incorporating board and system level flight delays, crosstalk, simultaneous switching noise, jitter, and signal quality. The purpose of this paper is to present a training curriculum that teaches digital and analog hardware design engineers how to perform basic signal integrity analysis and simulations.

1.1 Signal Integrity Groups

An early answer to signal integrity design challenges was to establish dedicated signal integrity design groups within organizations to solve them. Plexus had a signal integrity group along these lines and the group worked on many small projects, usually with a design handed to them just before or early on in the PCB layout stage. This structure had some inherent problems. It was difficult to keep the group busy because of the transactional nature of the relationships with customers. It was difficult to efficiently allocate highly specialized signal integrity engineers to many different, short in duration tasks. Another problem with this type of signal integrity group was that it was difficult to integrate them into the product development process since the group was separate from the hardware design group and was not involved in the other aspects of the process. Performing signal integrity analysis only at the beginning of the PCB development phase of a project is not efficient with current high-speed digital designs and it must be considered at all stages of the design process from architecture definition through hardware verification. Also the signal integrity engineers were only involved in the verification process when a design was failing.

1.2 Plexus Signal Integrity Process

Plexus has a new signal integrity design approach to address the problems uncovered with the dedicated signal integrity group. The approach is for signal integrity design to be a core competency of the digital systems design group. A few members of the group are designated as experts, with that expertise rooted in the experience of the signal integrity group. These people are responsible for improving the signal integrity design processes, staying on top of new trends, tools, and methods in the industry, and distributing a basic level of signal integrity knowledge throughout the hardware design groups. In addition to these responsibilities, these engineers can also be allocated to digital design tasks or can be technical team leads on projects. The rest of the group has varying levels of signal integrity experience and training. This allows for most basic signal integrity analysis to be done by the actual digital engineers designing the hardware. It also ensures that the engineers who did some of the signal integrity analysis and simulations will be part of the hardware verification team and makes it much more likely that signal integrity measurements will be included in hardware test plans. Finally, this structure provides the ultimate amount of flexibility for staffing projects and prevents a small number of engineers from always being stuck doing simpler and less interesting signal integrity work.

It is becoming critical that any signal integrity design process include correlation between simulation and measurement to improve the quality of the simulations. Design trade offs are made based on the quality of the information available, and the better the quality of the simulations, the better the design decisions will be. Figure 1 shows a flow diagram of the Plexus signal integrity design process. Our primary signal integrity analysis is done before routing and then rules are driven into the PCB design through constraint management and routing guidelines documents. For the most part, post route analysis

is limited to simulating crosstalk. Finally hardware test plans are developed to correlate signal integrity simulations to reality. The process is a closed loop.

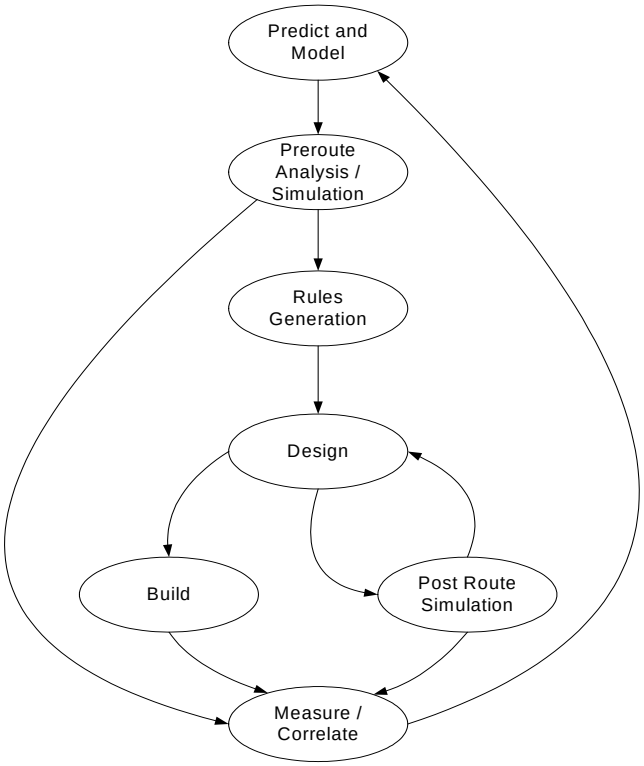


Figure 1 - Plexus Signal Integrity Design Flow

1.3 Signal Integrity Training Options

In order to achieve this new structure, Plexus had to arrange training for the members of the digital group in signal integrity analysis. There are plenty of external training options available such as short courses taught by industry experts, classes from EDA tool vendors, and university courses. Short courses usually lasting between 2 days and a week offered by many different industry experts can be a great source of signal integrity training. Engineers from Plexus have attended these and feedback is usually positive. However, these classes usually lack specific focus on signal integrity simulation tools. They focus much more on theory, rules of thumb analysis, and conceptual understanding. These are all important, but they do not help an engineer solve the complicated problems that exist and require simulation to solve. The EDA tool vendor classes usually focus on how to use their tools to solve problems and do not contain enough conceptual understanding. Both industry expert classes and EDA vendor classes usually pack a lot of information into a short period of time. Most people require some practice of concepts in order to learn them and the accelerated time frame does not allow it. University courses have the ability to solve all of these shortcomings. Plexus was not aware of any available in our area that met all of our needs and were taught based on our design flow. A problem with all of these training options is cost because sending an entire digital group to any of these would be quite expensive. The solution that has been developed is an internally taught course based on the Plexus tools and signal integrity processes, and the curriculum of that course is described in this paper. The course is designed to meet a total of 14 times for 2 hours each with a total of 2 to 4 hours of reading and assignments in between meetings.

1.4 Signal Integrity Training Introduction

The training course curriculum described in this paper is targeted toward both digital and analog engineers with a few years of experience designing hardware. The training consists of theory, tool usage, and signal integrity analysis methodologies that are used at Plexus. The primary tool used in this training is a preroute signal integrity tool such as Cadence SigXplorer, Mentor Hyperlynx, or SISoft SI Auditor combined with Synopsys HSPICE. Any of these tools would be appropriate to base a training course like this around. In addition to software tool usage, the course also includes some instruction on the use of signal integrity lab equipment such as high-speed oscilloscopes, TDRs, and VNAs. This paper will describe the selection of a textbook for this course and go through the syllabus in detail.

2 Textbook Selection

There are several well-written books that cover topics ranging from beginner electromagnetics to advanced modeling and simulation. When selecting a textbook for a signal integrity class it is important to keep in mind what is relevant and applicable to the engineers participating.

2.1 Criteria

Our signal integrity course targets hardware engineers with 3 or more years of experience that have a solid understanding of electronic principles and board-level design practices and have seen several signal integrity related phenomenon in their own designs. Having this real-world experience allows for a better understanding and greater appreciation for the topics covered in this course and helps immensely in the learning process. This provides the baseline for our book selection criteria.

2.1.1 Coverage of Electronic Principles

Basic principles such as setup and hold time, voltage thresholds, noise margin, capacitance, impedance, inductance, resistance, transmission line fundamentals, etc. are expected to be understood at a basic level by participants in the course. The book need not cover the fundamentals of these topics in great detail, but rather provide detail on how they affect signal integrity under specific conditions.

2.1.2 Coverage of Digital System-Level Issues

The participants are expected to be well aware of potential issues with board-level design. Decoupling, ground and VCC bounce, power distribution, bus protocols, etc. should be understood to some level. The main focus of this course is how to analyze these issues through simulation and calculation. The ideal book need only cover the basics of these phenomena, methodologies for analysis and simulation, and techniques to mitigate them.

2.1.3 Coverage of Interconnection

As it is generally the most controllable and flexible factor of a design, digital system engineers are often most concerned and have the greatest influence over interconnection. We define interconnection as the channel between the die on a driving device and the die on a receiving device. As an introductory signal integrity course, this is the area that we would like our book to focus on. Key subjects in our selection criteria include flight delay, timing analysis, stack-up design, reflection, crosstalk and coupling, skin effect, via and IBIS modeling, and simulation. Not only must these subjects be well covered, they must be written in a way that is easy to understand and flow well from one topic to the next.

2.1.4 Depth of Coverage

As a final selection criterion, our book must not cover topics in excruciating detail. Our signal integrity course is not a course on developing a simulation engine or writing simulation models, thus we do not need cover the theoretical detail and equations but need more of a conceptual understanding.

2.2 Books Considered

Several books were considered and evaluated to the criteria above. This section details each book considered.

2.2.1 Digital Signal Integrity: Modeling and Simulation with Interconnects and Packages by Brian Young

The first time this course was taught at Plexus, this was the book of choice. It is well written and provides good information on most of the topics covered. It covers driver and receiver modeling, interconnect modeling, digital timing analysis, simultaneous switching noise and crosstalk, signal integrity test equipment such as TDR and VNA, and frequency domain topics such as S-parameters. However, the book is too theory based for a beginner signal integrity course. Participants in the class found the book to be somewhat difficult to understand. While it meets all of the selection criteria, in practice the book was a little too advanced for this introductory course. We would recommend this book along with High-Speed Signal Propagation: Advanced black Magic by Howard Johnson and Martin Graham for use in an advanced signal integrity course.

2.2.2 Right the First Time: A Practical Handbook On High Speed PCB and System Design by Lee W. Ritchey and John Zasio

This book is fairly well written and covers most of the topics in our criteria, but not in enough detail. We would recommend this book for a new engineer not familiar with the basics of high-speed digital system design, but not to an experienced engineer. Engineers at the level this course is targeted to should already have an understanding of digital system design comparable to the level of detail in this book.

2.2.3 High-Speed Digital Design: A Handbook of Black Magic by Howard Johnson and Martin Graham

This is a classic signal integrity book. It is well written and covers signal integrity topics in great detail. It is an excellent book for experienced digital engineers and signal integrity engineers. The book was written in 1993 and is still a very useful reference, but is a little dated for coverage of current high-speed digital design issues such as differential signaling and serial digital multi-gigabit interconnection. This book also has little coverage of simulation and modeling which is a key part of this signal integrity course. While this is an excellent book that no signal integrity or digital engineer's library is complete without, it was not the best choice for this signal integrity course. Some material presented in the course actually did come from this book though.

2.2.4 High-Speed Signal Propagation: Advanced Black Magic by Howard Johnson and Martin Graham

This is the newest signal integrity book by Johnson and Graham, an extension of their other book. It is well written and covers signal integrity topics in great detail. It is an excellent book for experienced signal integrity engineers looking for all of the theory on a topic as well as plenty of practical information, but not a good starting point for beginners. The book is also very broad in its coverage of topics and it would be difficult to focus a beginning course around because the focus of a beginning course needs to be on fundamentals.

2.2.5 High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices by Stephen H. Hall, Garrett W. Hall and James A. McCall

This book covers most of the topics in our criteria, but does not explain them well. The book seems to jump around a lot and does not flow well. It could be a good reference manual or handbook if the user has a specific topic/equation in mind, but not a good book to learn from or teach a class from.

2.2.6 Electromagnetics Explained: A Handbook for Wireless / RF, EMC, and High-Speed Electronics by Ron Schmitt

This is a good book for understanding electromagnetic fields, RF and EMC phenomenon and is clearly geared towards RF engineers. All topics are relevant when discussing signal integrity, but this book is not all-inclusive and does not cover the specific digital signal integrity aspects of electromagnetics. We used the first chapter of this book when explaining electromagnetics, but it is not our primary book. The first chapter does a great job of refreshing the practicing engineer's memory about electromagnetics and also puts the topic in a much broader perspective than just the low to microwave frequency bands that digital engineering is concerned with.

2.2.7 Computer Circuits Electrical Design by Ron K. Poon

This book is intended for an engineer designing high-speed systems and has a focus on SPICE modeling. Explanations of topics are short and mathematical equations and theories make up the majority of the content. This book is a better reference manual than a learning tool.

2.2.8 High-Speed Circuit Board Signal Integrity by Stephen C. Thierauf

While covering a number of topics, this book provides only a high-level overview of each topic as it applies to printed circuit board design (PCB). It is best suited to engineers not yet familiar to PCB design, and does not provide enough detail to meet our needs.

2.2.9 Signal Integrity - Simplified by Eric Bogatin **Book of Choice**

Signal Integrity – Simplified is our book of choice. It is very well written and covers many of the topics in our criteria in sufficient detail. It focuses on interconnection and emphasizes intuitive understanding using detailed diagrams and practical tools. Mathematics and theory are secondary to establishing clear mental images of concepts, making this book an excellent tool for learning signal integrity. Eric Bogatin divides signal integrity into three primary categories, timing, noise and electromagnetic interference (EMI). He covers noise and EMI in great detail, but leaves timing to other books. The book also does not cover digital system level simulation issues such as driver and receiver modeling or S-parameters. For our purpose this is not a major issue as we have developed class notes covering these topics based mainly on Digital Signal Integrity: Modeling and Simulation with Interconnects by Brian Young and High-Speed Signal Propagation: Advanced Black Magic by Howard Johnson.

3 SI Training Syllabus

The syllabus for the signal integrity training course is shown in table 1. The sessions are described in more detail in the following sections.

Meeting #	Topic(s)	Assignments Given (Due the following meeting)	Reading Assignment Due
1	SI Intro	Assignment 1	Read Ch 1 of Signal Integrity – Simplified
2	General Electromagnetic Theory (1 of 2)	Assignment 2	Read sections 7 (7.1-7.6, 7.15, 7.18), 9 (9.1-9.2), 8 (8.1-8.6), 5 (5.1-5.4), and 6 (6.1-6.6) of Signal Integrity – Simplified
3	General Electromagnetic Theory (2 of 2)	Assignment 3	Read sections 4 (4.1-4.4), 6 (6.16), and 9 (9.3-9.11) of Signal Integrity – Simplified
4	PCB Technology	Assignment 4	Read sections 7 (7.9-7.14, 7.16-7.17, 7.19-7.20) and 5 (5.7-5.8) of Signal Integrity – Simplified
5	Digital System Design and Digital Signaling Standards Modeling	Assignment 5	Read sections 2 (2.1-2.13), 8 (8.8-8.13), and 11 (11.1) of Signal Integrity – Simplified
6	IBIS Modeling	Assignment 6	
7	Interconnect Modeling	Assignment 7	Read sections 2 (2.15-2.16), 3 (3.3-3.10), 8 (8.14-8.19), 9 (9.12-9.16) of Signal Integrity – Simplified
8	Timing Analysis	Assignment 8	
9	Crosstalk and SSN	Assignment 9	Read sections 5 (5.5), 6 (6.7-6.14), and 10 (10.1-10.19) of Signal Integrity – Simplified
10	Lab Measurements		Read section 2 (2.14), and 8 (8.7) of Signal Integrity – Simplified
11	Preroute Simulation		
12	Post Route Simulation		
13	Constraint Management		
14	Advanced Topics		Read section 11 (11.2-11.21) of Signal Integrity – Simplified

Table 1 – SI Training Syllabus

3.1 Week 1 – Introduction to Signal Integrity

The first signal integrity course session is meant to give an overview of signal integrity design at Plexus, our goals, the services we provide to our customers, and the method by which we provide them.

First, the goals and background information discussed in the first section of this paper is presented. Once we have established our goals, we then briefly discus the services that we provide, when and why each service is needed, tools to accomplish each task, and typical output generated from the analysis.

Plexus provides several signal integrity services such as high-speed board design review, stack-up design, timing analysis including board flight delays, IBIS model checking, signal quality analysis, crosstalk analysis, and PCB constraint generation; both through documentation and the use of electronic constraint databases such as Cadence Constraint Manager. Each task is equally important, but only one, a combination of a few, or all may be applicable for a particular project and each customer may have a desired delivery format in mind as well as a tool of choice. Time is spent going over a typical SI report and PCB guidelines document in detail to provide a good starting point for potential documentation deliverables.

Next, time is spent explaining some very basic information about digital signal integrity such as the knee frequency of digital signals and the electrical length of an interconnection and how that relates to the length of a rising edge of a digital signal. Finally, the session wraps up with an open group discussion

about the reading assigned before this session and a quick demo of how to invoke and run our preroute simulation tools, as an aid to the assignment for the following week.

3.1.1 Pre-reading

The reading for the first week is meant to provide a high-level overview of what signal integrity is, the various aspects of it that must be considered for high-speed design, and topics that will be discussed in detail in futures sessions. Concepts such as signal quality, crosstalk, rail collapse in the power and ground distribution system, and EMI are described in a pictorial sense, instilling a clear image of the problem in the engineers' minds without getting into the detail of the theory and mathematic equations. Finally, the chapter wraps up by describing the SI methodology for product design such as circuit analysis, modeling, and simulation that can be used to mitigate these problems.

3.1.2 Assignment 1

The assignment for the first week is intended to introduce the engineers to the simulation tools and to teach them how to perform a simple simulation to determine the appropriate termination achieve the best signal quality on a typical transmission line. Other than a quick overview of how to invoke the simulation tool, little information is given to the engineers in demo during the first session. The purpose is to have the engineers try to learn the tool with as little up front guidance as possible. From our experience this method ensures that questions are generated regarding tool settings and their meaning, and leads to a better understanding of how the tool works.

Determine the appropriate passive termination (series or parallel and resistor values) to minimize overshoot and undershoot for a 3.3V, 24mA, ALVC logic family buffer driving a 10 in. 50 Ohm transmission line. Discuss the effect of placement of the termination element on overshoot and undershoot. The receiver is also a 24mA ALVC logic family buffer. Use the following:

- Specctraquest SigXP for simulation
- Model repository for buffer model

Based on the rise time (or fall time, whichever is faster) that you measure for your terminated signal:

a) What is the fknee frequency of a digital signal using this buffer?
b) At what length of trace do you need to use distributed models instead of lumped?

3.2 Week 2 – General Electromagnetic Theory Part I

The next two sessions are the first fully technical ones and general background information about electromagnetic theory and transmission lines as they apply to signal integrity design is covered. The first topic is the basic RLGC lumped element circuit model of the transmission line followed by some additional discussion about the propagation of signals in transmission lines and the difference between uniform and non-uniform transmission lines. After basic transmission line background, the concept of the lossless LC mode of the transmission line is discussed. The basic equations relating characteristic impedance, propagation delay, dielectric constant, and capacitance and inductance per unit length are presented. The lumped element model for an LC transmission line is covered and rules of thumb for how many lumped element sections are required based on the edge rate or frequency content of a signal are given. The concept of the ideal distributed lossless transmission line is compared to the lumped element approximations.

Next, the concept of lossy transmission lines is covered. The RC mode of transmission line operation is covered just to show why it is not usually used in SI analysis since it is usually only applicable at low frequencies. The RLC model is discussed with a differentiation made between the DC resistance of a transmission line and the AC resistance due to skin effect. The RLGC model is also discussed where the

conductance of the dielectric medium becomes an important source of loss at higher frequencies. The frequency dependent nature of the loss such as dispersion and edge rate degradation are covered.

The next topic is that of reflections at impedance discontinuities. The bounce diagram is used to illustrate this concept using the reflection and transmission coefficients.

The last topics in this session are regarding inductance and capacitance. These ideal circuit elements are discussed with their basis in magnetic and electric fields. This is very important background information for understanding many signal integrity topics such as coupling and ground bounce. Especially inductance as it tends to be misunderstood by digital engineers and requires some focus.

Examples used throughout the session to illustrate the topics are given as follows.

- Lossless transmission line examples:
  - Characteristic impedance of a copper stripline is 60 Ohms, dielectric constant = 4.3. Determine the capacitance and inductance per inch of a trace.
  - You measure the delay of a 7 inch long stripline trace in FR4 to be 1.25 ns. What is the effective dielectric constant?
  - If the relative dielectric constant of a transmission line is 4.3 and the relative magnetic permeability is 100 and it is a 60 Ohm stripline – determine the capacitance and inductance per inch of a trace
- Lossy transmission line examples
  - For a 50 Ohm, 4.1 dielectric constant, 5 mil, 1/2 oz copper trace, answer the following:
    - Below what frequency would R be much larger than ωL?
    - Above what trace length would R be significant enough to affect the simulation results in the LC mode of operation?

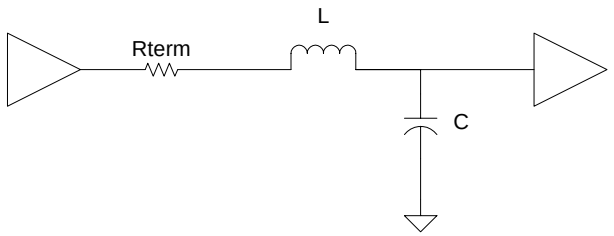
3.2.1 Pre-reading

The reading covers all of the topics discussed very effectively. Bogatin does a great job of explaining these topics in an easy to understand way that does not get bogged down in mathematics.

3.2.2 Assignment 2

The assignment has the engineer resimulate using the topology from assignment 1 but with cascaded lumped element models instead of the distributed transmission line model. This assignment helps develop an intuitive feel for how the lumped element circuit models approximate the ideal transmission line model.

Using the LC lumped model discussed, calculate L and C for the 10 inch transmission line from assignment 1. Resimulate the terminated driver/receiver circuit from assignment 1 driving a single lumped element circuit with the calculated L and C as shown in the following figure:



Compare the results of the simulation with those from assignment 1.

Divide the lumped element model into multiple sections (two 5 in. sections, three 3.3 in. sections, four 2.5 in. sections, etc.) and resimulate until you have good agreement between the distributed model used by Specctraquest and your cascaded lumped element model.

At what lumped element segment length do you get good agreement with the distributed transmission line simulation. Compare this segment length with the 1/6 length of a rising edge rule discussed in session 1.

3.3 Week 3 – General Electromagnetic Theory Part II

This session is a continuation of session 2. The first thing covered is the concept of resistance. The sources of resistance in transmission lines are presented including the DC resistance caused by the conductivity of a conductor and the AC resistance caused by the skin effect. The skin effect is described in terms of the path of least inductance and the concept of the decrease in inductance of a transmission line around the onset of the skin effect is presented. An approximation for the AC resistance from High-Speed Signal Propagation – Advanced Black Magic by Howard Johnson is presented and used in some examples.

Next, loss mechanisms in transmission lines are covered in more detail focusing on skin effect and dielectric loss. Some approximations for skin effect loss and dielectric loss from High-Speed Signal Propagation – Advanced Black Magic by Howard Johnson are used to illustrate at what frequencies skin effect and dielectric loss are dominant for PCB trace structures.

The final topic discussed is that of parameter scaling. The basic concept here is that as all three physical dimensions of a structure are scaled, the parasitic inductance and capacitance will scale proportionally and the frequency response will scale inverse proportionally. This concept is very important for getting a basic understanding of how transmission lines relate to physical structures and is covered very well in High-Speed Signal Propagation – Advanced Black Magic by Howard Johnson.

Examples used in this session to illustrate the points are listed as follows.

- Skin effect examples
    - At what frequency does the skin effect start to take effect for a 1/2 ounce copper stripline trace using the skin depth approximation?
    - For a 5 mil wide 1/2 ounce copper trace
        - At what frequency does the High-Speed Signal Propagation – Advanced Black Magic equation predict the onset of the skin effect region?
        - What is the AC resistance of a 10 in. long trace at 500 MHz?
        - How does this compare with what a 2D field solver predicts?
- Loss examples
    - For a 50 Ohm, 5 mil, 1/2 ounce copper trace, with dielectric constant 4, and loss tangent 0.025
        - At what frequency does dielectric loss begin to exceed skin effect loss?
        - What is the dielectric and skin effect loss of a 20 in. long trace in dB at 100 MHz and 1 GHz?

3.3.1 Pre-reading

This reading covers the concepts of resistance and loss but does not cover parametric scaling. No reading was given to cover this topic and it was included in the class notes.

3.3.2 Assignment 3

The purpose of this assignment is to see the difference between a lossless simulation and a lossy simulation. The assignment uses the same topology as used in assignment 1.

Using the results from assignment 1 as a starting point, run the simulations with and without lossy simulation turned on and compare the results. Change the model for the interconnection from a simple transmission line to a single stripline with the following parameters:

- er = 4.3
- dielectric loss tangent = 0.025
- Height to ground plane above = 5.1 mils
- Height to ground plane below = 10 mils
- Trace width = 4 mils
- Trace thickness = 0.6 mils
- Length = 50 in.

3.4 Week 4 – Printed Circuit Board Technology

Printed Circuit Board (PCB) technology selection is becoming more and more important in digital system design as signaling speeds increase requiring tighter impedance control, more buried capacitance, and less lossy materials. The goal of the week 4 session is to gain a general understanding of PCB structures in digital signal transmission, gain an intuitive feel for how various parameters of a PCB affect characteristic impedance, learn how to use a 2D field solver to calculate characteristic impedance, gain an understanding of special PCB dielectric materials and constructions, and learn some basic PCB stack-up design considerations.

The discussion of PCB technology begins with the types of PCB structures and the tradeoffs of each. Microstrips on the top and bottom layers of PCBs, and striplines on the internal layers are covered in detail. Other structures such as coplanar waveguide microstrips, edge coupled differential striplines, and broadside coupled differential striplines are described as well. Once the basic structures are understood, our discussion focuses on impedance and the parameters that define the impedance of single-ended and differential structures. The main parameters that determine the impedance of a single-ended trace are trace width, trace thickness, distance to the nearest plane from both the top and bottom of the trace, and dielectric constant. Differential structures include all of the above parameters as well as the spacing between the traces.

The primary benefit of a controlled impedance board is that it allows for a consistent impedance connection between devices, therefore minimizing impedance mismatches and thus reflections. Board houses will guarantee the impedance of PCB traces to be within a given tolerance, and will test the boards to this tolerance before shipping them to their customers. The primary focus is knowing when to use controlled impedance and how to work with a board house to come up with a stackup that is physically realizable and meets the needs of the design.

As tool for understanding impedance, a brief demonstration is performed where both a single-ended and differential structure is placed into a 2D field solver and the parameters are changed to show how they affect the impedance of the structure. Now that impedance is well understood, the last topic for discussion is stack-up considerations including special materials.

In complex digital system design, stack-up design can be a difficult task. The applicable manufacturability rules such as balanced stack-up and aspect ratio are presented. The effects of system limitations such as size and thickness are discussed. Basic rules of thumb for layer stacking (power, ground, and signal), plane splits, buried capacitance, and advanced topics like blind and buried vias, micro vias, and special materials like Rogers and Nelco are described in detail. All of these factors must be well understood and taken under consideration when designing an effective stack-up.

3.4.1 Pre-reading

The reading does not focus too much on actual PCB design and stackup selection. It does contain some information on 2D field solvers and dielectric constants. It focuses on characteristic impedance and signal and return paths in PCBs. It also covers some of the frequency dependent properties of characteristic impedance. The class notes that contain information about PCB construction and stackup augment the reading material.

3.4.2 Assignment 4

Design a 6 layer stack-up including 2 planes, 2 signal layers, and top and bottom component layers. 50 Ohm single ended impedance is required.

3.5 Week 5 – Digital System Design, Signal Standards and Modeling

The purpose of this session is to cover the driver and receiver modeling aspects of signal integrity design as well as some general characteristics of high-speed digital systems. The session begins with discussion about digital system bus architecture and describes the synchronous, source synchronous, and embedded clock serial bus structures. The applicability of signal integrity design to each bus structure is discussed. Next the frequency content of a digital signal is considered in the context of data rate and edge rate.

After these background concepts are presented the focus is placed on single-ended driver modeling of a CMOS push pull driver including the input to output voltage transfer characteristic, the current and voltage characteristics, and the source impedance. The discussion is extended to the current steering architecture for differential driver signaling.

The next topic is the analog nature of the digital waveform including rise time, overshoot, ring back, monotonicity, and plateaus. Basic buffer parameters such as Vih, Vil, Voh, and Vol are used to explain the concept of noise margin for digital signaling.

Examples of single ended and differential signaling are explored such as CMOS, LVTTL, LVDS, LVPECL, and SSTL2 to show the differences in basic parameters and characteristics. A topic that has been particularly important in past design work is the conversion between different differential signaling standards such as LVDS and LVPECL. Time is spent describing passive circuit network topologies to convert between signaling standards.

The modeling of drivers and receivers is described and the differences between behavioral IBIS models and transistor level SPICE models are explained.

The final topic is that of digital signal propagation and termination. The basic structures are unterminated, source terminated, end terminated, and source and end terminated. These structures are compared through a demonstration that shows the ringing, ledges, and voltage magnitude reached for receivers at various locations along a transmission line. The different types of termination are explained

such as source, end, diode, and AC. Also explained is how to choose between termination types and how to choose component values. Some detail is spent explaining the pitfalls of AC termination and requirements for choosing capacitor and resistor values. The termination concepts are also extended to differential signaling.

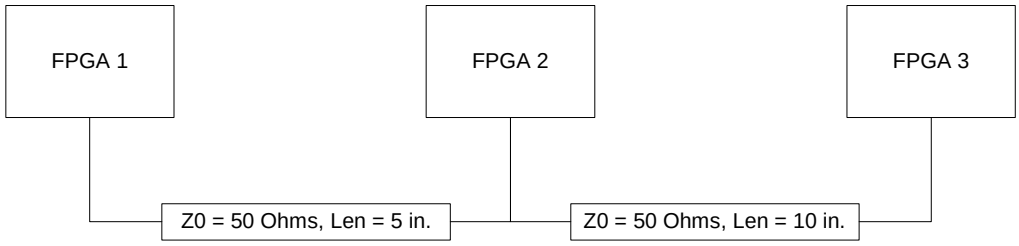
3.5.1 Pre-reading

The Signal Integrity Simplified book does not contain much material regarding the modeling of digital drivers and receivers. The reading assignment covers the frequency content of digital signals including the concepts of bandwidth and FFT. It also contains information about termination strategies and reflections from different transmission line structures. Finally, the reading has a brief introduction to differential signaling.

3.5.2 Assignment 5

This assignment focuses on topology exploration in signal integrity design and the advantages and disadvantages of the different termination types in a multi drop bus.

Using the following topology:



Make the following assumptions

- For the FPGA buffer models use a 16mA LVTTL buffer model for the Xilinx Virtex II Pro device
- Feel free to experiment with other drive strength buffers

Perform the following simulation cases

- Unterminated
- Single series termination resistor at one end
- Series termination resistor at the output of each FPGA buffer
- Thevenin end termination at one end (R=2*Z0 to Vcc and R=2*Z0 to Gnd)
- End terminations at both ends, same resistor values as previous

Record the overshoot, ringback, and monotonicity characteristics for each of the above simulation cases with each of the 3 FPGAs driving and each of the other two FPGA receivers.

3.6 Week 6 – IBIS Modeling

Week 6 focuses on the primary digital buffer and receiver modeling type prevalent in signal integrity simulation, the IBIS model. The structure of the IBIS model is stepped through in detail including the device model level and the buffer model level. Package models are described and some example IBIS models are shown. The IV curves and how they relate to the transistor and clamping diode structures inside digital buffers are explained in detail. The Vt curves and the loading conditions under which they are generated for the rising and falling waveforms are also described. The sources of IBIS models are

briefly discussed, either from SPICE simulations or from measurements of real devices and the characteristics to expect from each.

After describing the IBIS format, the process of cleaning IBIS models is presented. Cleaning is a process of fixing syntax errors, adding missing or incorrect datasheet parameters to the model, and evaluating the reasonableness of the models. A clear distinction is made between this process and that of model verification, which would require test equipment to measure the buffer characteristics. Model cleaning simply gives confidence in the quality of the models and a critical perspective from which to view the simulation results.

3.6.1 Pre-reading

Signal Integrity Simplified does not contain any more than passing mention of IBIS models. There is no reading assignment and all material is based on the IBIS specification and class notes.

3.6.2 Assignment 6

This assignment gives the participants a chance to evaluate and clean an actual IBIS model.

Choose an IBIS model from a manufacturers web site. Clean the IBIS model. Answer the following questions.

1) What things were missing from the IBIS model?
2) What changes did you have to make to the IBIS model?
3) What things in the IBIS model did not seem to be correct and what impact do you think these will have on your simulation results?

3.7 Week 7 – Interconnect Modeling

The purpose of this session is to expand on the transmission line discussions from week 2 and 3 to include some details about how transmission lines are actually modeled and simulated. The first task is to define what the transmission channel is. The transmission channel consists of package connections, PCB traces, vias, connectors, cables and everything else in between the die of the digital transmitter and the die of the digital receiver. A description is given for the different types of 2D and 3D field solvers and what types of transmission channel elements each one is appropriate for modeling. The different types of models are covered such as lumped element, ideal distributed transmission line, parametric lossy transmission line models such as the HSPICE W-element model, frequency domain S-parameter models, and behavioral time domain models. The majority of the focus is on the parametric lossy transmission line model since that is what many SI simulators use for mid-range data rate simulations such as below 1 Gbps. For simulations above 1 Gbps the S-parameter and behavioral time domain models are often required, especially for complex transmission channel elements such as connectors. Time is spent focusing on the frequency range of validity for each type of model.

After a general introduction to the different types of models is given, time is spent describing how these models apply to PCB traces, device package connections, connectors, vias, and cables. The final topic of discussion is that of creating models through making measurements with a VNA or TDR. This measurement process is only covered in concept at this point.

3.7.1 Pre-reading

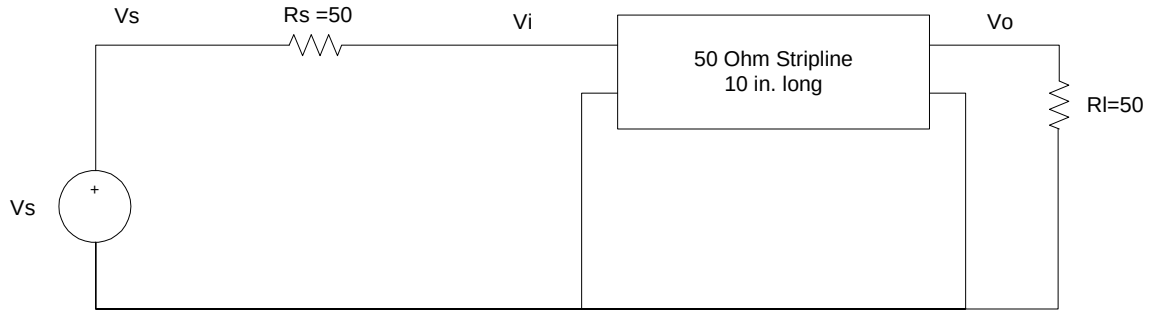
The reading first covers the concept of the bandwidth of a model in chapter 2. In chapter 3 the reading concentrates on the ideal circuit elements and the use of simulation tools such as SPICE. The chapter 8 reading contains some information about the types of impedance discontinuities that different elements

cause and their effects. Finally the reading in chapter 9 focuses on the modeling and effects of lossy transmission channel elements.

3.7.2 Assignment 7

The purpose is to give hands on experience with the effects of discontinuities on the channel bandwidth.

Plot the channel bandwidth of the channel shown in the following figure.



To plot this, create the function of Vo/Vi in dB versus frequency. For the stripline use a w-element model for a stripline trace with the following geometry:

- width = 4.3 mils
- dielectric constant = 4
- loss tangent = 0.025
- impedance = 50 Ohms (adjust dielectric thickness to achieve this)
    1) What is the half power bandwidth (-3dB) of this transmission channel?
    2) What is the bounded power spectra density bandwidth (-35 dB) of this transmission channel?

Rerun the simulation but break the trace up with a via located in the middle of the trace. Use the following SPICE subcircuit for the via model.

```
* Cadence Specctraquest 15.1 extracted this model
* Board thickness = 62 mils
* Via pad size = 20 mils
* Via antipad size = 29 mils
*
.subckt VIA_062_20milpad_29milantipad_simple 1 2

CL1A0W80 1 0 5e-014
CL5An1W45 2 0 5e-014
RLL1A0W80_L5An1W45 1 3 1e-7
l_RLL1A0W80_L5An1W45a 2 3 3.83916e-010


.ends VIA_062_20milpad_29milantipad_simple
```

3) How did the via affect the shape of the bandwidth plot?

3.8 Week 8 – Timing Analysis

The week 8 session focuses on timing analysis; what it is, how timing affects digital systems, the various components of timing that can lead to violations, and how an analysis can be performed to minimize potential timing problems.

In nearly every digital system design, components communicate with one another via protocols that are either synchronous with respect to a clock or asynchronous to a clock but with a specific timing relation between other signals within the protocol. Timing analysis is the process of analyzing the path delays of the system to ensure that all of the required timing relationships between signals are met. This session focuses primarily on synchronous logic or flip flops, which have specific timing relationships for their inputs that must be met to ensure communication stability.

Timing errors in synchronous circuits occur when the setup and hold time requirements of a device are not met. An analysis of a flip flop is performed detailing scenarios where voltage thresholds are not met within the specified timing parameters of a device, and what the result can be on the output buffer within the device. Conditions such as metastability or an unexpected bit transition can occur, which can propagate through the entire system. To perform an effective timing analysis, it is important to understand all the elements that can adversely affect a timing path.

In high-speed system design it is no longer sufficient to calculate setup and hold time margins between devices simply using the setup, hold, and clock-to-out parameters of each device in conjunction with the clock frequency. Several other factors such as flight delay, buffer delay, combinational logic delay, signal skew, jitter, and the conditions under which they are measured can have a major impact on timing margins. Each of the above elements is described in detail with particular emphasis on flight delay. Flight delay is defined as the amount of time that must be added to the clock to out delay specified in a datasheet to account for the differences in loading between the actual transmission channel and the test load used by the manufacturer to specify the clock to out delay. The flight delay is a measure of the delay incurred through the transmission channel interconnection in a digital system. A clear distinction is made for the purposes of timing analysis between flight delays and propagation delays where propagation delays are the amount of time it takes for an electromagnetic signal to propagate through a medium and are simply a function of the speed of light, the dielectric constant, and the length. This can be a particularly difficult concept to understand since flight delays can be negative if the transmission channel loading is effectively less than the test load, and the only accurate and efficient means to determine flight delays is through simulation.

Finally, once all of the conditions that can affect timing margins are understood, a detailed example is shown. A timing analysis is performed between and processor and memory on a multi-drop bus with several other devices on it and several loading topologies for data, address and control signals. Flight delays are calculated through simulation and the data is collected in both Forte Design Systems' Timing Designer and a spreadsheet that perform the calculations automatically.

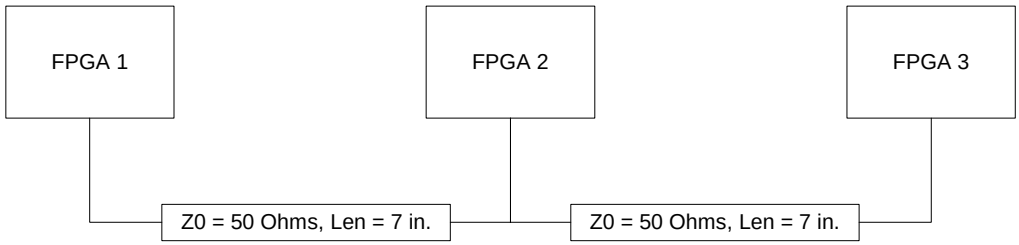
3.8.1 Pre-reading

Bogatin does not cover timing analysis in his book. Plexus has developed documentation on this subject, which is used to teach this session. There is no reading assigned this week.

3.8.2 Assignment 8

This assignment provides the participants with an opportunity to perform a simple timing analysis taking into account flight delays derived from simulation.

Using the following topology:



Make the following assumptions:
For the FPGA buffer models use PCI-X buffer models for the Virtex II Pro device
PCI 66 MHz timing parameters
Tcko = 2 ns to 6 ns
Tsup = 3 ns
Thd = 0 ns
Tclk_skew = 1 ns
PCI-X 133 MHz timing parameters
Tcko = 0.7 ns to 3.8 ns
Tsup = 1.2 ns
Thd = 0.5 ns
Tclk_skew = 0.5 ns

Using the typical process corner for simulation, find the minimum and maximum flight delays for all combinations of drivers and receivers. From these results choose the highest maximum flight delay and the lowest minimum flight delay and record them as follows.
Maximum flight delay = _____
Minimum flight delay = _____

Using the PCI 66 timing parameters calculate the setup and hold margin for 66 MHz operation (Tper = 15 ns)
66 MHz setup margin = _____
66 MHz hold margin = _____

Using the PCI-X 133 timing parameters calculate the setup and hold margin available for 133 MHz operation (Tper = 7.5 ns)
133 MHz setup margin = _____
133 MHz hold margin = _____

EXTRA CREDIT
Determine the maximum length for the segments to allow the system to run at 133 MHz.

3.9 Week 9 – Crosstalk and Simultaneous Switching Noise

Week nine focuses on noise and its effects on digital systems. Crosstalk, simultaneous switching noise (SSN), intersymbol interference (ISI), and jitter are the primary topics discussed in this session. Each subject is broken down into a definition of what it is, it's various effects, ways to measure it, and methods to mitigate it.

The session begins with a brief description of how noise can affect digital systems. Changes in signal amplitude, which can cause incorrect logic levels, and degradation of signal transitions, which can cause timing errors are just a few of the effects described. Most importantly, it must be understood that noise fundamentally limits the transmission capacity of a digital communication system. An example of an application of the Shannon theorem for data transmission capacity is provided to help describe this point. Next, each type of noise, sources for that noise, and ways to mitigate them are covered.

Crosstalk is signal energy from one signal line coupling onto another. It can be due to close proximity of transmission lines, in which case the electromagnetic fields between the lines are interacting. It can also be caused by radiated electromagnetic energy from far away signals. Crosstalk can be further broken down into two components, capacitive crosstalk, and inductive crosstalk. A detailed description of each is provided. Crosstalk can affect the magnitude of signals, and it can affect timing. For parallel busses in which several signals are switching, crosstalk can slow down or speed up the edge rate, which can cause skew between signals. For serial signals, crosstalk adds jitter through timing effects and vertical eye degradation through magnitude effects. In most cases spacing the signals farther apart will improve the effect of crosstalk. These are just a few examples of the effects of crosstalk that are discussed.

Next, the discussion moves to the topic of simultaneous switching noise. Simultaneous switching noise is generated in digital systems due to rapid changes in voltage and current caused by many circuits switching at the same time. This effect is most prominent in synchronous systems where several circuits are switching on clock edges. This effect can further be broken down to two types, on chip switching, which can cause rail collapse, and off chip switching, which can cause ground or power bounce. Each of these types of occurrences is described in detail and several methods to mitigate them such as reducing the number of simultaneous switching outputs, using slow slew rate buffers to decrease the edge rate, decoupling capacitors, etc., are discussed.

Finally, as data rates increase and systems begin using serial interfaces in the gigahertz range, jitter becomes a dominant factor. Jitter is the variation in position of a signal in time versus the ideal position of that signal based on an ideal clock. The effects of jitter in parallel synchronous systems such as degradation of setup and hold times, and in serial systems where it causes bit errors, are described in detail. Measurement conventions for jitter such as cycle-to-cycle, periodic, random and deterministic jitter separation, and total jitter, are described as methods that can help isolate sources of the jitter. These sources, thermal noise, semiconductor noise, PLL noise from power supplies, SSN, ISI, duty cycle distortion, and crosstalk, etc. are discussed in detail. Finally, measuring jitter accurately, which can be a difficult task, wraps up this session.

3.9.1 Pre-reading

The reading for this week covers most of the above topics in a clear and concise manner. Bogatin paints a clear picture of how noise affects systems and provides detailed diagrams to illustrate the contributing factors. Some of the material on jitter is based on class notes.

3.9.2 Assignment 9

The purpose of assignment 9 is to gain an intuitive understanding of how crosstalk affects the timing characteristics of a signal.

Using a Xilinx LVTTL 12mA fast slew rate FPGA model driving two adjacent traces (A and B) with the following parameters:

- 50 Ohm characteristic impedance

- 5 mil trace
- 5 mil spacing
- 10 in. long traces

Determine the affect on flight delay (TYPICAL corner only) for net B for the following cases

1) A driving low, B driving low
2) A driving low, B driving high
3) A driving high, B driving low
4) A driving low, B driving high

3.10 Week 10 – Lab Measurements

Making accurate and precise measurements is an extremely import part of the signal integrity process. Correlating simulation results to lab measurements increases confidence in the simulation tools as well as provides insight into adjustments in the simulation tool when its results do not match the measurements. Knowing what type of equipment to use and the method by which to make the measurement is the focus of this session.

The session begins with a differentiation between bandwidth, sampling rate, and rise time. Bandwidth is defined as the frequency at which a sinusoidal input signal has been attenuated by 3dB. Sampling rate is defined as samples per second. These concepts are important to understand as most test equipment is specified in terms of bandwidth and sampling rate. It is even more important to understand the effective bandwidth of the scope and probe system, as the true bandwidth of the equipment depends on both the scope and the probe. For modern high-speed scopes with a flat response, a first order approximation of the effective bandwidth of the scope and probe is the lower bandwidth of the two. For the most accurate measure of bandwidth of flat response systems, data should be obtained from the manufacturer. The performance of test equipment for digital signals also depends on the rise time of the equipment, which can be found as the step response of the scope and probe combination. The importance of both the frequency response and rise time of the equipment is stressed.

After establishing some basic information about the specifications of test equipment some specific types of equipment are described. There are two broad categories of equipment for signal integrity design, one for measuring signals and one for measuring transmission channels. In the signal measurement category, the first types measure voltage vs. time and these consist of real time oscilloscopes and sampling oscilloscopes. The operation of these types of instruments is described and they are compared and contrasted. The primary use for oscilloscopes is measurement of signal quality. The next type of signal measurement equipment discussed is the bit error rate tester (BERT). Bit error rate is the primary measurement of digital system communication performance and can be a very important tool for verifying that a design is working correctly. Some time is spent discussing the statistical nature of bit error rate measurements and two methodologies using confidence intervals are presented. The first one predicts the confidence interval of a measurement based on how many errors were counted. The second uses an error free interval to predict to a certain confidence that the true bit error rate is below a certain level. A new type of test equipment called a BERT scope that is a cross between a BERT and a traditional oscilloscope is also described. BERT scopes can vary the decision voltage threshold and decision sampling time to construct an eye diagram. They can perform statistical bit error analysis and make very accurate jitter measurements. The final type of signal measurement equipment discussed is the time interval analyzer (TIA) used for measuring timing relationships such as jitter. Several tips are offered for making measurements with each of theses types of equipment.

The second broad category of test equipment is for measuring the characteristics of transmission channels. Examples discussed are time-domain reflectometry (TDR) and time-domain transmission (TDT) analyzers and vector network analyzers (VNA) are useful for signal integrity analysis as well. TDRs measure impedance and capacitive/inductive discontinuities in transmission channels, which can cause signal reflections. They provide an intuitive display of transmission line characteristics in the time domain and allow extraction of s-parameters though software, which can be used in the simulation tools. VNAs are useful for measuring s-parameters in the frequency domain as well as the ability to measure and characterize small parasitics.

The lab measurement session wraps up with a detailed discussion on measurement techniques and sources of error when making the measurements. Distortion due to ground clips of probes and large ground loops, distortion due to probe input characteristics, and methods to mitigate theses effects complete this session.

3.10.1 Pre-reading

The reading for this week focuses on concept of bandwidth and how it relates to measurement equipment. Bogatin also provides information on using a TDR for measuring reflection.

3.10.2 Assignment 10

There is not an assignment for this week.

3.11 Week 11 – Preroute Simulation

Preroute simulation to determine flight delay and signal quality is an integral part of the Plexus design process. Nearly every project in product development has some amount of preroute simulation performed on it. This session begins with a discussion on identifying when and where preroute simulation is needed, what tools can be used to perform this analysis, and a detailed demonstration using a practical design to determine flight delay, appropriate loading, topology, and termination for good signal quality.

Simulation is no longer only necessary for high-speed signals. Heavily loaded busses and long daisy chains operating below 100MHz can still cause major problems unless carefully designed. Several block diagrams for both low and high-speed designs are shown and the group identifies potentially problematic signals. Any bus with more than 3 loads, or large daisy chains can have timing and signal quality problems from reflections. Signals above 100MHz should always be simulated for flight delay to be included in the timing analysis. Any signal above 100MHz connected to an IC on a 90nm process should be checked for overshoot and undershoot violations. And of course, signals running at 400Mbps and above should always be simulated. Now that a solid understanding for identifying problematic signals has been established, the session moves to a demonstration of the preroute tools.

The tool demonstration begins by describing a typical design scenario where a heavily loaded bus from a processor communicates to SDRAM, flash, an Ethernet PHY, etc. Certain bits of the address, data, and control lines are loaded differently, i.e. some have five loads, some three, etc. A timing analysis has already been performed on this interface and simulation is used to determine flight delay for use in conjunction with the timing analysis, as well as signal quality; will the design work as is or must topologies change to improve signal quality? The current layout of the board shows that a daisy chain topology provides the easiest routing strategy, and estimates can be made for trace length. With all of this information gathered, the tool is invoked, set up to yield the required information, and simulation begins. Topology changes are made, termination added, and tradeoffs are performed to maximize the potential for the design to work correctly on the first pass.

3.11.1 Pre-reading
There is no reading assigned this week.

3.11.2 Assignment 11
There is not an assignment for this week.

3.12 Week 12 – Post Route Simulation
This session focuses mainly on the process used to perform post route signal integrity simulation at Plexus. The main area where this is used within the Plexus signal integrity design flow is for crosstalk analysis. The session focuses on the details of using a post route simulation tool such as Cadence Specctraquest (Allegro SI 610). The goal of the session is for engineers to be able to run the tools used at Plexus for doing this analysis. Specific things that are covered are entering a PCB stackup cross section, creating models, assigning models to parts, setting up simulation parameters, setting up multi-board simulations with cables and connectors, and generating waveforms and reports. The session is based on stepping through the post route signal integrity simulation for an actual past design. Many of the steps of setting up the tool are documented in notes that are given to the engineers for future reference.

3.12.1 Pre-reading
There is no reading assigned for this week.

3.12.2 Assignment 12
The best application of the material in this session would be practical experience on a real project so no assignment is given.

3.13 Week 13 – Constraint Management
Along the same lines as week 12, this session focuses on the process used to perform constraint management. The session focuses on the details of using the constraint manager within the Cadence Allegro tool set to perform constraint management. The purpose of constraints is to communicate from the hardware engineer the PCB placement and routing guidelines necessary for the design to work correctly based on preroute simulation and analysis. With the current constraint management tools available it is not possible to completely eliminate a PCB guidelines document because not everything can be constrained in an effective way. So the session contains some examples of PCB guidelines documents and what to include in them such as board stack-up information, identification of spacing requirements and signal impedances, and a brief review of everything that is implemented in the constraint manager. Also, the PCB guidelines document generally contains information necessary for the placement and routing of the power supply sections of a design since this information is not easily implemented in constraint manager.

After covering the PCB guidelines document, the use of the constraint manager is presented for entering the most common types of constraints. These constraints include pin-to-pin delay or length constraints, length matching constraints, overall total length constraints, and routing topology constraints. Special attention is also given to differential pair routing constraints such as matching between the two signals in a pair, spacing rules, and rules governing allowable separation when routing around obstacles such as vias and BGA pin fields. The use of the tool is demonstrated by actually implementing constraints in a real design. Many of the steps of setting up the tool are documented in the notes that are given to the engineers for future reference.

3.13.1 Pre-reading
There is no reading assigned this week.

3.13.2 Assignment 13
The best application of the material in this session would be practical experience on a real project so no assignment is given.

3.14 Week 14 – Advanced Topics
The purpose of this session is to provide an introduction to some advanced topics that are becoming increasingly important in signal integrity design. These topics apply to data rates above 1 Gbps. The session focuses on the topics of frequency domain modeling of interconnections, the concept of the bit error rate and how it relates to serial digital multi-gigabit communication systems, and on some advanced differential pair topics. The first topic for discussion is the use of S-parameters for describing the frequency dependent behavior of transmission channel elements. The concept of S-parameters is introduced and an example of how they are computed for a simple circuit network is given. Normalization of S-parameters is covered next. The concepts of input return loss and insertion loss are covered in relation to S-parameters. Next, the sources of S-parameters such as field solvers and VNAs are discussed. Finally, the use of S-parameters in circuit simulation or the conversion of S-parameters to behavioral SPICE circuit models for use in simulation is presented. No actual details of how to perform these simulations are given, as the purpose is mainly to provide exposure to the topic.

The next advanced topic presented is the relationship between jitter and the bit error rate in a multi-gigabit serial interconnection. This presentation is based on material contained in the Fibre Channel Methodologies for Jitter and Signal Quality Specification (MJSQ). The concepts of the probability density function for the edge position of a bit is discussed based on deterministic and random jitter components. The bathtub curve of probability of a bit error versus sampling position is introduced. The bathtub curve is a plot of the cumulative probability that a transition occurs beyond a given sampling point and that is the probability of a bit error.

The final topic covered relates to differential signaling in digital systems. The concepts of odd and even modes are discussed both in terms of impedance and signal component. Time is spent talking about the return current path of a differential signal. The different types of coupling within a PCB such as edge coupled and broadside coupled are compared. Examples are demonstrated using a 2D field solver to show the effects on impedance of the different parameters. Finally, some focus is given to termination of differential signals.

3.14.1 Pre-reading
There is no material in Bogatin's book relating to S-parameters, the relationship of jitter to bit error rate, or the statistical measurement of bit error rate. The topic of S-parameters is based on chapter 4 in Digital Signal Integrity Modeling and Simulation with Interconnects and Packages by Brian Young. The statistics of bit error rate is based on class notes created from a statistics textbook. Bogatin covers the topic of differential pairs and that is what the reading focuses on.

3.14.2 Assignment 14
There is not an assignment given for this week.

4 Delivery of the Signal Integrity Training

The implementation of this training at Plexus has been meetings every other week over lunch with lunch provided to minimize the impact on productivity of the participants. The class notes have been developed in power point format and are presented in the meetings on a projector. Plexus has design centers located in Boulder, CO and Raleigh, NC in addition to Neenah WI where the training is initiated. Participants have come from all design centers and remote design centers are included in the training through Web EX. This tool allows the slides to be displayed to the remote participants as well as sharing of the applications during demonstrations. A lab tour is included after week 10 to demonstrate the usage of the TDR. At this time, the tour has only been offered locally.

The training course has been successfully taught to 5 digital design engineers and 1 analog design engineer. These engineers have performed SI analysis on multiple projects and have greatly expanded the capabilities of Plexus for offering signal integrity design services. Currently the course is being offered again to a total of 19 people spread across the design centers. So far experience has shown that this is the upper limit of the number of people to include in the course at once.

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