

Single chip 2.4 GHz Transmitter

nRF2402

FEATURES

- True single chip GFSK transmitter in a small 16-pin package (QFN16 4x4)
- Adjustable output power up to 0dBm
- Data rate 0 to 1Mbps
- Low Bill of Material
- Multi Channel operation
 - 128 channels
 - Support frequency hopping
 - Channel switching time <200µs.
- Power supply range: 1.9 to 3.6 V
- CRC computation
- ShockBurst™ mode for ultra-low power operation
- Low supply current, typical 10mA peak @ -5dBm output power
- World wide use

APPLICATIONS

- Wireless mouse, keyboard, joystick
- Keyless entry
- Wireless data communication
- Alarm and security systems
- Home Automation
- Remote control
- Surveillance
- Automotive
- Telemetry
- Intelligent sports equipment
- Industrial sensors
- Toy

GENERAL DESCRIPTION

nRF2402 is a single-chip radio transmitter for the world wide 2.4 - 2.5 GHz ISM band. The transmitter consists of a fully integrated frequency synthesizer, a power amplifier, a crystal oscillator and a modulator. Output power and frequency channel is easily programmable by use of the 3-wire interface. Current consumption is very low, only 10 mA at an output power of -5dBm. Built-in ShockBurst™ and Power Down modes makes power saving easily realizable.

QUICK REFERENCE DATA

Parameter	Value	Unit
Minimum supply voltage	1.9	V
Maximum output power	0	dBm
Maximum GFSK data rate	1000	kbps
Supply current GFSK transmitter @ -5dBm output power	10	mA
Supply current in Power Down mode	200	nA

Table 1 nRF2402 quick reference data

Type Number	Description	Version
nRF2402 IC	16 pin QFN 4x4	A

Table 2 nRF2402 ordering information



BLOCK DIAGRAM

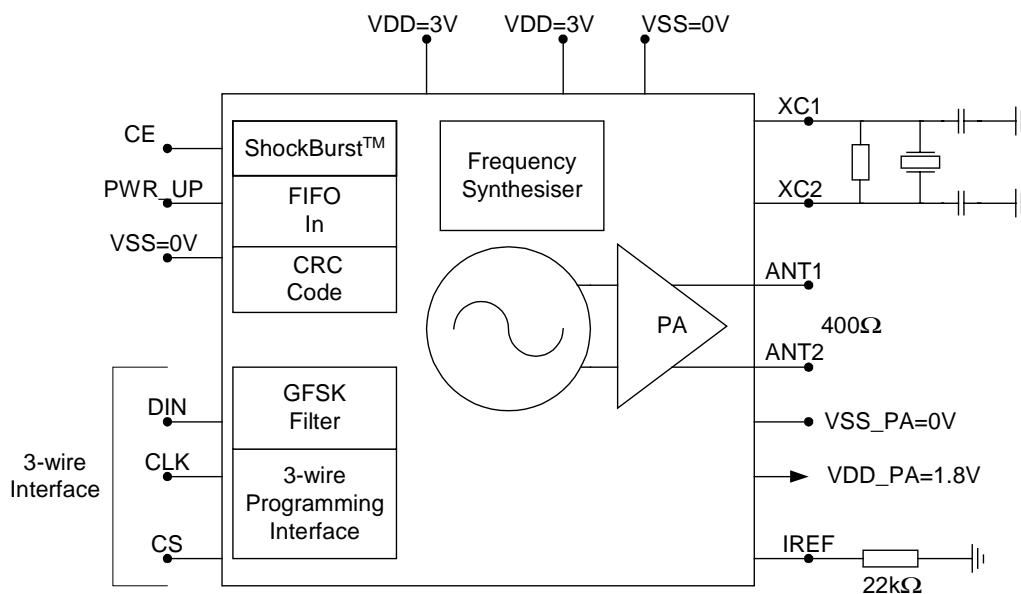


Figure 1 nRF2402 with external components.

PIN FUNCTIONS

Pin	Name	Pin function	Description
1	CE	Input	Chip Enable Activates TX mode
2	CS	Input	Chip Select Activates Configuration Mode
3	CLK	Input	Clock Input TX Data and 3-wire Interface
4	DIN	Input	TX Data Input / Configuration Data Input
5	VSS	Power	Ground (0V)
6	XC2	Output	Crystal pin 2
7	XC1	Input	Crystal pin 1
8	VDD	Power	Power Supply (+3V DC)
9	VSS_PA	Power	Ground (0V)
10	ANT1	Power/RF	Antenna output 1
11	ANT2	Power/RF	Antenna output 2
12	VDD_PA	Power Output	Power Supply (+1.8V DC) to the PA
13	VDD	Power	Power Supply (+3V DC)
14	IREF	Input	Reference current
15	VSS	Power	Ground (0V)
16	PWR_UP	Input	Power Up

Table 3 nRF2402 pin functions



nRF2402 Single Chip 2.4 GHz Radio Transmitter

PIN ASSIGNMENT

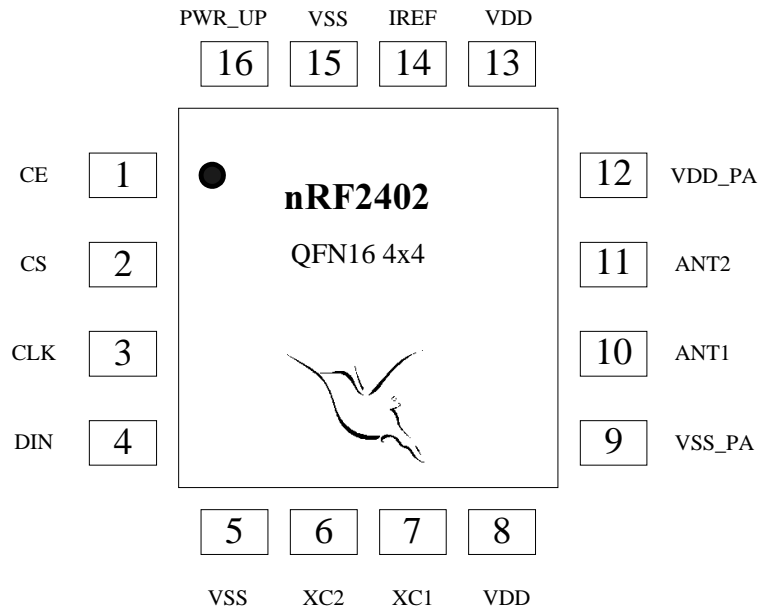


Figure 2. nRF2402 pin assignment (top view).



ELECTRICAL SPECIFICATIONS

Conditions: VDD = +3V, VSS = 0V, T_A = - 40°C to + 85°C

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
Operating conditions						
VDD	Supply voltage		1.9	3.0	3.6	V
TEMP	Operating Temperature		-40	+27	+85	°C
Digital input pin						
V _{IH}	HIGH level input voltage		VDD- 0.3		VDD	V
V _{IL}	LOW level input voltage		Vss		0.3	V
Digital output pin						
V _{OH}	HIGH level output voltage (I _{OH} =-0.5mA)		VDD- 0.3		VDD	V
V _{OL}	LOW level output voltage (I _{OL} =0.5mA)		Vss		0.3	V
General RF conditions						
f _{OP}	Operating frequency	1)	2400		2527	MHz
f _{XTAL}	Crystal frequency	2)	4		20	MHz
Δf	Frequency deviation		±115	±156	±175	kHz
R _{GFSK}	GFSK data rate ShockBurst™		>0		1000	kbps
R _{GFSK}	GFSK data rate Direct Mode	3)	250		1000	kbps
F _{CHANNEL}	Channel spacing		1			MHz
Transmitter operation						
P _{RF}	Maximum Output Power	4)		0	+4	dBm
P _{RFC}	RF Power Control Range		16	20		dB
P _{RFCR}	RF Power Range Control Resolution				±3	dB
P _{BW}	20dB Bandwidth for Modulated Carrier				1000	kHz
P _{RF2}	2 nd Adjacent Channel Transmit Power 2MHz				-20	dBc
P _{RF3}	3 rd Adjacent Channel Transmit Power 3MHz				-40	dBc
I _{VDD}	Supply current @ 0dBm output power	5)		11.5	13	mA
I _{VDD}	Supply current @ -5dBm output power	5)		10.0	11	mA
I _{VDD}	Average Supply current @ -5dBm output power, ShockBurst™	6)		500		μA
I _{VDD}	Average Supply current in stand-by mode			12		μA
I _{VDD}	Average Supply current in power down			200		nA

NOTES:

- 1) Usable band is determined by local regulations
- 2) The crystal frequency may be chosen from 5 different values (4, 8, 12, 16, and 20MHz) which are specified in the configuration word, see Table 8. 16MHz are required for 1Mbps operation.
- 3) Data rate must be either 250kbps or 1000kbps.
- 4) Antenna load impedance = 400 Ω
- 5) Antenna load impedance = 400 Ω. Effective data rate 250kbps or 1Mbps.
- 6) Antenna load impedance = 400 Ω. Effective data rate 10kbps.

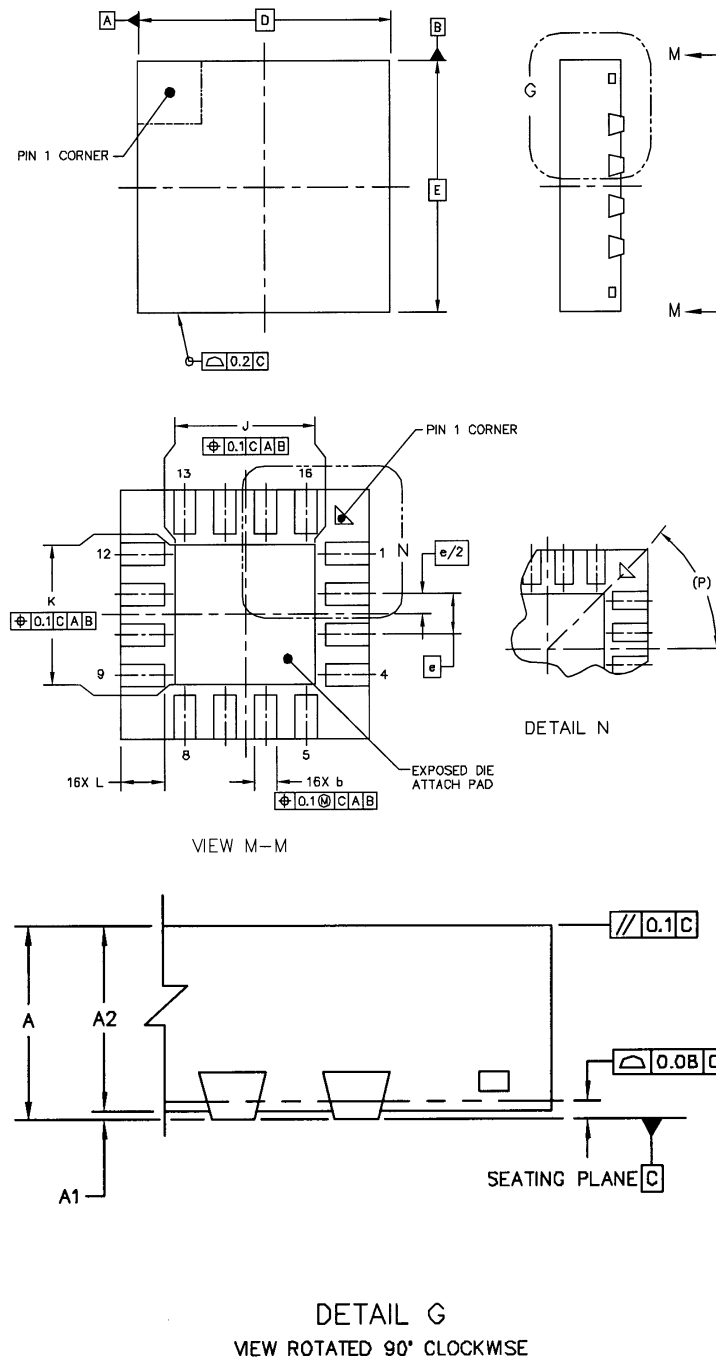
Table 4 nRF2402 electrical specifications



nRF2402 Single Chip 2.4 GHz Radio Transmitter

PACKAGE OUTLINE

nRF2402, uses the QFN16 4x4 package. Dimensions are in mm.



Package Type		A	A ₁	A ₂	b	D	E	e	J	K	L	P			
QFN16 (4x4 mm)	Min	0.8	0.0	0.75	0.23	4 BSC	4 BSC	0.65 BSC	0.75	0.7	0.45	45°			
	typ.				0.3									0.55	REF
	Max	1	0.05	1	0.38									0.75	

Figure 3 nRF2402 Package outline.



ABSOLUTE MAXIMUM RATINGS

Supply voltages

VDD - 0.3V to + 3.6V

VSS..... 0V

Input voltage

V_I..... - 0.3V to VDD + 0.3V

Output voltage

V_O..... - 0.3V to VDD + 0.3V

Total Power Dissipation

P_D (T_A=85°C)..... 35mW

Temperatures

Operating Temperature.... - 40°C to + 85°C

Storage Temperature..... - 40°C to + 125°C

Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.

ATTENTION!

Electrostatic Sensitive Device

Observe Precaution for handling.





GLOSSARY OF TERMS

Term	Description
CLK	Clock
CRC	Cyclic Redundancy Check
CS	Chip Select
CE	Chip Enable
GFSK	Gaussian Frequency Shift Keying
ISM	Industrial-Scientific-Medical
MCU	Micro Controller Unit
OD	Overdrive
PWR_DWN	Power Down
PWR_UP	Power Up
RX	Receive
ST_BY	Standby
TX	Transmit

Table 5 Glossary



MODES OF OPERATION

Overview of Operational Modes

Table 6 provides an overview of the different modes that the nRF2402 may be set to.

Mode	PWR UP	CE	CS
Transmit	1	1	0
Configuration	1	0	1
Stand By	1	0	0
Power Down	0	X	X

Table 6 Overview of Operational Modes of nRF2402.

Active Modes

The nRF2402 has two transmit modes:

- ShockBurst™
- Direct Mode

The device functionality in these modes is determined by the content of a configuration word. This configuration word is presented in the configuration section.

ShockBurst™

The ShockBurst™ technology uses on-chip FIFO to clock in data at a low data rate and transmit at a very high rate thus enabling extreme reduction in power consumption.

When operating the nRF2402 (in co-operation with nRF2401/nRF24E1) in ShockBurst™, you gain access to the high data rates (1 Mbps) offered by the 2.4 GHz band without the need of a costly, high-speed micro controller (MCU) for data processing.

By putting all high speed signal processing related to RF protocol on-chip, the nRF2402 offers the following benefits:

- Highly reduced current consumption
- Lower system cost (facilitates use of less expensive micro controller)
- Greatly reduced risk of ‘on-air’ collisions due to short transmission time

The nRF2402 can be programmed using a simple 3-wire interface where the data rate is decided by the speed of the micro controller.

By allowing the digital part of the application to run at low speed while maximizing the data rate on the RF link, the nRF ShockBurst™ mode reduces the average current consumption in applications considerably.



nRF2402 Single Chip 2.4 GHz Radio Transmitter

ShockBurst™ principle

When the nRF2402 is configured in ShockBurst™, TX operation is conducted in the following way (10 kbps for this example only).

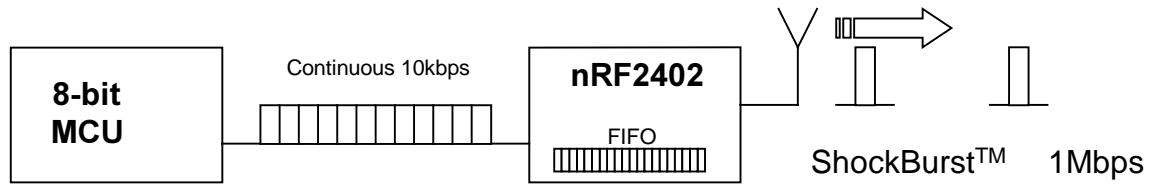


Figure 4 Clocking in data with MCU and sending with ShockBurst™ technology

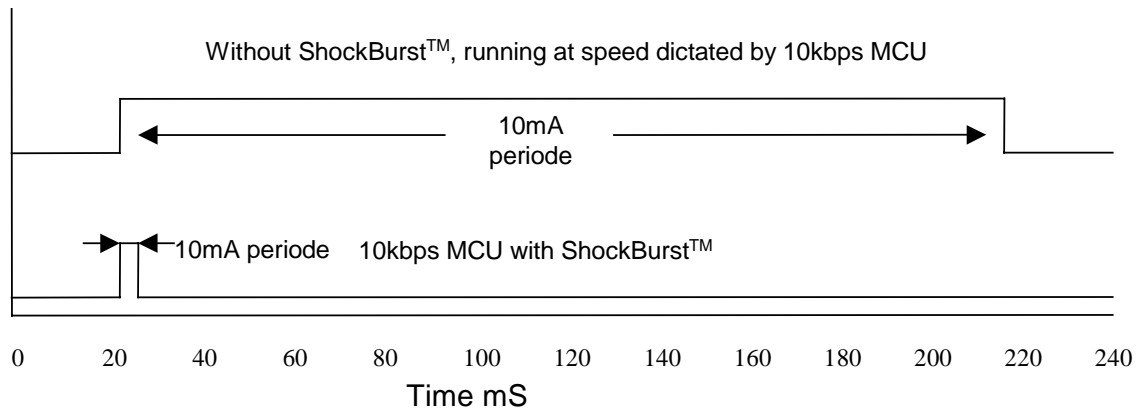


Figure 5 Current consumption with and without ShockBurst™ technology

nRF2402 ShockBurst™ Transmit:

MCU interface pins: CE, CLK, DIN

1. When the application MCU has data to send, set CE high. This activates RF2402 on-board data processing.
2. The address of the receiving node (RX address) and payload data is clocked into the nRF2402. The application protocol or MCU sets the speed (ex: 10kbps).
3. MCU sets CE low, this activates a nRF2402 ShockBurst™ transmission.
4. nRF2402 ShockBurst™:
 - RF front end is powered up
 - RF package is completed (preamble added, CRC calculated)
 - Data is transmitted at high speed (250 kbps or 1 Mbps configured by user).
 - nRF2402 returns to stand-by when finished

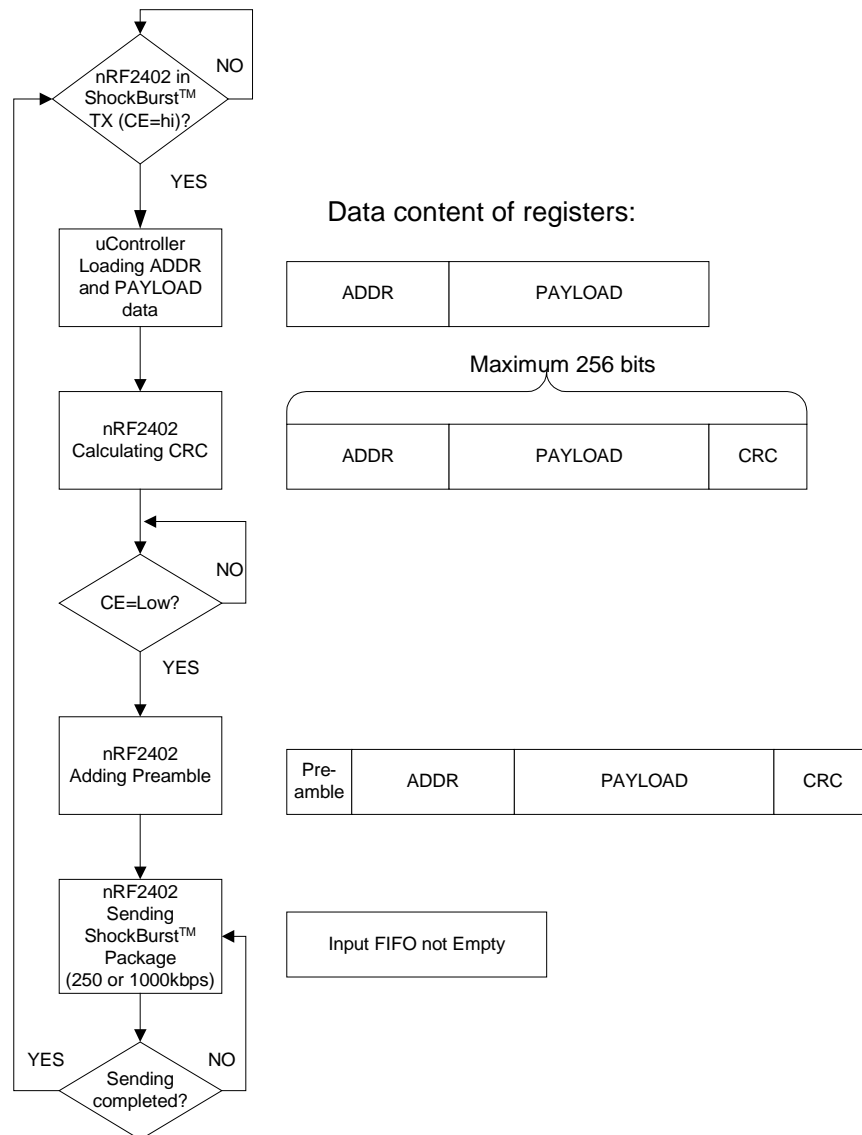


Figure 6 Flow Chart ShockBurst™ Transmit of nRF2402 with CRC and preamble.



Direct Mode

In direct mode the nRF2402 works like a traditional RF device. Data must be at 1Mbps, or 250kbps for the receiver (nRF2401/nRF24E1) to detect the signals.

MCU interface pins: CE, DIN

1. When application MCU has data to send, set CE high
2. The nRF2402 RF front end is now immediately activated, and after 200 μ s settling time, data will modulate the carrier directly.
3. All RF protocol parts must hence be implemented in MCU firmware (preamble, address and CRC).

Configuration Mode

In configuration mode a configuration word of up to 20 bits is downloaded to nRF2402. This is done through a simple 3-wire interface (CS, CLK and DIN). For more information on configuration please refer to the nRF2402. Device configuration chapter, page12.

Power Down Mode

Power down mode is used to achieve very low current consumption. Effectively the chip is disabled with minimal leakage current consumption, typically less than 200nA. Operating in this mode when not transmitting data significantly increases battery lifetime.

Stand-By Mode

Stand by mode is used to achieve low current consumption. In this mode only a part of the crystal oscillator is running (12 μ A) to guarantee a short start-up time. Operating in this mode when not transmitting data increases battery lifetime while keeping start up delays short.

Pin configuration for the different modes of nRF2402

nRF2402 MODES	INPUT PINS				
	PWR_UP	CE	CS	CLK	DIN
Power down	0	0	X	X	X
Stand by	1	0	0	X	X
Configuration	1	0	1	CLK	CONFIG DATA
TX ShockBurst™	1	1	0	CLK	TX DATA
TX Direct	1	1	0	Set to 0*	TX DATA

Table 7 Pin configuration of nRF2402.

* CLK not used in direct mode.



DEVICE CONFIGURATION

All configuration of the nRF2402 is done via a 3-wire interface to a single configuration register. The configuration word can be up to 20 bits long for ShockBurst™ use and up to 14 bits long for direct mode.

Configuration for ShockBurst™ operation

The configuration word in ShockBurst™ enables the nRF2402 to handle the RF protocol (in co-operation with nRF2401/nRF24E1). Once the protocol is completed and loaded into nRF2402 only seven bits, also used in direct mode, needs to be updated during operation.

The configuration bits dedicated to ShockBurst™ is as follows:

- Preamble: Generation of preamble in transmitted data.
- CRC: Enables nRF2402 on-chip CRC generation.

NOTE:

The MCU must generate an address and a payload section that fits the configuration of the nRF2401/nRF24E1 that is to receive the data.

When using the nRF2402 on-chip CRC feature ensure that CRC is enabled and uses the same length for both the nRF2402 and the receiving nRF2401/nRF24E1 devices.

PRE-AMBLE	ADDRESS	PAYLOAD	CRC
-----------	---------	---------	-----

Figure 7 Data packet set-up



Configuration for Direct Mode operation

For direct mode operation only the 14 first bits (bit[13:0]) of the configuring word is relevant. For ShockBurst™ also bit[17:14] must be configured.

Configuration Word overview

	Bit position	Number of bits	Name	Function
General device configuration	19	6	PLL Control	Close the PLL for test.
	18	1		UNUSED
	17	1	PREAMBLE	Enable on-chip PREAMBLE generation
	16	1	PREAMBLE	8 or 4 bit PREAMBLE
	15	1	CRC	8 or 16 bit CRC
	14	1	CRC	Enable on-chip CRC generation
	13	1	CM	Communication mode (Direct or ShockBurst™)
	12	1	RFDR_SB	RF data rate (1Mbps requires 16MHz crystal)
	11:9	3	XO_F	Crystal frequency
	8:7	2	RF_PWR	RF output power
6:0	7	RF_CH#	Frequency channel (0 to 127)	

Table 8 Table of configuration words.

The configuration word is shifted in MSB first on positive CLK edges. New configuration is enabled on the negative edge of CS.

NOTE!

On the negative edge of CS, the nRF2402 updates the number of bits actually shifted in during the last configuration.

Ex:

If the nRF2402 is to be configured for Preamble and CRC in ShockBurst™, a total of 17 bits must be shifted in during the first configuration after VDD is applied.

Once the wanted "protocol", modus and RF channel are set there is no need to update this part of the configuration during operation.



Configuration Word Detailed Description

The following describes the function of the 32 bits (bit 31 = MSB) that is used to configure the nRF2401.

General Device Configuration: bit[13:0]

ShockBurst™ Configuration: bit[17:14]

Test Configuration: bit[31:18]

TEST		ShockBurst				Default
D19	D18	D17	D16	D15	D14	
PLL		PRE_EN	PRE_L	CRC		0
0	0	1	1	0	0	

RF-Programming													LSB		Default
D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D0	
Burst	OD	XO Frequency			RF Power		Channel selection								
0	0	1	1	1	1	0	0	0	0	0	0	0	1	0	

The MSB bit should be loaded first into the configuration register.

Default configuration word: h3.0F02.

Test configuration

Bit 19:

PLL: For test purposes the PLL may be closed (non-operational).
 Logic 0: Open loop (normal operation)
 Logic 1: Closed loop (test only)

Bit 18:

Not used:



ShockBurst™ configuration

The section bit[17:14] contains the segments of the configuration register dedicated to ShockBurst™ operation. After VDD is turned on ShockBurst™ configuration is done once and remains set whilst VDD is present. During operation only the 7 bits for frequency channel normally need to be changed.

PREAMBLE		CRC	
17	16	15	14

Table 9 Preamble and CRC settings.

Bit 17:

PRE_EN: Preamble to be generated by nRF2402 in ShockBurst™.
 Logic 0: No generation of Preamble
 Logic 1: Preamble generation enabled (default)

Bit 16:

PRE_L: Selecting 8 or 4 bit Preamble.
 Logic 0: 4 bit Preamble.
 Logic 1: 8 bit Preamble (default)

Bit 15:

CRC_L: CRC length to be calculated by nRF2402 in ShockBurst™.
 Logic 0: 8 bit CRC (default)
 Logic 1: 16 bit CRC

Bit 14:

CRC_EN: Enables on-chip CRC generation (TX)
 Logic 0: On-chip CRC generation disabled (default)
 Logic 1: On-chip CRC generation enabled

NOTE:

An 8 bit CRC (compared to 16 bit) will increase the number of payload bits possible in each ShockBurst™ data packet, but will also reduce the communication integrity.

General device configuration:

This section of the configuration word handles RF and device related parameters.

Burst	OD	XO F			RF PWR	
13	12	11	10	9	8	7

Table 10 RF operational settings.

Bit 13:

Burst: Logic 0: nRF2402 operates in direct mode (default)
 Logic 1: nRF2402 operates in ShockBurst™ mode



DATA PACKAGE DESCRIPTION

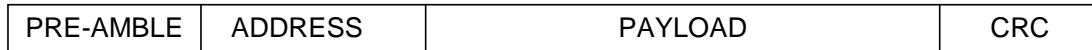


Figure 8 Data Package Diagram

The data packet for both ShockBurst™ mode and direct mode communication is divided into 4 sections. These are:

1. PREAMBLE	<ul style="list-style-type: none"> The preamble field is a requirement for ShockBurst™ and Direct modes Preamble is 8 (or 4) bits in length and is dependent on the 1st data bit. <table style="margin-left: 20px;"> <tr> <td>PREAMBLE</td> <td>1st Data Bit (Address)</td> </tr> <tr> <td>01010101</td> <td>0</td> </tr> <tr> <td>10101010</td> <td>1</td> </tr> </table> Preamble is automatically added to the data packet and thereby gives extra space for payload in ShockBurst™. Preamble must be added by MCU in Direct mode 	PREAMBLE	1 st Data Bit (Address)	01010101	0	10101010	1
PREAMBLE	1 st Data Bit (Address)						
01010101	0						
10101010	1						
2 ADDRESS	<ul style="list-style-type: none"> The address field is required in ShockBurst™ mode. 						
3 PAYLOAD	<ul style="list-style-type: none"> The data to be transmitted In ShockBurst™ mode payload size is 256 bits minus the following: (Address: 8 to 40 bits. + CRC 8 or 16 bits). In Direct mode the maximum payload size is defined by 1Mbps for 4ms: 4000 bits minus the following: (Preamble: 8 (or 4) bits. + Address: 0 to 40 bits. + CRC: 0, 8 or 16 bits). 						
4 CRC	<ul style="list-style-type: none"> On chip CRC calculation is an option in ShockBurst™ mode, and is not used in Direct mode. 8 or 16 bits length 						

Table 14 Data package



IMPORTANT TIMING DATA

The following timing applies for operation of nRF2402.

nRF2402 Timing Data

nRF2402 timing	Min.	Max.	Name
PWR_DWN → Configuration mode		3ms	Tpd2cfgm
PWR_DWN → Active mode (TX)		3ms	Tpd2a
ST_BY → TX ShockBurst™		195µs	Tsby2txSB
ST_BY → TX Direct Mode		202µs	Tsby2txDM
Minimum delay from CS to data.	5µs		Tcs2data
Minimum delay from CE to data.	5µs		Tce2data
Delay between edges	50ns		Td
Setup time	500ns		Ts
Hold time	500ns		Th
Delay to finish internal GFSK data	1/data rate		Tfd
Minimum input clock high	500ns		Thmin

Table 15 Switching times for nRF2402

When the nRF2402 is powered up it must always settle in stand by for 3ms before it can enter configuration or active mode.

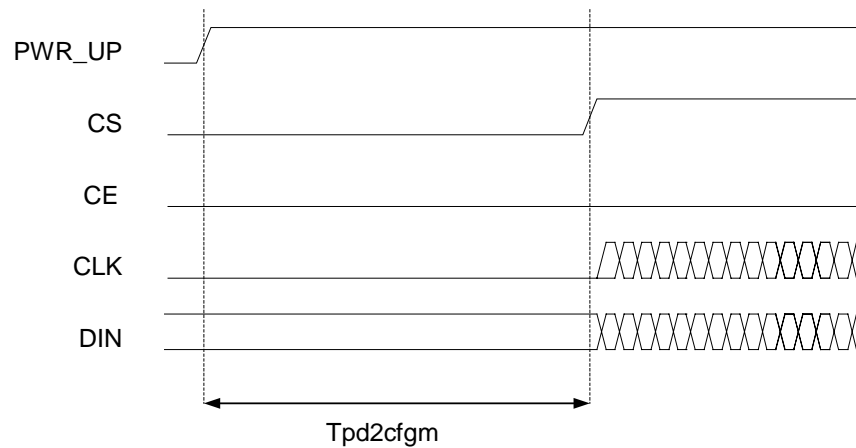


Figure 9 Timing diagram for power down (or VDD off) to configuration mode for nRF2402.

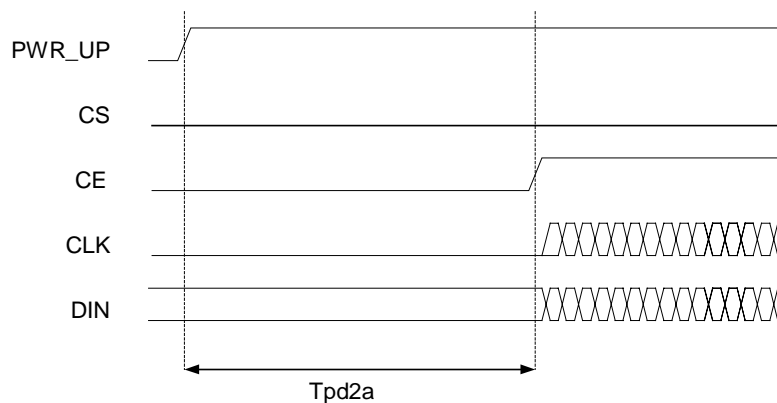


Figure 10 Power down (or VDD off) to active mode



Note that the configuration word will be lost when VDD is turned off and that the device then must be configured before going to active mode. If the device is configured one can go directly from power down to active mode.

Note:

CE and CS may not be high at the same time. Setting one or the other decides whether configuration or active mode is entered.

Configuration Mode

In configuration mode the transmitter is configured to its output power, transmit frequency, data rate, CRC, and preamble. The configuring data will be loaded during the Chip Select period (CS="1"). A random number of bits between 1 and 20 may be shifted in to the register to configure the transmitter, but normally you would at least shift in the seven channel frequency bits. The transmitter is configured on the negative edge of CS.

When one or more of the bits in the configuration word needs to be changed the following timing apply.

Configuration Mode Timing

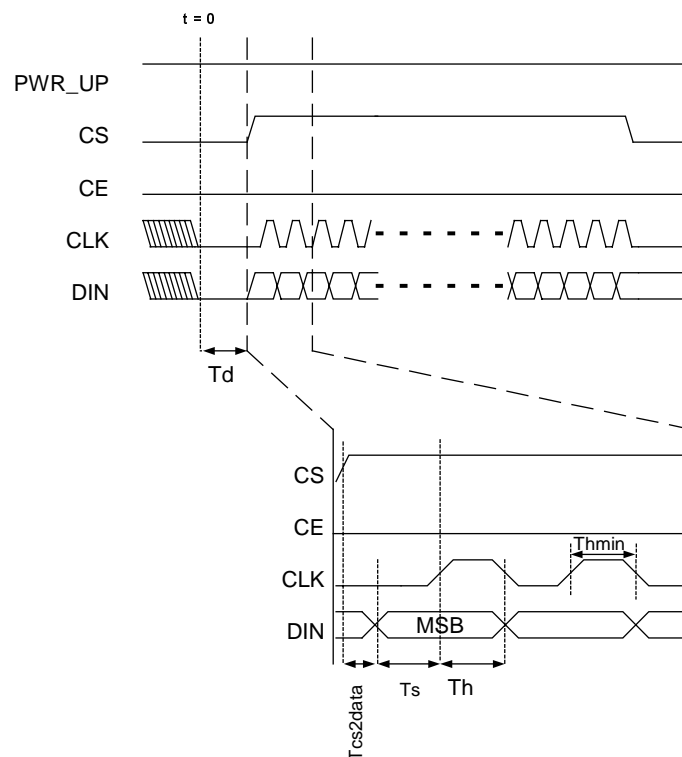


Figure 11 Timing Diagram of Configuration Mode

If configuration mode is entered from power down, CS can be set high after Tpd2sby as shown in Figure 9.



ShockBurst™ Mode Timing

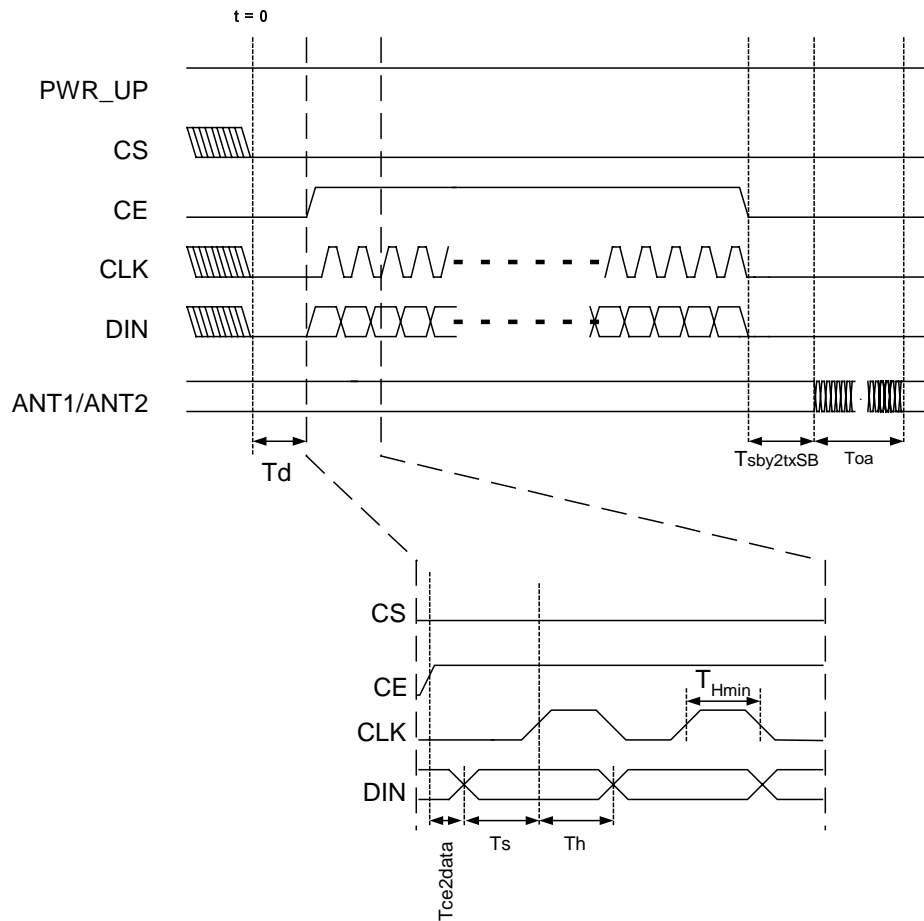


Figure 12 Timing of ShockBurst™ in nRF2402.

The package length and the data rate give the delay T_{OA} (time on air), as shown in the equation.

$$T_{OA} = 1 / \text{datarate} \cdot (\# \text{ databits} + 1)$$



Direct Mode Timing

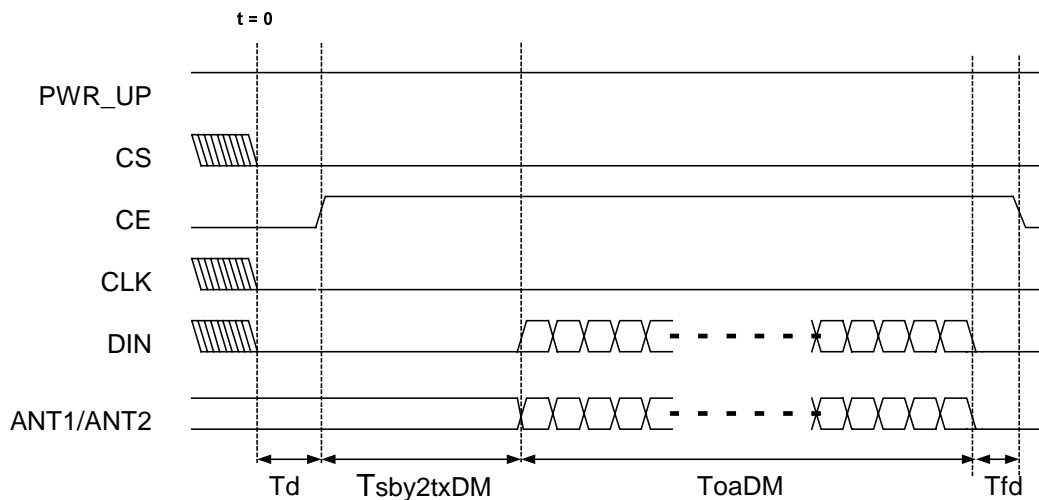


Figure 13 Timing Diagram of Direct Mode

In direct mode the input data will be sampled by nRF2402 and therefore no clock is needed. The clock must be stable at low level during transmission due to noise considerations. The exact delay $T_{sby2txDM}$ is given by the equation:

$$T_{sby2txDM} = 194\mu s + 1/F_{XO} \cdot 20 + 2.25\mu s$$



PERIPHERAL RF INFORMATION

Antenna output

The ANT1 and ANT2 output pins provide a balanced RF output to the antenna. The pins must have a DC path to VDD_PA, either via an RF choke or via the center point in a dipole antenna. The load impedance seen between the ANT1/ANT2 outputs should be in the range 200-700Ω. Load impedance of 400Ω is recommended for maximum output power (0dBm). Lower load impedance (for instance 50 Ω) can be obtained by fitting a simple matching network or a RF transformer (balun).

Output Power adjustment

Power setting bits of configuring word	RF output power	DC current consumption
11	0 dBm ±3dB	11.5 mA
10	-5 dBm ±3dB	10.0 mA
01	-10 dBm ±3dB	8.5 mA
00	-20 dBm ±3dB	7.0 mA

Conditions: VDD = 3.0V, VSS = 0V, T_A = 27°C, Load impedance = 400 Ω.

Table 16 RF output power setting for the nRF2402.

Crystal Specification

Tolerance includes initially accuracy and tolerance over temperature and aging.

Frequency	C _L	ESR	C _{0max}	Tolerance
4	12pF	150 Ω	7.0pF	±30ppm
8	12pF	100 Ω	7.0pF	±30ppm
12	12pF	100 Ω	7.0pF	±30ppm
16	12pF	100 Ω	7.0pF	±30ppm
20	12pF	100 Ω	7.0pF	±30ppm

Table 17 Crystal specification of the nRF2402

To achieve a crystal oscillator solution with low power consumption and fast start-up time, it is recommended to specify the crystal with a low value of crystal load capacitance. Specifying C_L=12pF is OK, but it is possible to use up to 16pF. Specifying a lower value of crystal parallel equivalent capacitance, Co is also good, but this can increase the price of the crystal itself. Typically Co=1.5pF at a crystal specified for Co_max=7.0pF.



DEFINITIONS

Data sheet status	
Objective product specification	This datasheet contains target specifications for product development.
Preliminary product specification	This datasheet contains preliminary data; supplementary data may be published from Nordic VLSI ASA later.
Product specification	This datasheet contains final product specifications. Nordic VLSI ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 18. Definitions.

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LIFE SUPPORT APPLICATIONS

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Product Specification: Revision Date: 25/08/2003.

Datasheet order code: 250803-nRF2402.

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Main Office:

Vestre Rosten 81, N-7075 Tiller, Norway

Phone: +47 72 89 89 00, Fax: +47 72 89 89 89

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