SMDK6400 Evaluation Board for S3C6400

1. PCB Revision

Date	Description
2006. 12. 12	Preliminary Version

2. Table of Contents

CPU Board

Page	Function
01	S3C6400(Addr/Data)
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05	Memory(OneNand)/JTAG/CLK
06	Buffers(SROM I/F)
07	USB/USB OTG/MIPI
08	HS_MMC/HS_SPI
09	CPU B/D Power1(ARM, INT)
0A	CPU B/D Power2(Alive, I/O)
0B	Board to Board Connector (CPU)

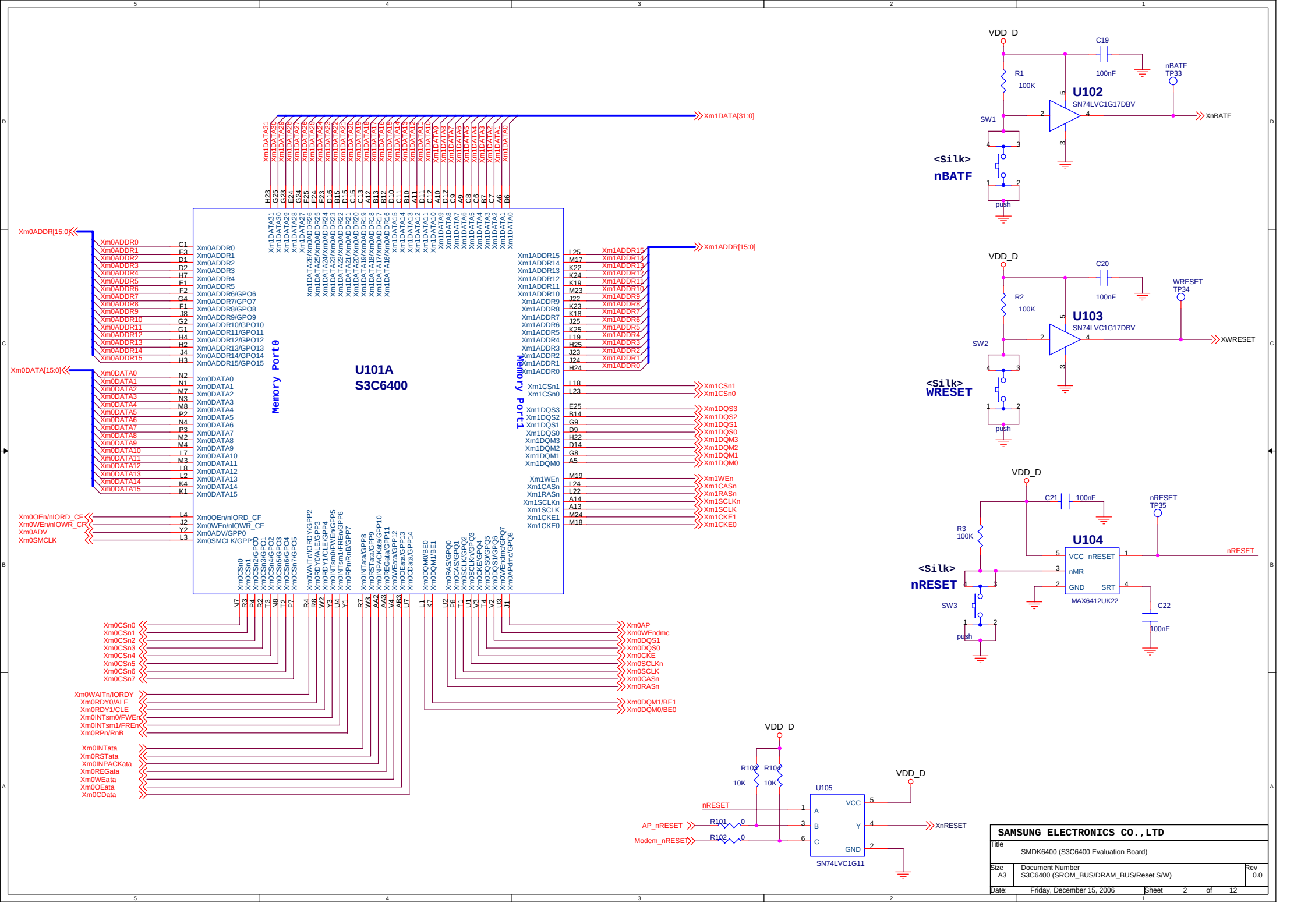
Base Board

00	Board to Board Connector (Base)
01	NOR/SRAM/NAND/Config
02	CF+
03	CF+/Ext. Bus/Modem I/F
04	Ethernet Controller
05	LCD:RGB 24bpp_320X240
06	LCD:RGB CPU18bpp_RGB666_240x320
07	LCD:7inch
08	Camera IF/I2C
09	Audio(AC97/PCM)
0A	Audio(IIS)
0B	UART/IrDA/SPI
0C	Keypad
0D	HSMMC/TV
0E	Base B'd Power

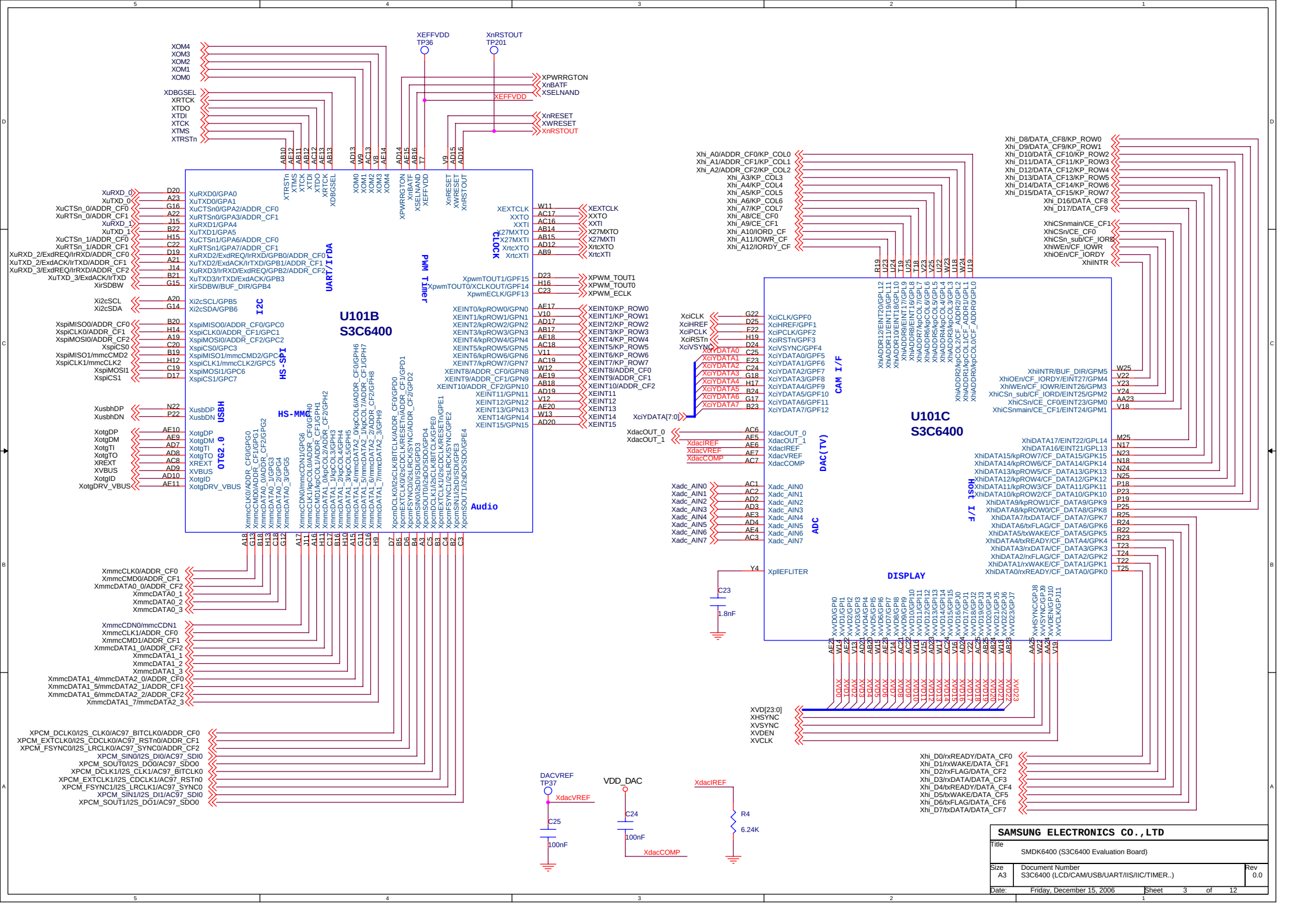
3. Part Reference

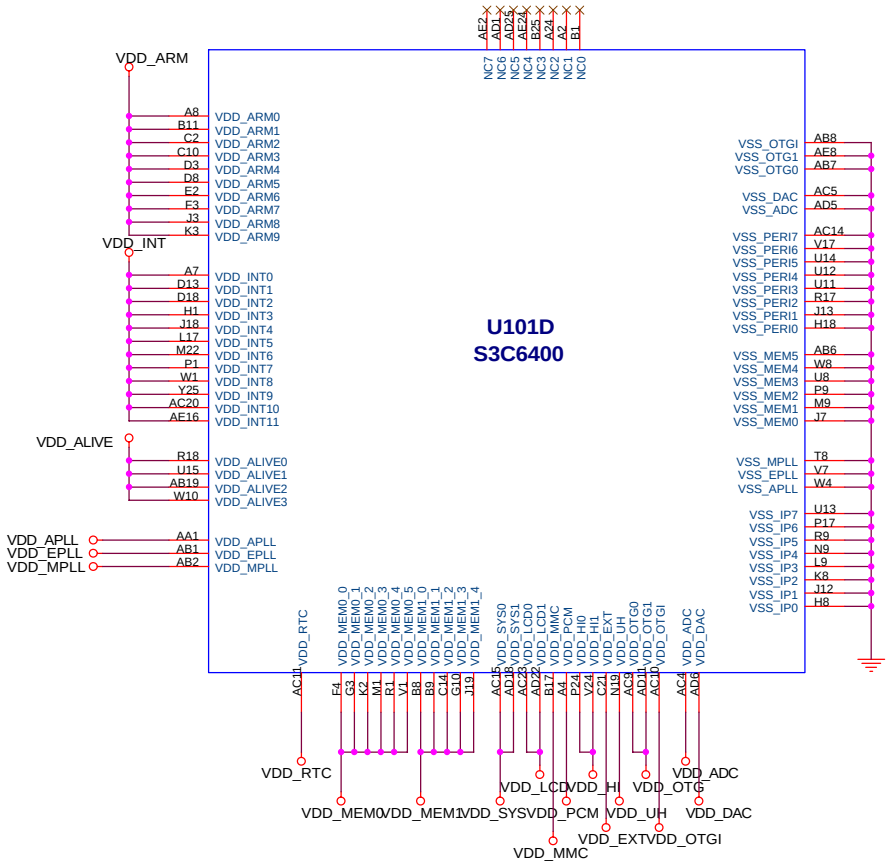
<Component><Number>

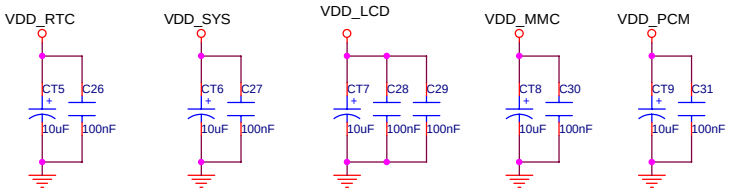
- U - COMPONENT IC & REGURATOR IC
- C - CAPACITOR
- CT- TANTAL CAPACITOR
- R - RESISTER
- RP - RESISTOR PACK
- VR - VARIABLE RESISTER
- J - JUMPER
- L - INDUCTOR
- F - FERRITE BEAD
- Y - OSCILLATOR
- X - CRYSTAL
- Q - TRANSISTOR/FET
- D - DIODE
- SW - TACT/PUSH SWITCH
- CON - CONNECTOR
- CFG - DIP SWITCH

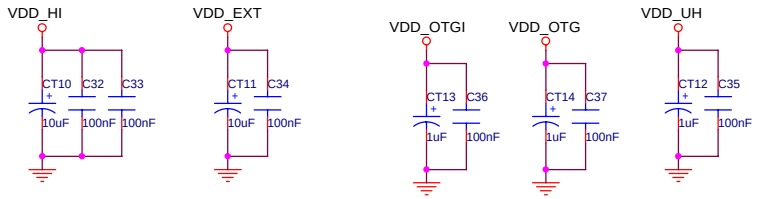


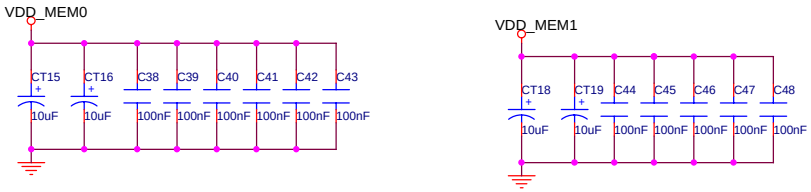
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK6400 (S3C6400 Evaluation Board)		
Size: A3	Document Number: S3C6400 (SROM_BUS/DRAM_BUS/Reset S/W)	Rev: 0.0
Date: Friday, December 15, 2006	Sheet 2 of 12	

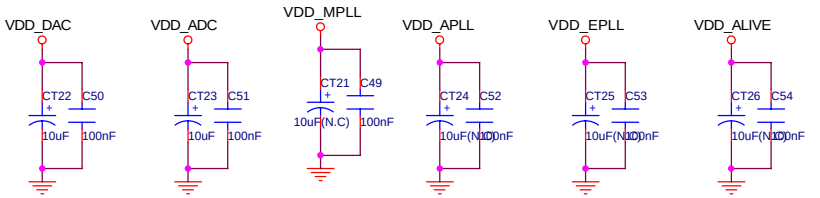

U101B
S3C6400
U101C
S3C6400
I2C
UART/IrDA
PWM Timer
CLOCK
HS-SPI
HS-MMC
USBH
OTG2.0
Audio
CAM I/F
DAC(TV)
ADC
HOST I/F
DISPLAY
XEFFVDD
TP36
XnRSTOUT
TP201
DACVREF
TP37
VDD_DAC
C23
1.8nF
C25
100nF
C24
100nF
R4
6.24K
XdacVREF
XdacCOMP
XdacIREF
SAMSUNG ELECTRONICS CO.,LTD
SMDK6400 (S3C6400 Evaluation Board)
S3C6400 (LCD/CAM/USB/UART/IIS/IIC/TIMER..)
Friday, December 15, 2006
Sheet 3 of 12

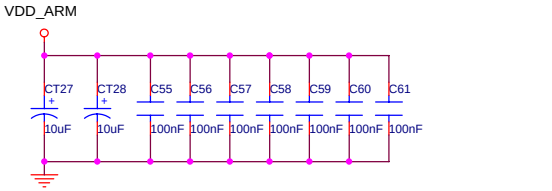


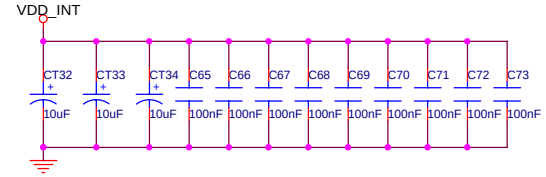




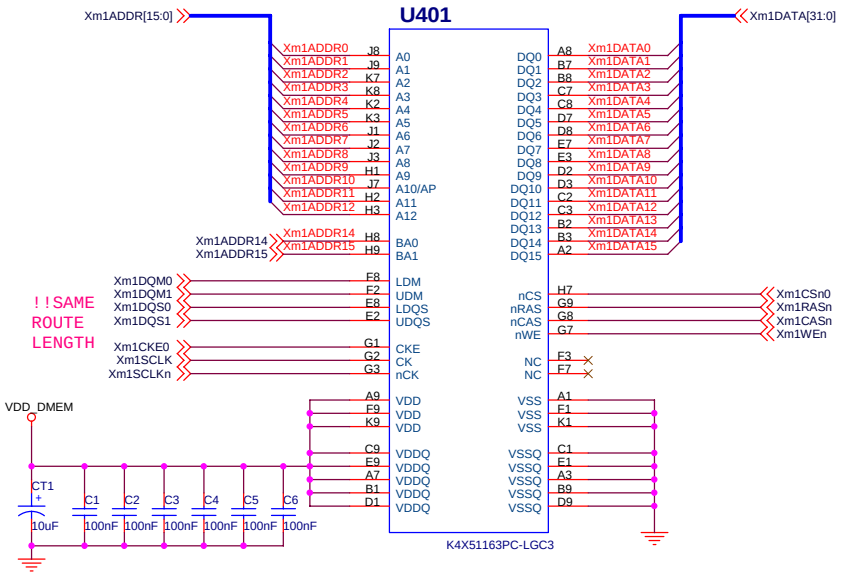


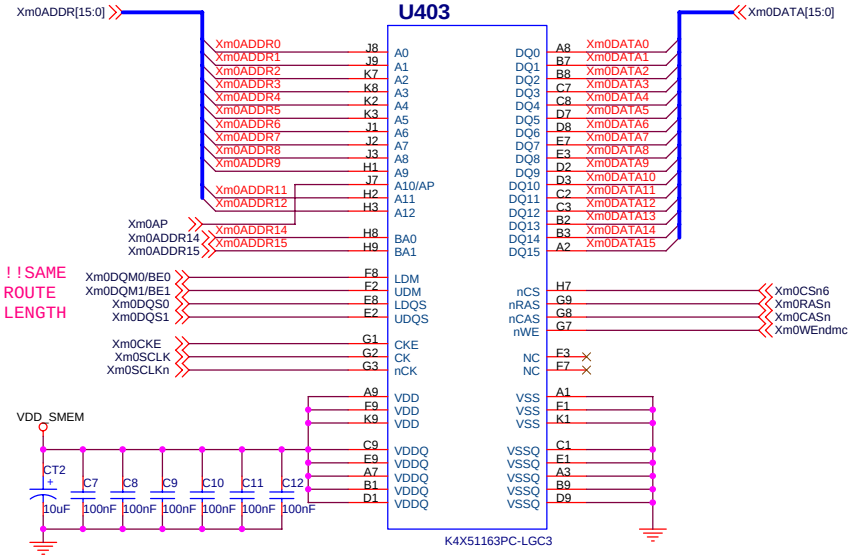


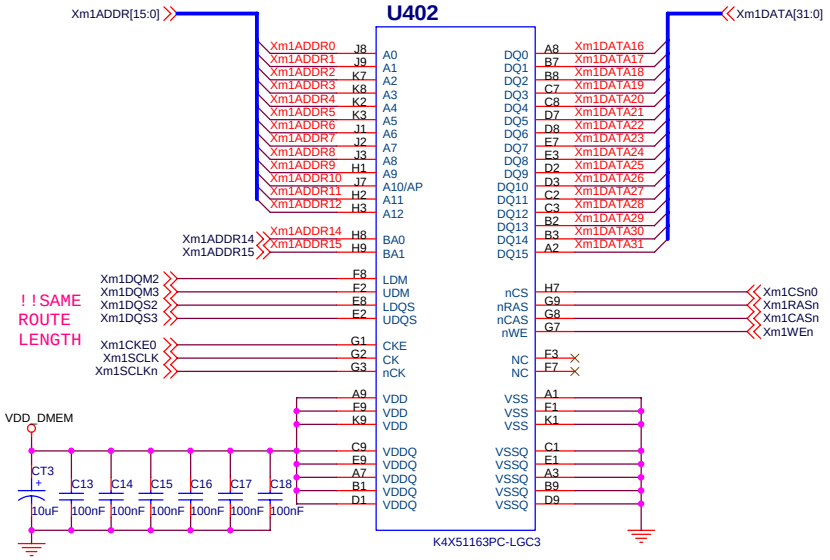




SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK6400 (S3C6400 Evaluation Board)		
Size: A3	Document Number: S3C2443 (POWER)	Rev: 0.0
Date: Friday, December 15, 2006	Sheet 4 of 12	







Just Only PADS on Lines

Xm1ADDR0	TP1	M1A0	Xm0ADDR0	TP2	M0A0
Xm1DATA0	TP3	M1D0	Xm0DATA0	TP4	M0D0
Xm1CKE0	TP5	M1CKE0	Xm0CKE	TP6	M0CKE0
Xm1CKE1	TP7	M1CKE1	Xm0SCLK	TP8	M0SCLK
Xm1SCLK	TP9	M1SCLK	Xm0SCLKn	TP10	M0SCLKn
Xm1SCLKn	TP11	M1SCLKn	Xm0WEndmc	TP12	M0WEn
Xm1WEn	TP13	M1WEn	Xm0CASn	TP14	M0CASn
Xm1CASn	TP15	M1CASn	Xm0RASn	TP16	M0RASn
Xm1RASn	TP17	M1RASn	Xm0DQM0/BE0	TP18	M0DQM0
Xm1DQM0	TP19	M1DQM0	Xm0DQM1/BE1	TP20	M0DQM1
Xm1DQM1	TP21	M1DQM1	Xm0DQS0	TP22	M0DQS0
Xm1DQM2	TP23	M1DQM2	Xm0DQS1	TP24	M0DQS1
Xm1DQM3	TP25	M1DQM3	Xm0AP	TP26	M0AP
Xm1DQS0	TP27	M1DQS0	Xm0CSn7	TP28	M0CSn7
Xm1DQS1	TP29	M1DQS1	Xm0ADDR10	TP102	Xm0A10
Xm1DQS2	TP30	M1DQS2			
Xm1DQS3	TP31	M1DQS3			
Xm1CSn1	TP32	M1CSn1			
Xm1ADDR13	TP103	Xm1A13			

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK6400 (S3C6400 Evaluation Board)		
Size: A3	Document Number: mDDR (Memory Port1 / Memory Port 0)	Rev: 0.0
Date: Friday, December 15, 2006	Sheet 5 of 12	

CFG0						
Booting Mode	[6]	[5]	[4]	[3]	[2]	[1]
NAND, 512/3 cycle	1	0	0	0	0	ON : EXTCLK
NAND, 512/4 cycle	1	0	0	0	1	
ANAND, 2K/4 cycle	1	0	0	1	0	
ANAND, 2K/5 cycle	1	0	0	1	1	
NOR/SROM	x	0	1	0	0:8bit 1:16bit	
OneNAND	0	0	1	1	0	OFF :XTI
Modem	x	0	1	1	1	
Internal ROM	x	1	1	1	1	

12.14繕無 熱薑 脾

CFG1 [1]	OneNANDC Select
[1]: OFF	ONDC0 (nCS2)
[1]: ON	ONDC1 (nCS3)

IN: L => D <-> *S2
H => D <->
*S1

IN: "H" => ON

QTH/QSH Series (0.5mm)

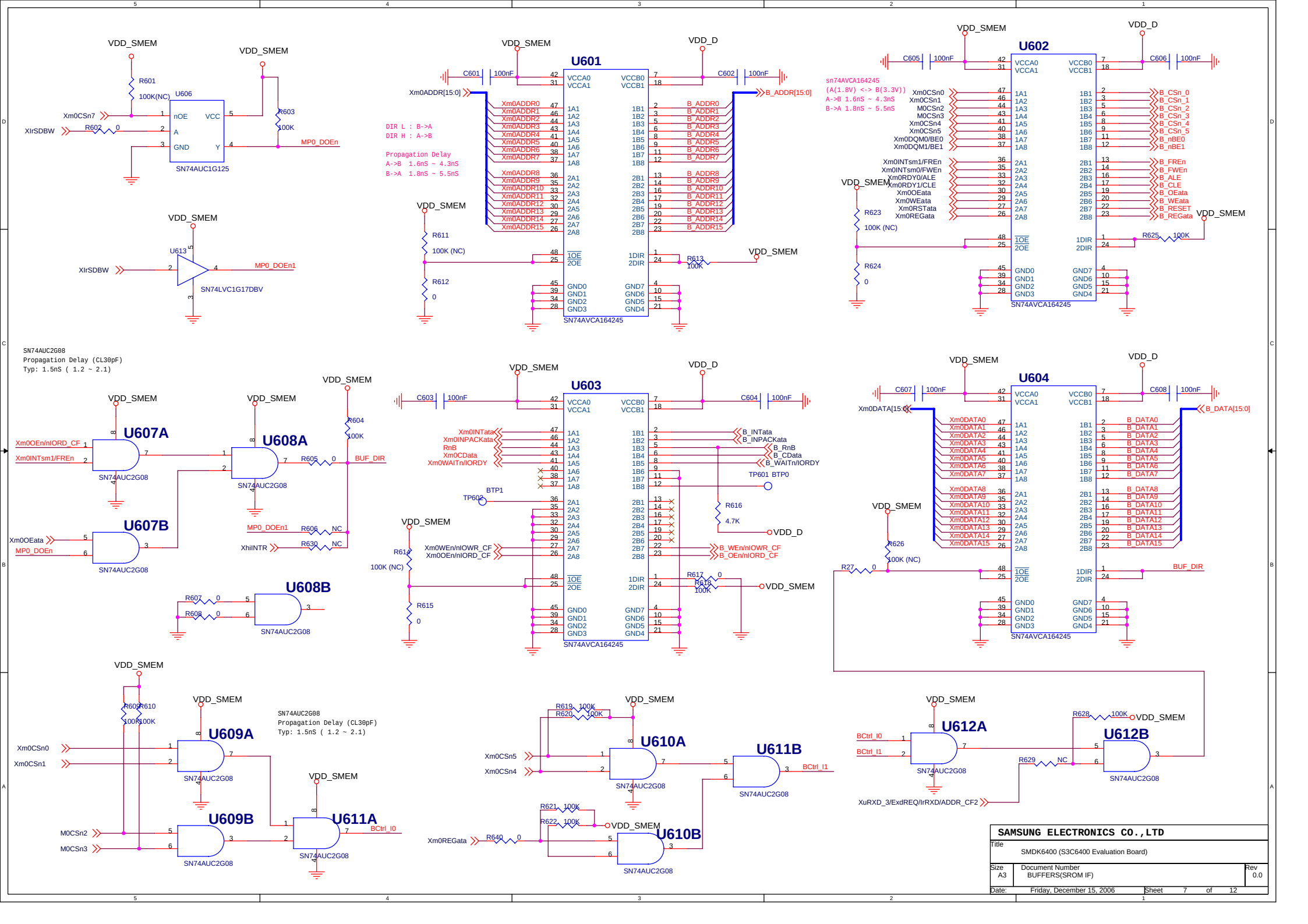
Clocks

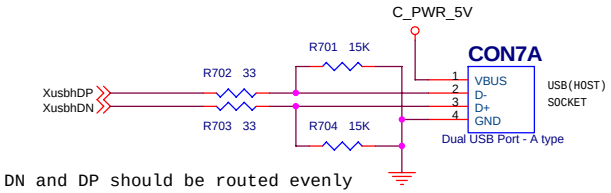
SAMSUNG ELECTRONICS CO.,LTD

Title: SMDK6400 (S3C6400 Evaluation Board)

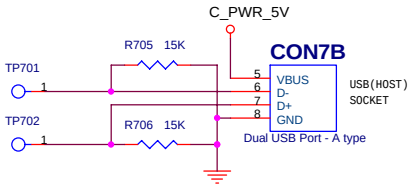
Size: A3 | Document Number: MEMORY(OneNAND)/JTAG/CLK | Rev: 0.0

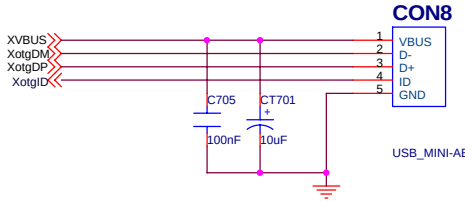
Date: Friday, December 15, 2006 | Sheet 6 of 12

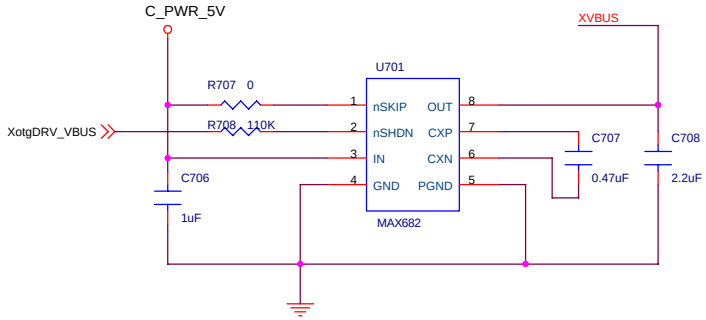

VDD_SMEM
R601
100K(NC)
U606
Xm0CSn7
XIrSDBW
R602
nOE
A
GND
VCC
Y
R603
100K
MP0_DOEn
SN74AUC1G125
U613
MP0_DOEn1
SN74LVC1G17DBV
U601
VDD_D
C601
C602
100nF
Xm0ADDR[15:0]
B_ADDR[15:0]
DIR L : B->A
DIR H : A->B
Propagation Delay
A->B 1.6nS ~ 4.3nS
B->A 1.8nS ~ 5.5nS
R611
R612
R613
SN74AVCA164245
U602
sn74AVCA164245
(A(1.8V) <-> B(3.3V))
A->B 1.6nS ~ 4.3nS
B->A 1.8nS ~ 5.5nS
R623
R624
R625
B_CSn_0
B_CSn_1
B_CSn_2
B_CSn_3
B_CSn_4
B_CSn_5
B_nBE0
B_nBE1
B_FREn
B_FWEn
B_ALE
B_CLE
B_OEata
B_WEata
B_RESET
B_REGata
SN74AUC2G08
Propagation Delay (CL30pF)
Typ: 1.5nS (1.2 ~ 2.1)
U607A
U607B
U608A
U608B
Xm0OEn/nIORD_CF
Xm0INTsm1/FREn
Xm0OEata
MP0_DOEn
MP0_DOEn1
XhiINTR
R604
R605
R606
R630
R607
R608
BUF_DIR
NC
U603
C603
C604
Xm0INTata
Xm0INPACKata
RnB
Xm0CData
Xm0WAITn/IORDY
B_INTata
B_INPACKata
B_RnB
B_CData
B_WAITn/IORDY
TP601 BTP0
TP602
BTP1
R616
4.7K
Xm0WEn/nIOWR_CF
Xm0OEn/nIORD_CF
B_WEn/nIOWR_CF
B_OEn/nIORD_CF
R614
R615
R617
R618
U604
C607
C608
Xm0DATA[15:0]
B_DATA[15:0]
R626
R27
U609A
U609B
U611A
Xm0CSn0
Xm0CSn1
M0CSn2
M0CSn3
R609
R610
BCtrl_I0
U610A
U610B
U611B
Xm0CSn5
Xm0CSn4
Xm0REGata
R619
R620
R621
R622
R640
BCtrl_I1
U612A
U612B
BCtrl_I0
BCtrl_I1
R628
R629
XuRXD_3/ExdREQ/IrRXD/ADDR_CF2
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK6400 (S3C6400 Evaluation Board)
Size
A3
Document Number
BUFFERS(SROM IF)
Rev
0.0
Date:
Friday, December 15, 2006
Sheet
7
of
12



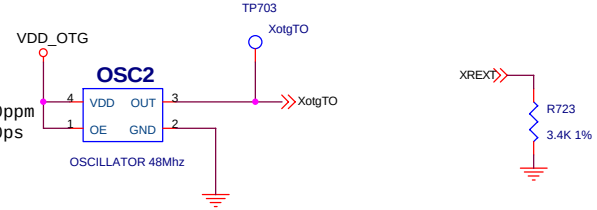
DN and DP should be routed evenly





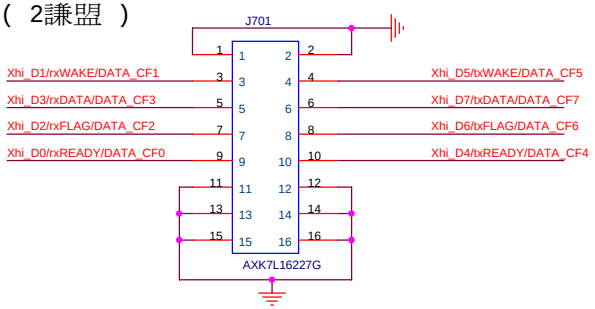


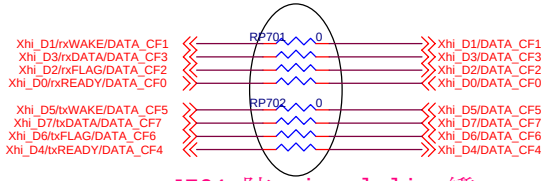
fundermental
Oscillator
tolerance +-100ppm
peak jitter 100ps
duty cycle
40/60~60/40
swing 3.3V



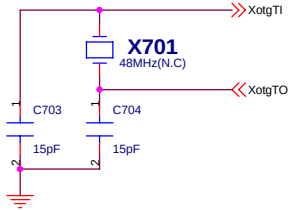
For USB Clock

FPC Cable 薯濛 (2謙盟)

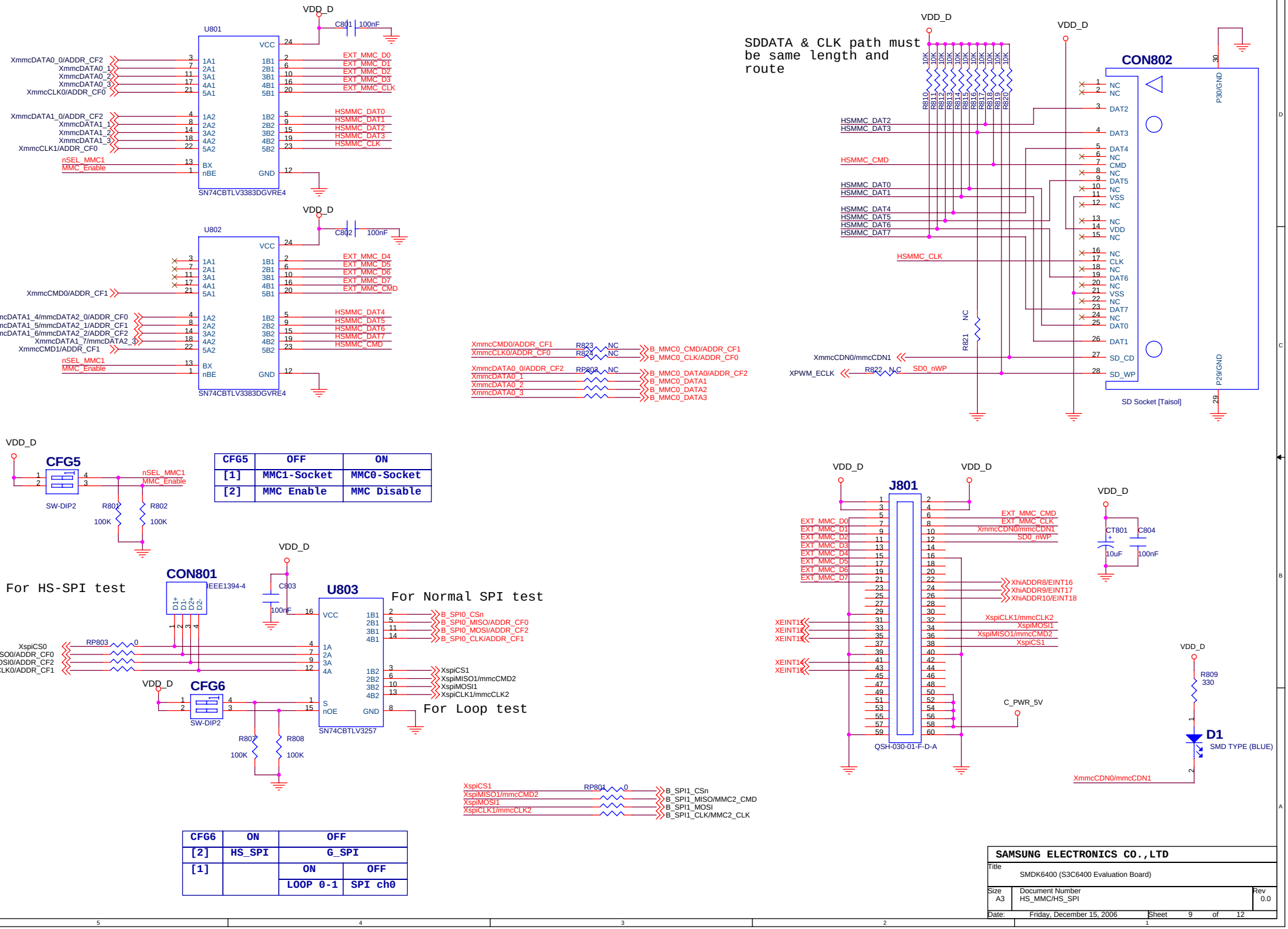




J701 陝 signal line縑
譆渠 陛梱檜 寡纂



SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK6400 (S3C6400 Evaluation Board)		
Size: A3	Document Number: USB/USB OTG/MIPI	Rev: 0.0
Date: Friday, December 15, 2006	Sheet 8 of 12	


U801
SN74CBTLV3383DGVRE4
U802
SN74CBTLV3383DGVRE4
C801 100nF
C802 100nF
VDD_D
XmmcDATA0_0/ADDR_CF2
XmmcDATA0_1
XmmcDATA0_2
XmmcDATA0_3
XmmcCLK0/ADDR_CF0
XmmcDATA1_0/ADDR_CF2
XmmcDATA1_1
XmmcDATA1_2
XmmcDATA1_3
XmmcCLK1/ADDR_CF0
nSEL_MMC1
MMC_Enable
EXT_MMC_D0
EXT_MMC_D1
EXT_MMC_D2
EXT_MMC_D3
EXT_MMC_CLK
HSMMC_DAT0
HSMMC_DAT1
HSMMC_DAT2
HSMMC_DAT3
HSMMC_CLK
EXT_MMC_D4
EXT_MMC_D5
EXT_MMC_D6
EXT_MMC_D7
EXT_MMC_CMD
XmmcCMD0/ADDR_CF1
XmmcDATA1_4/mmcDATA2_0/ADDR_CF0
XmmcDATA1_5/mmcDATA2_1/ADDR_CF1
XmmcDATA1_6/mmcDATA2_2/ADDR_CF2
XmmcDATA1_7/mmcDATA2_3
XmmcCMD1/ADDR_CF1
HSMMC_DAT4
HSMMC_DAT5
HSMMC_DAT6
HSMMC_DAT7
HSMMC_CMD
SDDATA & CLK path must be same length and route
CON802
SD Socket [Taisol]
HSMMC_DAT2
HSMMC_DAT3
HSMMC_CMD
HSMMC_DAT0
HSMMC_DAT1
HSMMC_DAT4
HSMMC_DAT5
HSMMC_DAT6
HSMMC_DAT7
HSMMC_CLK
XmmcCDN0/mmcCDN1
XPWM_ECLK
SD0_nWP
SD_CD
SD_WP
P30/GND
P29/GND
CFG5
SW-DIP2
R801 100K
R802 100K
CFG5 OFF ON
[1] MMC1-Socket MMC0-Socket
[2] MMC Enable MMC Disable
XmmcCMD0/ADDR_CF1
XmmcCLK0/ADDR_CF0
B_MMC0_CMD/ADDR_CF1
B_MMC0_CLK/ADDR_CF0
XmmcDATA0_0/ADDR_CF2
XmmcDATA0_1
XmmcDATA0_2
XmmcDATA0_3
B_MMC0_DATA0/ADDR_CF2
B_MMC0_DATA1
B_MMC0_DATA2
B_MMC0_DATA3
J801
QSH-030-01-F-D-A
C_PWR_5V
CT801 10uF
C804 100nF
XhiADDR8/EINT16
XhiADDR9/EINT17
XhiADDR10/EINT18
XspiCLK1/mmcCLK2
XspiMOSI1
XspiMISO1/mmcCMD2
XspiCS1
XEINT11
XEINT12
XEINT13
XEINT14
XEINT15
R809 330
D1
SMD TYPE (BLUE)
For HS-SPI test
CON801
IEEE1394-4
C803 100nF
U803
SN74CBTLV3257
RP803
XspiCS0
XspiMISO0/ADDR_CF0
XspiMOSI0/ADDR_CF2
XspiCLK0/ADDR_CF1
For Normal SPI test
B_SPI0_CSn
B_SPI0_MISO/ADDR_CF0
B_SPI0_MOSI/ADDR_CF2
B_SPI0_CLK/ADDR_CF1
XspiCS1
XspiMISO1/mmcCMD2
XspiMOSI1
XspiCLK1/mmcCLK2
For Loop test
CFG6
SW-DIP2
R807 100K
R808 100K
CFG6 ON OFF
[2] HS_SPI G_SPI
[1] ON OFF
LOOP 0-1 SPI ch0
RP801
B_SPI1_CSn
B_SPI1_MISO/MMC2_CMD
B_SPI1_MOSI
B_SPI1_CLK/MMC2_CLK
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK6400 (S3C6400 Evaluation Board)
Size A3
Document Number HS_MMC/HS_SPI
Rev 0.0
Date: Friday, December 15, 2006
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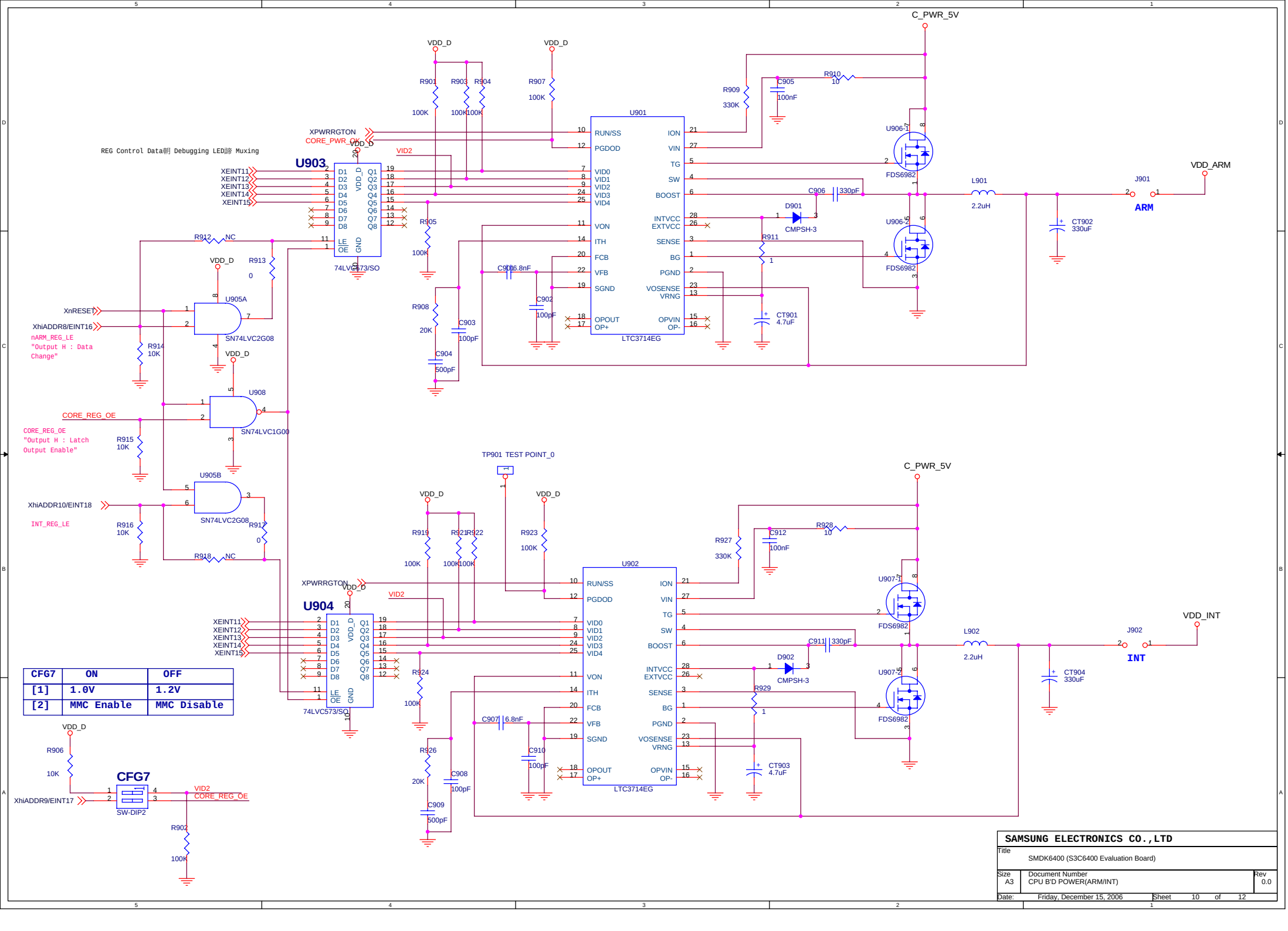
C_PWR_5V
VDD_D
U903
U901
XPWRRGTON
CORE_PWR_OK
VID2
REG Control Data해 Debugging LED諦 Muxing
XEINT11
XEINT12
XEINT13
XEINT14
XEINT15
74LVC573/SO
LTC3714EG
RUN/SS
PGDOD
VID0
VID1
VID2
VID3
VID4
VON
ITH
FCB
VFB
SGND
OPOUT
OP+
ION
VIN
TG
SW
BOOST
INTVCC
EXTVCC
SENSE
BG
PGND
VOSENSE
VRNG
OPVIN
OP-
R901
R903
R904
R907
R905
R908
R909
R910
R911
C905
C906
C901
C902
C903
C904
D901
CMPSH-3
U906-1
U906-2
FDS6982
L901
2.2uH
J901
ARM
VDD_ARM
CT901
4.7uF
CT902
330uF
R912
NC
R913
U905A
SN74LVC2G08
XnRESET
XhiADDR8/EINT16
nARM_REG_LE
"Output H : Data Change"
R914
U908
SN74LVC1G00
CORE_REG_OE
"Output H : Latch Output Enable"
R915
U905B
XhiADDR10/EINT18
INT_REG_LE
R916
R917
R918
TP901 TEST POINT_0
U902
U904
R919
R921
R922
R923
R924
R926
R927
R928
R929
C907
C908
C909
C910
C911
C912
D902
U907-1
U907-2
L902
J902
INT
VDD_INT
CT903
CT904
R906
CFG7
SW-DIP2
XhiADDR9/EINT17
R902
CFG7 | ON | OFF
[1] | 1.0V | 1.2V
[2] | MMC Enable | MMC Disable
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK6400 (S3C6400 Evaluation Board)
Size A3
Document Number
CPU B'D POWER(ARM/INT)
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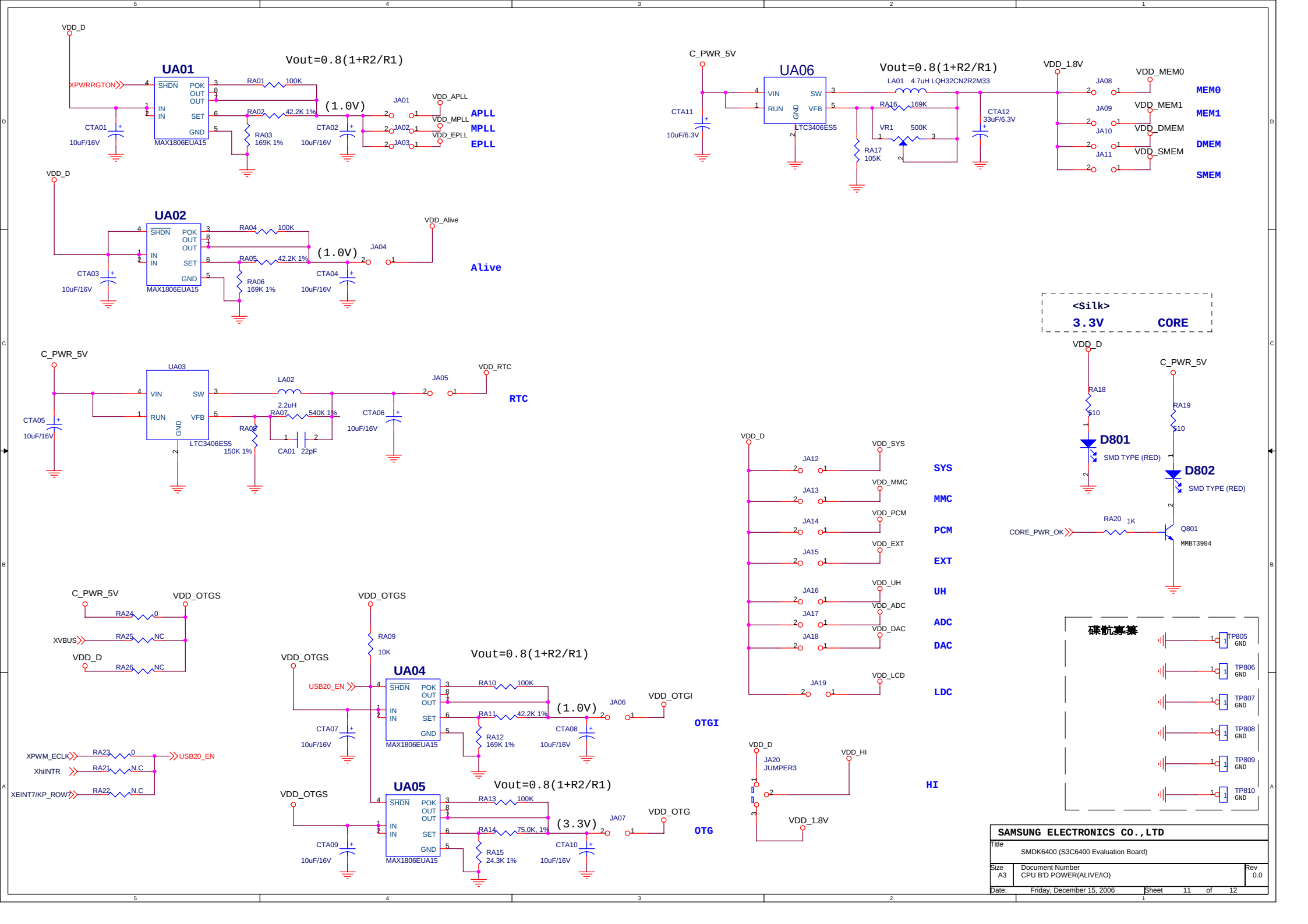
VDD_D
UA01
Vout=0.8(1+R2/R1)
XPWRRGTON
SHDN
POK
OUT
IN
SET
GND
MAX1806EUA15
RA01 100K
RA02 42.2K 1%
RA03 169K 1%
(1.0V)
CTA01 10uF/16V
CTA02 10uF/16V
JA01
JA02
JA03
VDD_APLL
VDD_MPLL
VDD_EPLL
APLL
MPLL
EPLL
VDD_D
UA02
RA04 100K
RA05 42.2K 1%
RA06 169K 1%
(1.0V)
CTA03 10uF/16V
CTA04 10uF/16V
JA04
VDD_Alive
Alive
C_PWR_5V
UA03
VIN
SW
RUN
VFB
GND
LTC3406ES5
LA02 2.2uH
RA07 540K 1%
RA08 150K 1%
CA01 22pF
CTA05 10uF/16V
CTA06 10uF/16V
JA05
VDD_RTC
RTC
C_PWR_5V
UA06
Vout=0.8(1+R2/R1)
LA01 4.7uH LQH32CN2R2M33
RA16 169K
VR1 500K
RA17 105K
CTA11 10uF/6.3V
CTA12 33uF/6.3V
LTC3406ES5
VDD_1.8V
JA08
JA09
JA10
JA11
VDD_MEM0
VDD_MEM1
VDD_DMEM
VDD_SMEM
MEM0
MEM1
DMEM
SMEM
<Silk>
3.3V
CORE
VDD_D
C_PWR_5V
RA18 510
RA19 510
D801
SMD TYPE (RED)
D802
SMD TYPE (RED)
RA20 1K
CORE_PWR_OK
Q801
MMBT3904
VDD_D
JA12
JA13
JA14
JA15
JA16
JA17
JA18
JA19
VDD_SYS
VDD_MMC
VDD_PCM
VDD_EXT
VDD_UH
VDD_ADC
VDD_DAC
VDD_LCD
SYS
MMC
PCM
EXT
UH
ADC
DAC
LDC
C_PWR_5V
VDD_OTGS
RA24 0
RA25 NC
RA26 NC
XVBUS
VDD_D
XPWM_ECLK
XhilNTR
XEINT7/KP_ROW7
RA23 0
RA21 N.C
RA22 N.C
USB20_EN
VDD_OTGS
RA09 10K
UA04
Vout=0.8(1+R2/R1)
USB20_EN
SHDN
POK
OUT
IN
SET
GND
MAX1806EUA15
RA10 100K
RA11 42.2K 1%
RA12 169K 1%
(1.0V)
CTA07 10uF/16V
CTA08 10uF/16V
JA06
VDD_OTGI
OTGI
VDD_OTGS
UA05
Vout=0.8(1+R2/R1)
RA13 100K
RA14 75.0K 1%
RA15 24.3K 1%
(3.3V)
CTA09 10uF/16V
CTA10 10uF/16V
JA07
VDD_OTG
OTG
VDD_D
JA20
JUMPER3
VDD_HI
VDD_1.8V
HI
碟骯寡纂
TP805 GND
TP806 GND
TP807 GND
TP808 GND
TP809 GND
TP810 GND
SAMSUNG ELECTRONICS CO.,LTD
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SMDK6400 (S3C6400 Evaluation Board)
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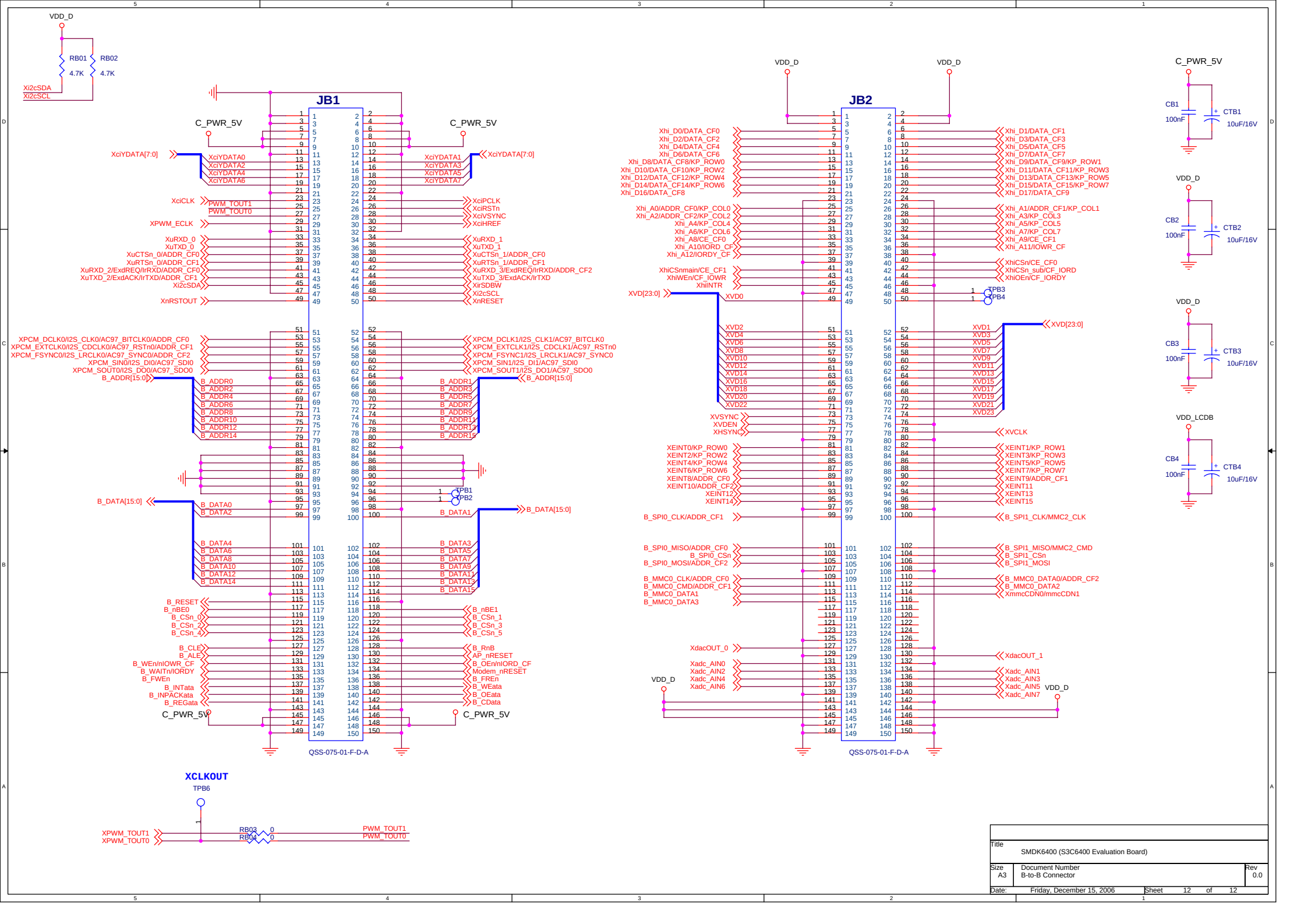

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