FAIRCHILD SEMICONDUCTOR™

March 2002
Revised March 2002

Section 6 - Noise, Cross-talk, Jitter, Skew, and EMI Backplane Designer's Guide

This section discusses backplane signal integrity, focusing on the phenomena and effects that can disrupt clean signals and high signal integrity. Enemies of signal integrity include noise, cross-talk, jitter, skew, and electromagnetic interference (EMI).

All electronic systems contain some elements of these phenomena. The key to designing for high signal integrity is the reduction of these phenomena below levels that will adversely affect signal quality. This discussion will focus on what causes these phenomena, and what can be done during system design to reduce or eliminate the causes.

As backplane frequencies increase, the effects of these phenomena become more pronounced. This, in turn, requires tighter control of layout and design to minimize detrimental effects on signal integrity. The result is an ever-tightening spiral that creates a battle between the backplane designer and the phenomena that can ruin signal integrity.

Poor signal integrity will limit backplane speed and adversely affect system reliability. Conversely, achieving a high level of signal integrity within the constraints of the design will result in a high-performing, reliable backplane design.

Section Reference

This section presents information covering:

- Noise (Ground Bounce, Ringing, and Reflections)
- Signal Cross-talk
- Jitter
- Skew
- Electromagnetic Interference (EMI)

Section	Section Title	Contents
1	Introduction	Application demands, basic backplane considerations, and how to use this guide.
2	Backplane Protocols	Descriptions of different backplane bus protocols, including PCI- and VME-based protocols.
3	Backplane Architecture	Topics relevant to backplane configuration, including parallel versus serial configuration and different configuration topologies and timing architectures
4	Backplane Design Considerations	Issues relevant to backplane layout, including distributed capacitance, transmission line effect, stub length, termination, and throughput.
5	Backplane Signal Driving and Conditioning	Signal driving and conditioning, including power consumption, rise/fall time, propagation delay, flight time, device drive, pin conditioning, live insertion, and incident wave switching.
6	**Noise, Cross-talk, Jitter, Skew and EMI**	**A review of the enemies of signal integrity and high frequency.**
7	Transceiver Technologies	Detailed information about the following technologies: TTL-based (ABT, FCT, and LVT); ECL; and GTLP.
8	Mechanical Considerations	Information about mechanical considerations such as backplane chassis/cages and connectors.
9	Layout Considerations	Physical layout of the receiver and driver cards plugged into the backplane, primarily focusing on construction of the physical layer and the configuration of the devices that comprise the cards.

Noise

Many factors generate noise in a system. The most significant noise-generating factors are ringing, cross-talk, and EMI. Ringing is the oscillations of the signal level after a state change. It is caused by three sources: device switching noise, system switching noise, and transmission line reflections.

Noise of all types has the single largest effect on system-signal integrity. Large amounts of noise will change the shape of signal edges, change edge placement in time, and induce voltage spikes and voltage droops (a voltage droop is defined as a momentary reduction of the voltage level) onto static signals. These voltage transients affect how the receivers sense the input signal.

A change to signal edges affects the shape of the edge and the time at which the edge arrives at the receiver. If voltage transients cross device threshold levels, the receiver will change states. The results are data corruption, and, if the problem is serious enough, system failure.

High levels of noise cause a significant reduction in system reliability, speed, and overall performance. The system designer can make choices that will control and limit noise.

The I/O technology selection has a significant impact on noise and overall system performance, because the amount of noise a system can tolerate is directly proportional to the noise tolerance of the I/O technology.

Device-Switching Noise

Device-switching noise can add significantly to a system's noise level. By ensuring the best fit of I/O technology to system design needs, as well as proper layout, a backplane designer can control the detrimental effects of device-switching noise.

I/O technologies contribute to system noise in the forms of ground bounce and dynamic threshold shift. How well a technology rejects these and other noise transients is the I/O's noise rejection, which is measured as noise margin.

Noise Margin

Noise margin is the amount of input noise a device can tolerate and still maintain the integrity of the logic levels. It can be quantified by measuring input threshold levels. These levels are usually specified in the databook as Voltage Input High Level (V_{IH}) and Voltage Input Low Level (V_{IL}). The ratings specify at what voltage level the input gate will change state.

In digital systems, one device output gate usually drives another device input gate. For example, an output gate whose voltage output is HIGH (V_{OH}) will drive an input gate to a high state when the input reaches its V_{IH} threshold level. The difference between the two, V_{OH} - V_{IH}, represents the noise margin. The equation for voltage high noise margin is:

$NM_H = V_{OH} - V_{IH}$

Where:

NM_H = High Noise Margin Voltage

V_{OH} = Output High Voltage

V_{IH} = Input High Voltage

The equation for voltage low noise margin is:

$NM_L = V_{OL} - V_{IL}$

Where:

NM_L = Low Noise Margin Voltage

V_{OL} = Output Low Voltage

V_{IL} = Input Low Voltage

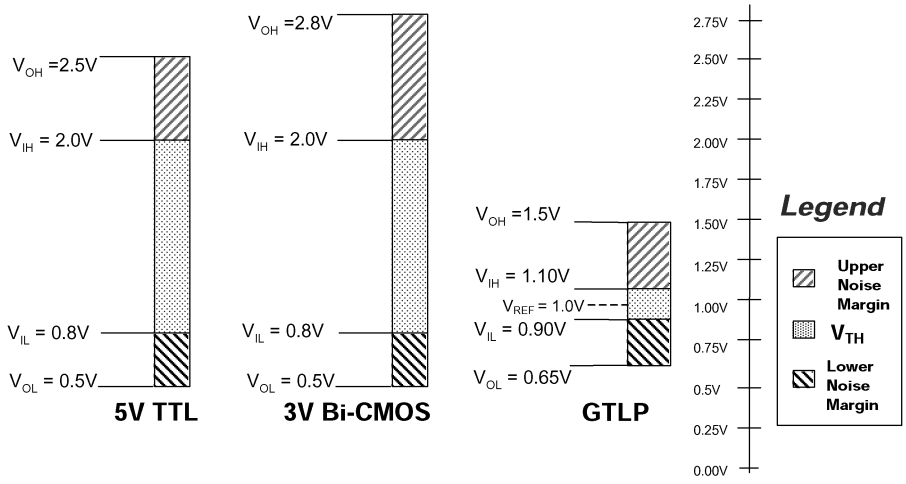


FIGURE 1. Typical Noise Margins for Single End Signal Backplane Technologies

Figure 1 illustrates noise margins for several backplane technologies showing typical V_{IHL} and V_{OHL} performance and noise margins. As an example, GTLP has a V_{IL} of 0.90V and input V_{OL} of 0.65V and the noise margin is 0.35V. A voltage LOW-to-HIGH noise transient would need to rise above 0.90V to place the input in jeopardy of switching states.

Noise (Continued)

It is notable that noise margins for most technologies are smaller for the V_{OL} to V_{IL} condition. This makes noise in the lower voltage portion of the signal range a potentially more significant problem that requires tighter control than is necessary for noise at the upper end of the signal level.

Most single-ended technologies have a fixed Voltage Reference level (V_{REF}). For example, CMOS devices typically have a V_{REF} that is 0.5 * V_{CC} (or $V_{CC}/2$).

GTLP's adjustable V_{REF} gives it an additional advantage over most single-ended technologies. The GTLP V_{REF} level is typically set between 0.7V and 1.3V and this allows the system designer to adjust the device threshold to a maximize noise margin for a specific application.

Differential technologies do not have the noise margin concerns of single-ended technologies. This is due to common mode rejection, which is the ability of the input to reject noise that appears coincident on both inputs. Although differential technologies are much better at rejecting input noise, they are not immune. Excessive noise is still an issue and can cause severe problems including edge delays and distortion.

Ground Bounce

Ground bounce of a digital electronic device is a measure of how the on-chip ground levels shift under dynamic switching conditions. The I/C package leads are seen as inductive elements during dynamic switching. Figure 2 illustrates a simplified model of a CMOS device in a package. L_1 represents the inductance of the ground lead, L_2 represents the V_{CC} lead, and L_3 the output lead. R_1 represents the impedance of the output structure during a discharge of the load. C_L and R_L represent the output load.

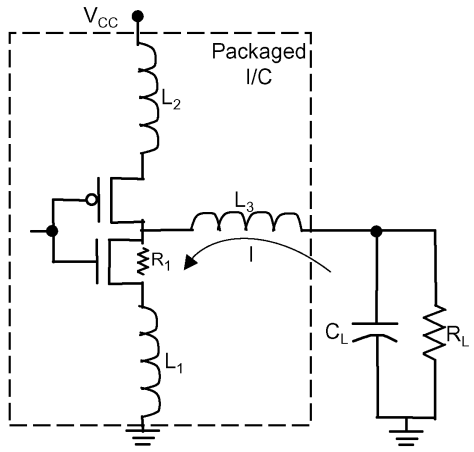


FIGURE 2. Package I/C Output Mode

To change the output load from HIGH-to-LOW, current flows through the output structure to discharge the load capacitance. As the current changes, voltage is generated across the inductances of the circuit. The formula for voltage across an inductor is:

$V_L = L\ (\Delta I/\Delta t)$

Where:

V_L = Generated Voltage

L = Inductance

ΔI = Change in Current

Δt = Change in Time

The inductance (L_1) between system ground and internal device ground induces a voltage. This induced voltage creates what is known as ground bounce. The voltage causes the device ground to be at a different level than system ground. This phenomenon appears as a device ground bounce above system ground level, followed by a swing below system ground before returning to parity with the system ground.

This same phenomenon occurs on the V_{CC} rail. This is the inverse of ground bounce and occurs when the device drives the load from LOW-to-HIGH.

The effects of ground bounce are seen both as output noise and as an internal shift of the input threshold region of the device. Both the output noise and the input threshold shift of a device can greatly reduce the effective usable noise margin on the bus.

In an extreme case, ground bounce can cause the false triggering of the switching device due to its moving internal threshold. It can also cause false triggering of a receiver device due to the output noise generated by the driver. The result of this can be unwanted bit errors.

Ground bounce is usually specified as V_{OLP} (peak level above the device static V_{OL}) and V_{OLV} (valley or lowest value of the shift below V_{OL}). Ground bounce phenomena are affected by several contributing factors: the number of outputs switching, output edge rate, the location of the output pin, the V_{CC} voltage, the load type and location, and the device technology.

The number of output pins switching in the same direction coincident with one another will affect the amplitude of the ground bounce pulse. Each output can be considered a resistive and inductive path in parallel with other outputs. As the number of output switching increases, the total effective resistance goes down. This generates more ground bounce.

Sharper output edge rates create a larger induced voltage across the inductive components in a shorter amount of time. This results in large amplitude of bounce.

The location of the output pin in relation to the ground and V_{CC} pins also affects ground bounce. The farther the output pin is from ground, the higher the ground bounce amplitude. Because of the bounce phenomenon, device manufactures have included a high number of ground and V_{CC} pins on high-drive and high-pin- count technologies

The V_{CC} voltage value affects the output voltage swing and the amount of current available. Both of these have a direct impact on ground bounce.

Load type and location also have a significant effect on ground bounce. A lumped capacitive load is a worst-case load for generating ground bounce. Conversely, a distributed load reacts as an impedance, and the resulting edge rate generates much lower ground bounce effects.

Noise (Continued)

The charging or discharging of a lumped load creates a much greater change in current flow over time ($\Delta I/\Delta t$) than the charging or discharging of a distributed load. This fact induces a much greater voltage across the ground or V_{CC} lead inductance.

Device technology and design play a large role in ground bounce generation. In simple terms, higher output drive devices generate steeper edge rates, and steeper edge rates generate more bounce. However, there are many mitigating factors.

Technology plays a large role in device edge rate. Pure CMOS devices, due to their design and behavior, turn on more quickly abruptly than equivalent bipolar devices. This abrupt delay results in more ground bounce for equivalent devices. Semiconductor vendors recognize this, and design in gradual turn-on (GTO®) circuits and edge rate control circuits to slow the edges and minimize bounce. BiCMOS designs combine some of the best features of bipolar and CMOS, including less bounce than most equivalent pure CMOS designs.

As mentioned earlier, the inclusion of multiple V_{CC} and ground pins helps minimize inductive lead effects. Some technologies such as GTLP take this a step further and include quiet grounds that separate the circuitry on the die and further quiet the device.

Dynamic Threshold

Dynamic threshold, the result of device ground bounce, is usually specified as Voltage Input Low Threshold Dynamic (V_{ILD}) and Voltage Input High Threshold Dynamic (V_{IHD}). As noted in the section on ground bounce, a shift in the device ground and V_{CC} also causes a shift in input threshold levels. Dynamic threshold problems arise when a dynamic input threshold crosses through the static input threshold level. This will cause the device to switch generating an unwanted change of state. Dynamic threshold problems usually occur only under the most severe circumstances, for example, when all outputs are switching simultaneously in the same direction into a lumped load.

Adequate grounding and decoupling can eliminate or minimize dynamic threshold and ground bounce effects.

System Switching Noise

The system power distribution network generates system noise. Current and voltage changes on ground and V_{CC} planes induce most of this noise. These changes are also seen on V_{CC} and ground traces and vias. These changes are created by the power demands of devices switching state.

High-speed and high-drive I/O technologies such as those used in backplanes require large amounts of current during switching. This is because large loads and high power terminations such as Thevenin and DC parallel designs require significant amounts of current. If the system power distribution network is not adequate for the current load, the voltage level on the supply planes can shift during switching. These voltage shifts are easily coupled throughout the system and are seen as voltage transients and ringing on the signals.

A transient voltage drop to a device V_{CC} also affects device noise margins adversely and reduces device output drive. These V_{CC} droops also cause device propagation delay to step out. As the V_{CC} level droops and recovers, the propagation time varies, inducing jitter.

A designer has more control over system-generated noise than over device-generated noise. System layout and design directly affect system switching noise levels.

Power Distribution

To minimize the effects of switching noise, adequate low-impedance ground and V_{CC} planes must be used. The layout and impedance of local supply traces and vias must be sufficient for current requirements. Local supply traces and vias should also be kept as short as possible. To further isolate and minimize switching noise, the separation of ground and supply planes for low- and high- speed sections of the system is recommended.

Decoupling

Local decoupling is also critical to eliminating voltage droops. Decoupling capacitors connected to the V_{CC} of devices will significantly reduce V_{CC} transients. These capacitors filter overshoots to ground and supply current to device V_{CC}s when the V_{CC} line voltage level droops.

The required capacitor values will vary with the system frequencies and the transients seen on the power planes. Use as many capacitors as needed to ensure adequate system decoupling, but a minimum of one decoupling capacitor for every device V_{CC} pin is recommended. In most applications, two decoupling capacitors are used to cover the frequency ranges of transients seen on the power rails. If possible, place the capacitors on the same side of the PCB as the device being decoupled, and minimize lead lengths between the decoupling capacitors and the device power pin.

Transmission Line Reflections

Transmission line reflection can be a major source of system noise. If transmission lines are left unterminated or are improperly terminated, the voltage level on the line will generate signal reflections, which, in turn, generate voltage overshoots and undershoots on the signal line. On an unterminated line, overshoots and undershoots can continue to propagate up and down the line repeatedly before settling to the quiescent voltage level.

Terminating transmission lines into their own impedance eliminates reflections. Section 4 of this Backplane Designer's Guide covers the subject of transmission lines and termination options.

Jitter

Jitter is movement of signal edges from their ideal position in time. This movement can lead or lag the ideal positions, and, as system speeds increase, these edge deviations present a significant problem for system signal integrity, causing skew, race conditions, and other timing problems.

Jitter is generally classified into three types: cycle-to-cycle jitter, period jitter, and phase jitter. The diagrams in Figure 3 illustrate these types. Cycle-to-cycle jitter is the change in an output's transition in time in relation to the transition during the previous cycle. Period jitter is the maximum change in a signal transition from the ideal position in time. Phase jitter, also called long-term jitter, in the maximum change in an output signal transition from its ideal position over many cycles (typically 10 to 20 microseconds).

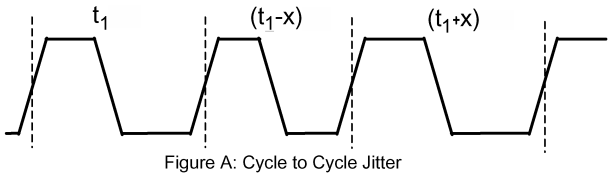


Figure A: Cycle to Cycle Jitter

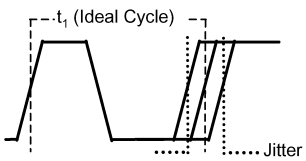


Figure B: Period Jitter

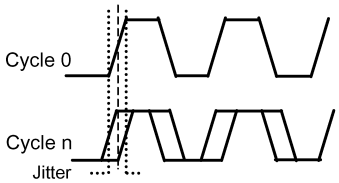


Figure C: Long Term Jitter

FIGURE 3. Three Types of Jitter

The causes of jitter are grouped into two general categories: deterministic jitter and random jitter. Deterministic jitter is caused by power supply fluctuations, cross-talk, and duty cycle distortion (e.g., asymmetric rising and falling edges). Random jitter is caused primarily by device thermal noise.

Although system designers have little control over the causes of random jitter, they can reduce the effects of deterministic jitter by minimizing cross-talk and duty cycle distortion and by ensuring the power network is adequate for system needs.

Cross-talk

Cross-talk is the capacitive and inductive coupling of signals from one signal line to another. As system performance and board densities increase, so does the problem of cross-talk. In the case of cross-talk, the line the signal is coupled from is usually referred to as the active (or aggressor) line, and the signal line the signals are coupled onto is called the passive (or victim) line.

The amplitude of the signal generated on the passive line is directly related to the edge rate of the signal on the active line, the proximity of the two lines, and distance that the two lines run adjacent to one another. Cross-talk noise can cause false switching by crossing the threshold regions of receivers on the passive line.

Cross-talk coupling generates two types of effects: forward cross-talk and reverse cross-talk.

Forward Cross-talk

Forward cross-talk is defined as the current coupled onto a passive line away from the active line driver, as shown in Figure 4. Forward cross-talk current is the result of capacitively coupled current (I_C) minus the inductively coupled current (I_L): I_C - I_L. This is due to the inductively coupled current traveling in the direction of the end of the passive line away from the active line driver (point D in Figure 4).

Forward cross-talk coupling occurs during the edge transitions on the active line and in opposite polarity. The pulse amplitude is a result of the difference in capacitive and inductive coupling.

Due to the short duration and small amplitude of forward cross-talk, the reflections of reverse cross-talk often hide this generally small pulse.

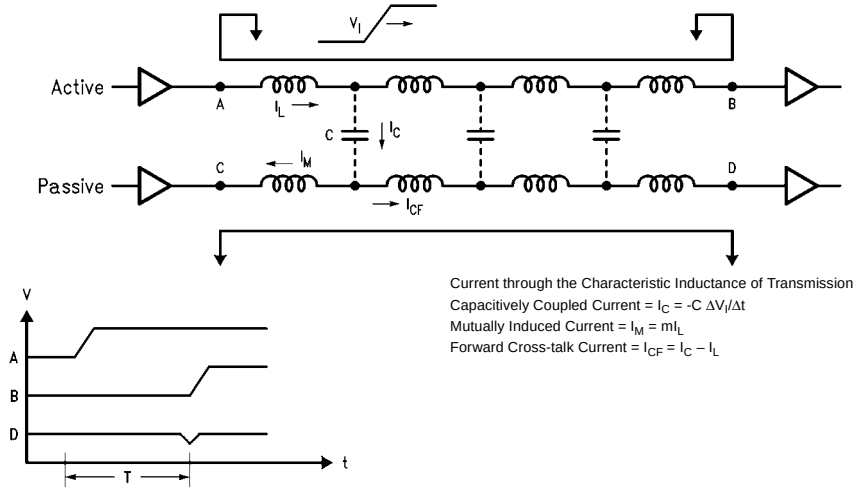


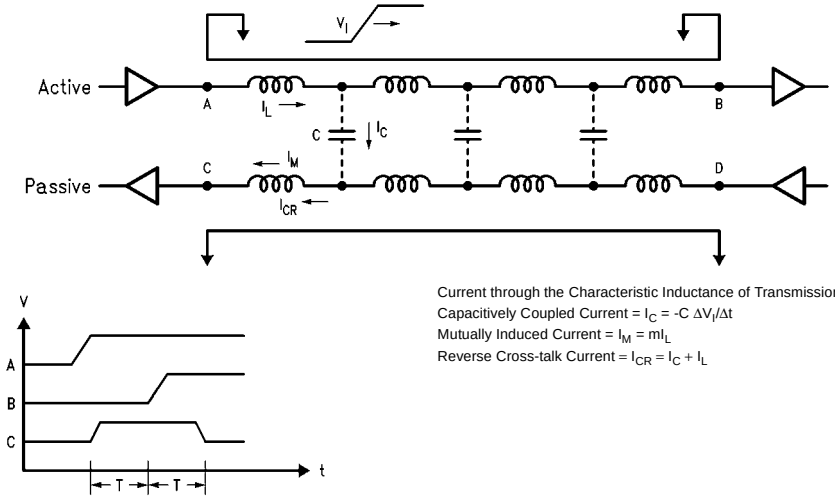
FIGURE 4. Illustration of forward cross-talk in a set of transmission lines between the driver and the receiver. As the active signal V_I propagates from A to B, a negative spike V_F propagates from C to D, coincident with V_I.

Cross-talk (Continued)

Reverse Cross-talk

Reverse cross-talk is defined as the current coupled onto a passive line toward the active line driver, as shown in Figure 5. Reverse cross-talk current is the result of capacitively coupled current (I_C) plus the inductively coupled current (I_L): $I_C + I_L$. This is due to the inductive coupling resulting in a transformer action.

Reverse cross-talk is directly proportional to line length and velocity of propagation on the line. Reverse cross-talk increases linearly with distance up to a certain length. This length is the distance that the signal can travel during its rise or fall time.



Current through the Characteristic Inductance of Transmission Line = I_L
Capacitively Coupled Current = $I_C = -C\ \Delta V_I/\Delta t$
Mutually Induced Current = $I_M = mI_L$
Reverse Cross-talk Current = $I_{CR} = I_C + I_L$

FIGURE 5. Reverse cross-talk in a set of transmission lines between the driver and the receiver. For reverse cross-talk, the active signal V_I propagates from A to B, while a positive pulse appears at C for a duration twice the coupled line delay T.

As illustrated in Figure 5, reverse cross-talk coupling starts at point C simultaneously with the beginning of the transition at point A. This coupling continues for the duration that the active line is switching. As the signal propagates down the active line to point B (t_B), the signal is coupled onto the passive line and toward point C. The reverse cross-talk then requires another flight time to reach point C. This makes the total reverse cross-talk waveform on the passive line twice the distance of the active line or $t_C = 2t_B$. Depending on the termination of the passive line, a reflection can be generated from the reverse cross-talk, and this reflection will propagate to D and, depending upon the amplitude and duration, back to C.

Minimizing Cross-talk

The use of tight geometry in most systems can reduce cross-talk significantly although it cannot eliminate it entirely. Some preventative design measures can be recommended to minimize cross-talk.

- Use maximum allowable spacing between signal lines.
- Minimize spacing between signal and ground lines.
- Isolate clocks and other critical signals from other lines (larger line spacing is recommended) or isolate with ground traces.
- In backplane or wire-wrap applications, use twisted pair for sensitive applications such as clocks and asynchronous set or clear functions.

  When using ribbon or flat cable, make every other line a ground line.
- Terminate signal lines into their characteristic impedance.

Skew

Skew is the variation of propagation delay differences between output signals. Minimizing output skew is a key design criterion in today's high-speed clocked systems. Excessive skew, especially for clock signals, can cause race conditions and other timing errors that result in system data faults. At the very least, poor skew will force a slower maximum system speed, and this, in turn, will limit system performance.

Matching trace lengths, trace impedances, and line loading will minimize system skew. Clock driving and I/O technology will also play a significant role in overall system skew.

Fairchild Semiconductor has developed skew specifications for interface devices. This section provides an overview of skew types, their definitions, and examples, as shown in Figure 6. Without skew specifications, a designer must approximate timing uncertainties. Skew specifications have been created to help clock designers define output propagation delay differences within a given device and duty cycle.

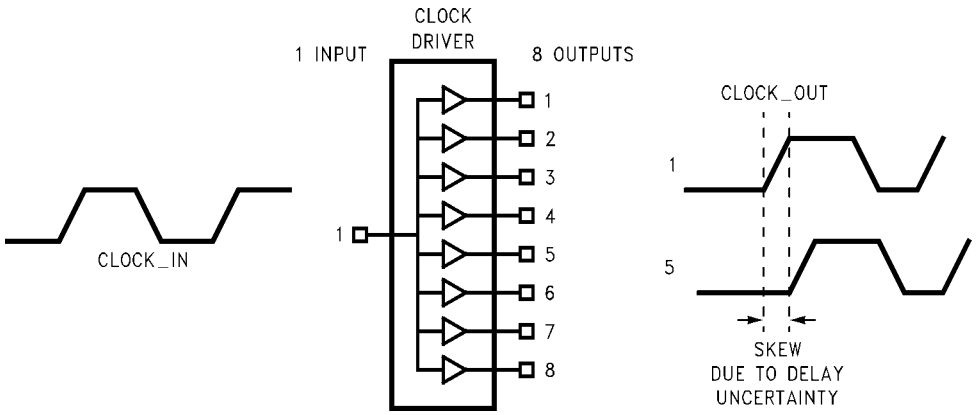


FIGURE 6. Clock driver showing output skew.
If a signal appears at output #1 in 3ns and at output #5 in 4ns, the skew is 1ns.

Sources of Clock Skew

Total system clock skew includes intrinsic and extrinsic skew. Intrinsic skew is defined as the differences in delays between the outputs of devices. Extrinsic skew is defined as the differences in trace delays and loading conditions. If the trace delays are poorly matched the result will be an increase in signal-to-signal skew.

A 50 MHz clock signal distribution on a PC board is given as an illustration of intrinsic and extrinsic skew. A frequency of 50 MHz with a 50% duty cycle produces 20ns clock cycles.

Total system skew budget = 10% of clock cycle = 2ns

If extrinsic skew = 1ns

Device skew (intrinsic skew) must be less than 1ns

Clock Duty Cycle

Clock duty cycle is a measure of the amount of time a signal is HIGH or LOW in a given clock cycle. Clock skew affects the duty cycle of a signal (duty cycle = t_{HIGH}/ t_{LOW} * 100%). As an example, in many systems, t_{HIGH} and t_{LOW} are each 50% of the clock cycle; therefore, the clock signal has a duty cycle of 50/50%. To ensure this requirement, skew must be guaranteed less than 1ns at 50 MHz to achieve 55/45% duty cycle requirements of core silicon.

Common Edge Skew (t_{OSLH}, t_{OSHL})

Device output skew is usually specified as output skew for HIGH-to-LOW transitions (t_{OSHL}) and output skew for LOW-to-HIGH transitions (t_{OSLH}). These parameters describe the delay from one driver to another on the same chip. This specification is the worst-case number of the delta between the fastest to the slowest path on the same chip. An example of this critical parameter is the case of the cache controller and the CPU, where both units use the same transition of the clock. In order for the CPU and the controller to be synchronized, t_{OSLH} and t_{OSHL} need to be minimized.

The output edge skew specifications are calculated by subtracting the specified propagation minimum (t_{PMIN}) from the propagation maximum (t_{PMAX}). Propagation delays are measured across all outputs of any single device.

Definition:

$t_{OSHL} = | t_{PHLMAX} - t_{PHLMIN} |$

Time of output edge skew edge HIGH-to-LOW = Time of propagation HIGH-to-LOW minimum minus time of propagation HIGH-to-LOW maximum

$t_{OSLH} = | t_{PLHMAX} - t_{PLHMIN} |$

Time of output edge skew edge LOW-to-HIGH = Time of propagation LOW-to-HIGH minimum minus time of propagation LOW-to-HIGH maximum

Pin Skew or Transition Skew

Pin Skew or Transition Skew (t_{PS}) describes opposite edge skews, i.e., the difference between the delay of the LOW-to-HIGH transition and the HIGH-to-LOW transition on the same pin.

Skew (Continued)

Pin Skew is measured across all the outputs (drivers) on the same device. The worst (largest delta) number is the guaranteed specification. Ideally, this number should be 0ns. Effectively, 0ns means that there is no degradation of the input signal's duty cycle.

Many of today's microprocessors require a minimum of a 45/55% duty cycle. System clock designers typically achieve this in one of two ways. The first method is with a crystal oscillator that meets the 45/55% duty cycle requirement. The second approach is to use a less expensive crystal oscillator and implement a divide-by-two function. Some microprocessors have addressed this by internally performing the divide-by-two.

Since duty cycle is defined as a percentage, the room for error becomes tighter as the system clock frequency increases. For example, in a 25 MHz system clock with a 45/55% duty cycle requirement, t_{PS} cannot exceed a maximum of 4ns (t_{PLH} of 18ns and t_{PLH} of 22ns) and still meet the duty cycle requirement. However, for a 50 MHz system clock with a 45/55% duty cycle requirement, t_{PS} cannot exceed a maximum of 2ns (t_{PLH} of 9ns and t_{PHL} of 11ns) and still meet the duty cycle requirement. This analysis assumes a perfect 50/50% duty cycle input signal.

Definition:

$$t_{PS} = | t_{PHL} - t_{PLH} |$$

Pin Skew or Transition Skew = Time pin HIGH-to-LOW minus time pin LOW-to-HIGH

Both HIGH-to-LOW and LOW-to-HIGH propagation delays are measured at each output pin across the given device. For example, a 33 MHz, 50/50% duty cycle input signal would be degraded by 2.6% due to a t_{PS} = 0.8ns (Note: Output symmetry degradation also depends on input duty cycle).

Opposite Edge Skew

Opposite Edge Skew (t_{OST}) defines the difference between the fastest and the slowest of both transitions within a given device. Given a specific system with two components, one being positive-edge triggered and one being negative-edge triggered, t_{OST} helps to calculate the required delay elements if synchronization of the positive- and negative-clock edges is required.

Definition:

$$t_{OST} = | t_{P(m)} - t_{P(n)} |$$

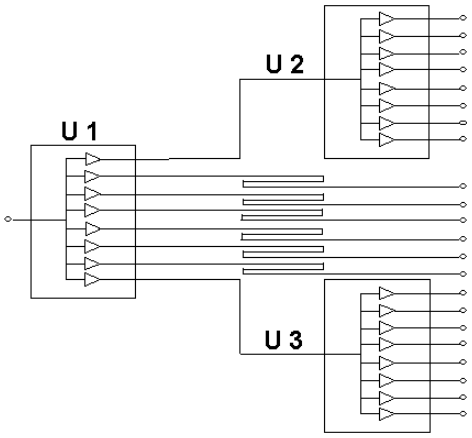
Opposite edge skew = Time output pin m minus time output pin n

Where:

Any edge transition (HIGH-to-LOW and LOW-to-HIGH) measured between any two outputs (m or n) within any given device.

Part Variation Skew or Part-to-Part Skew

Part Variation or Part-to-Part skew (t_{PV}) defines the distribution of propagation delays between the outputs of any two devices. Part-to-part skew (t_{PV}) becomes a critical parameter as the driving scheme becomes more complicated. This usually applies to higher-end systems that go from single clock drivers to distributed clock trees in order to increase fan out. In a distributed clock tree, part-to-part skew between clock drivers must be minimized to optimize system clock frequency. In the case of a clock tree in Figure 7, the total skew becomes a function of $t_{OSLH/HL}$ of U1 plus t_{PV} of U2 and U3.



Case 1: Single Clock Driver

Total Skew = common edge skew U1

= t_{OSLH} or t_{OSHL} of U1

Case 2: Distributed Clock Tree

Total skew (U2, U3) = common edge skew (U1) + part-to-part skew (U2, U3)

= t_{OSLH} or t_{OSHL} of U1 of U2 and U3

Definition:

$$t_{PV} = | t_{Pu,v} + t_{Px,y} |$$

t_{PV} = common edge skew of driver plus part-to-part skew of all drivers

Where: t_{PV} is any edge transition (HIGH-to-LOW or LOW-to-HIGH) measured from the outputs of any two devices.

FIGURE 7. A Clock Distribution Tree

Electromagnetic Interference

Electromagnetic Interference (EMI) consists of any unwanted spurious, conducted and/or radiated signals of electrical origin that can cause interference and degradation of system performance. This interference can result in data errors and system faults and can cause problems in line-to-line connections, inside the actual system, outside on the system's cables, or in other nearby systems.

EMI is directly related to system layout and noise level. EMI radiation sources include ICs, cables, connectors, and traces. Overall board and system layout have a significant effect on EMI radiation. Current flowing in a path within the system generates EMI. These paths can be V_{CC} to ground plane loops or transmission lines. The current pulses create magnetic field energy, while the voltage drop across the loop creates electric field energy. The current path material itself acts as an antenna either transmitting or receiving both magnetic and electrical fields.

EMI generation is a function of several major factors: signal frequency, duty cycle, edge rate, and output voltage swing. Current spikes, power line noise, and output ringing also contribute to overall EMI radiation. In addition to the signal components, circuit radiating area and the resultant antenna radiating efficiency also play an important role in EMI radiation.

Calculating Maximum Electric Field

As noted, system EMI is in large part a function of current loop area. Typically the largest loop areas in a system consist of backplane transmission lines and I/O cables. The V_{CC} to ground current loops on ICs are small in comparison to the current loops in transmission lines and power to ground plane loops.

The formula for modeling the maximum electric field is:

$$|E|_{Max} = \frac{1.32 \times 10^{-3} \bullet I \bullet A \bullet f^2}{D} \left[1 + \left(\frac{\lambda}{2\tau D}\right)^2\right]^{1/2} \frac{\mu V}{m}$$

Where

$|E|_{Max}$ = Maximum E-Field in the Plane of the Loop

I = Current Amplitude in Milliamps

A = Antenna Area in Square cm

λ = Wavelength at the Frequency of Interest

D = Observation Distance in Meters

f = Frequency in MHz

and the Loop Perimeter (P) is much less than the Wavelength (λ)

EMI Design Considerations

Designing a system with low EMI is critical to reliable system operation. Additionally, national and international agencies regulate and test systems for maximum allowable levels of EMI. The task of designing a low EMI radiation system is involved and covers almost every aspect of system operation and layout. To ensure low EMI radiation:

- Design a transmission line with the lowest possible impedance to reduce the antenna effect. Long transmission lines, such as those in clock-driver or bus-interface circuits, should be laid out in intermediate PCB layers rather than surface layers.
- Use multilayer PCB boards that include full ground and power planes. This provides impedances several orders of magnitude lower than power and ground traces and reduces transient voltage drops in power distribution and return loops.
- Use PCB shielding. Laying out transmission lines between PCB V_{CC} and GND planes reduces characteristic impedance and horizontal polarization through shielding with PCB copper planes. The metal stiffeners at the PCB edges shield against horizontal polarization.
- Match the impedance of the drivers and the transmission lines. Radiated emissions are high when transmitted signals exhibit overshoot, undershoot, and ringing. To minimize these effects, maintain careful impedance matches between drivers and transmission lines and between transmission lines and receivers.
- Terminate transmission lines to reduce or eliminate ringing and reflections.
- Minimize the number of simultaneously switching outputs to moderate current pulse amplitude and output ringing.
- Eliminate or minimize cross-talk.
- Ensure that the power supply network can supply sufficient current under all operating conditions, that it is low impedance, and that it has adequate decoupling to suppress power supply switching noise.

Summary

The key to designing for high signal integrity is the reduction of noise and interference phenomena below levels that will adversely affect signal quality. System interference includes switching noise, cross-talk, jitter, skew, and electromagnetic interference (EMI).

All electronic systems contain some elements of interference. Knowing the causes of noise and interference leads to an understanding of how they hinder performance and reliability as well as how they can be minimized or eliminated.

The goal is to reduce noise below operational interference levels. The level of signal integrity required will be different for every system type. Cost, function, and operating speed all play a part in the amount of noise that can be in tolerated in a design.