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Attack The Noise Gremlins That Plague High-Speed ADCs

Proper Converter Biasing, Voltage-Reference Considerations, And Careful Layout And Grounding Will Boost Accuracy.

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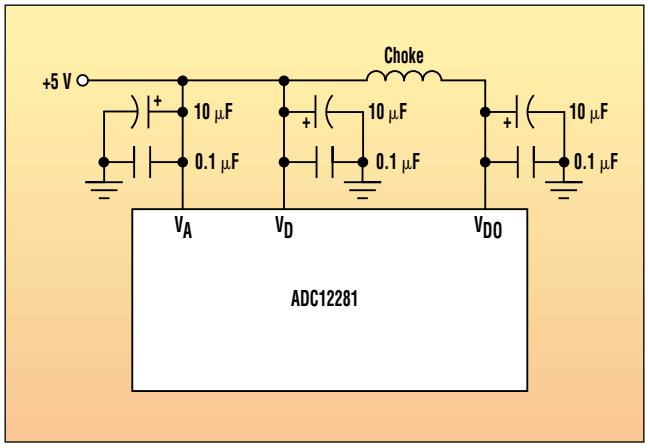
The analog nature of our physical world and the growing need to process continuous functions in the digital domain place ever-stringent performance demands on today's analog-to-digital converters (ADCs). A converter's raw processing speed per se, however, isn't usually the weak link in the system—though many designers find it difficult to get expected performance from a given device. Rather, it's the presence of noise.

The system designer's task, then, is achieving the ADC's advertised spec-sheet capabilities by addressing some signal and power issues in a practical way. These include minimizing the noise coming from power supplies or on its lines, establishing proper circuit biasing in the ADC, developing board layouts whose components and traces are resistant to unwanted coupling, and implementing sound grounding techniques. Overall, it's a better method than the "brute-force" technique of selecting ADCs with resolution that's higher than necessary.

Power considerations and associated issues are often the system designer's last thought, until noise—which is often coupled into the ADC through the power-supply pins—creeps in. The debate between analog and digital circuitry also complicates matters. Indeed, the supply used for digital circuitry may be too noisy for analog or mixed-signal components such as ADCs, which usually have a poor high-frequency power-supply rejection ratio (PSRR). Any way you look at it, however, getting the noise out of the system that powers the converter is critically important.



1. Separately bypass the power supply at both the low and high frequencies with capacitors suitably valued to the particular ADC and its frequency of operation. Isolate the ADC's output driver supply line with a small choke. A ferrite core with 2.5 turns will do well.

One key to improving ADC performance is maximizing its effective PSRR. A product's PSRR specification indicates the variation in a particular parameter for a given change in dc power-supply voltage.

For example, an ADC may specify the PSRR as the ratio of the change in full-scale gain or offset error with a given change in the dc supply voltage, usually expressed in dB. For many ADCs, the rejection ratio isn't all that good. If a change in supply voltage from 4.75 to 5.25 V (500 mV) results in a full-scale ADC gain error of 4 mV, the PSRR is:

$$\text{PSRR} = 20\log\left(\frac{\Delta\,\text{Gain error}}{\Delta\,\text{Supply}}\right)$$

$$= 20\log\left(\frac{4}{500}\right) = -42\ \text{dB}$$

The PSRR of the same converter will be much worse with an ac signal riding on the supply voltage. If analog and mixed-signal components are treated as though they have essentially a 0-dB PSRR, circuits will have better noise performance than they would if you relied upon the dc PSRR spec at higher frequencies. To minimize supply-noise problems, analog and digital supply pins should be separately decoupled with low-frequency and high-frequency bypass capacitors.

Typically, a parallel combination of

10- to 50-µF and 0.1-µF monolithic capacitors will suffice. The optimum capacitor values will vary somewhat with the particular ADC selected and the frequency of operation. Additionally, it's good practice to bring the power directly to the analog supply pins and supply the digital power pins through a choke. For high-speed ADCs, a ferrite core with 2.5 turns will do well. The choke usually only needs to isolate the power pins used for the output drivers *(Fig. 1)*.

Careful consideration to the size and routing of board traces also pays dividends. A wide trace for routing analog power, for instance, will often result in lower power-supply noise than it would with an analog power plane. This is because the capacitance between the ground and power planes can couple noise into the analog power plane, especially if the plane is over or below the digital ground plane. A trace has much less capacitance than a plane, though. Use the shortest possible runs to ground for the bypass capacitors.

The type of supply also affects performance. Switching power supplies, including capacitive dc-dc converters, create excessive electrical noise on the supply lines and on ground. When it comes to ADCs, it's best to avoid them. If there is no alternative, observe the following guidelines:

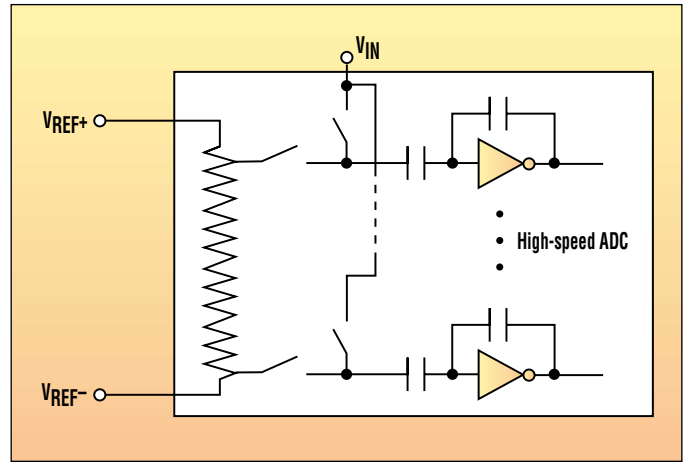
- Locate the switcher circuit as far as possible, electrically and physically, from all analog circuitry—especially from high-impedance nodes and low-level signals.
- Keep the switching circuit small and compact.
- Keep all traces with switching currents and voltages as short as possible.
- Use a linear regulator, if possible, to supply the analog circuitry. Or filter the analog supplies very well, at least.

The analog input signal is measured with respect to the reference voltage. The digital output indicates the ratio of the analog input to the reference voltage at the moment of sampling. For instance, an ideal 10-bit ADC with a 2-V reference, sampling a 1.6-V signal, yields an output code of:

$$\text{Output code} = \left(\frac{1.6}{2.00}\right) \times 2^{10} = 819$$

Any noise in the reference circuit will cause the instantaneous value of the reference voltage to change, altering the output code. In the above example, an instantaneous reference error of 50 mV changes the 2.00 V in the above equation to 2.05 V. The output code then becomes:

$$\text{Output code} = \left(\frac{1.6}{2.05}\right) \times 2^{10} = 799$$

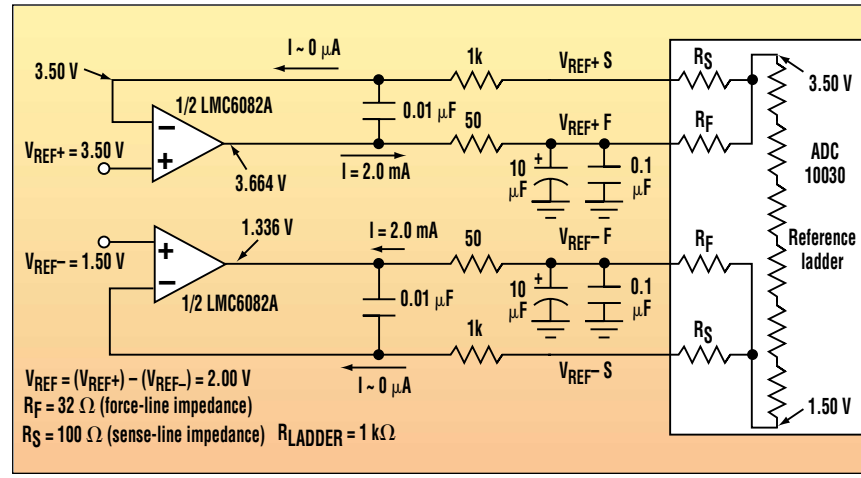


2. Switches in the reference ladder of the ADC add noise to the reference source. ADCs with reference force and sense pins make it easy for the designer to control the reference voltage at the top and bottom of the reference ladder.

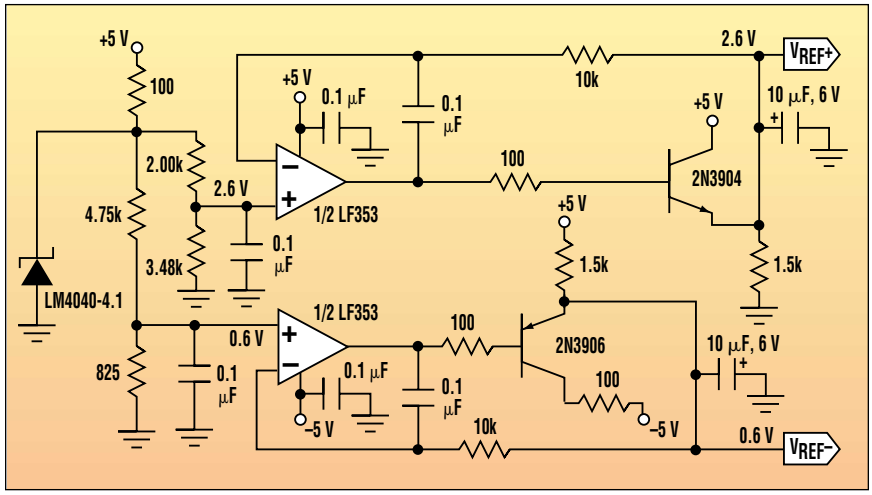
The error at any given instant is a function of the reference voltage error, the input voltage at the time of sampling, and the nominal reference voltage value. So, the importance of keeping the reference voltage quiet and stable cannot be overemphasized. Another source of noise comes from the ADC itself.

The reference ladder of high-speed converters has many internal switches *(Fig. 2)*. As these switches open and close (usually at the ADC's clock rate), they inject charge into the ladder, adding noise to the system. ADCs with reference force and sense pins make it easy to force the reference ladder to a precise dc voltage by enclosing the ends of the ladder in the driving amplifiers' feedback loops. This eliminates errors due to voltage drops across the printed-circuit-board traces, device bond wires, and traces within the converter.

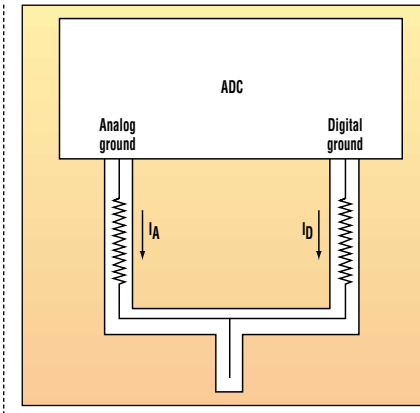
The op amp chosen for this application should have a low offset voltage to minimize the resulting ADC gain and offset errors. The LMC6082A *(Fig. 3)* was chosen for its low offset voltage (800 µV maximum, over temperature) and reasonable price ($2.53 in hundred-unit quantities). The 0.01-µF op-amp feedback capacitor adds a low-frequency pole to the op-amp transfer function, ensuring circuit



3. Op amps used to establish the ladder's limits should have low offset voltage to minimize the ADC's gain and offset errors. The 0.01-µF feedback capacitor across the op amp maintains circuit stability. Additional bypass caps across the ADC's reference pins help keep noise low.



4. This driver circuit for ADCs without reference force and sense pins behaves as a low-impedance buffer with the feedback loop closed around it. Emitter-follower transistor stages and 0.1-µF feedback-loop capacitors ensure circuit stability.



5. The differing ground currents that flow in boards that have separate analog and digital common points create a small potential between the grounds. Minimizing the resulting noise with this layout requires much trial-and-error experimentation.

stability *(Fig. 3)*. The bypass capacitors at the ADC's reference pins provide a low-impedance ac path to ground for the top and bottom of the reference ladder, keeping the reference pins quiet.

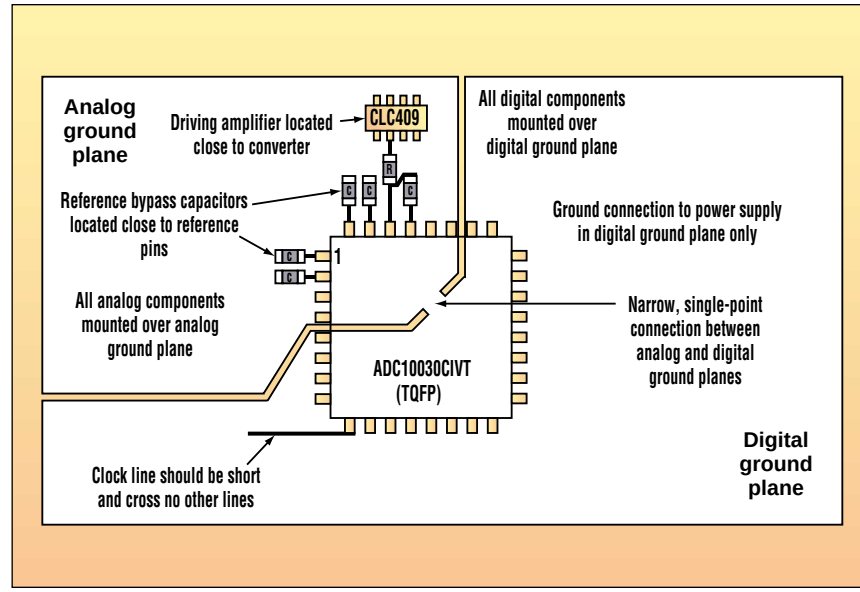
The reference driver circuit in Figure 4 is intended for ADCs without reference force and sense pins. This circuit uses a low-impedance buffer with the feedback loop closed around it. The 0.1-µF capacitor in the op-amp feedback loop ensures stability by reducing the high-frequency gain to unity. The output transistors are configured as emitter followers (high current gain, unity voltage gain). The additional voltage gain of a common-source or common-emitter configuration in the feedback loop of an op amp invites instability. That's why those configurations aren't recommended.

There are many ways to connect the analog and digital grounds of an ADC. The most important thing to remember is that they should both remain at the same potential at all times. One of the oldest grounding methods is to use separate analog and digital ground traces from the ADC to the power supply or to the board's power-ground entry point. The difficulty in doing this, though, is that the magnitude and frequency components of the analog and digital currents differ. This results in a potential difference between the analog and digital grounds of the converter as these currents flow through their respective trace resistances to a common point *(Fig. 5)*. Another big problem with this technique is that trial and error, lots of experience, and a bit of luck are needed to secure low noise levels.

Alternative Ground Techniques

Also, grounding can be accomplished by connecting all ground pins to the analog ground plane at the ADC. This can work well for ADCs with relatively low-frequency digital ground currents that wouldn't add significant noise to the analog ground plane. But it isn't desirable for high-speed ADCs, because their fast logic edge rates can add digital noise to the analog ground plane. Avoid this technique for sample rates over a few hundred kilosamples per second.

For very good first-time results, use separate analog and digital ground planes placed in the same board layer. The boundary between these planes should pass beneath the ADC and separate the pins with analog functions from those with digital functions. The two ground planes should be connected beneath the ADC by a narrow trace, the width of which is a function of the copper thickness, the analog ground-current



6. Use this suggested ground-plane layout for the ADC10030 and other similar high-speed ADCs. The trace width connecting analog and digital grounds, which itself is a function of copper thickness and the magnitude and frequency of analog ground currents, is a primary consideration.

frequency, and the amount of analog current going through this point.

We have empirically found that a width of 2 to 3 mm will work well with 1-oz copper and FR-4 board material. This narrow connection provides a relatively high impedance to the flow of high-frequency digital ground currents with high edge rates, but a relatively low impedance to the analog ground currents with lower-frequency components. A suggested ground plane layout for the ADC10030, a 10-bit, 27-Msample/s ADC, is shown in Figure 6.

Compared to the digital ground currents, the analog energy can flow through the connection between the analog and digital ground planes more easily. Consequently, the power-supply ground should be connected to the digital ground plane.

To avoid interaction between the ADC ground current and the digital ground currents of any high-powered digital components, locate the ADC's linear power supply ground or its regulator close to the ADC. Place the switching regulator and any high-current digital components as far from the ADC as possible.

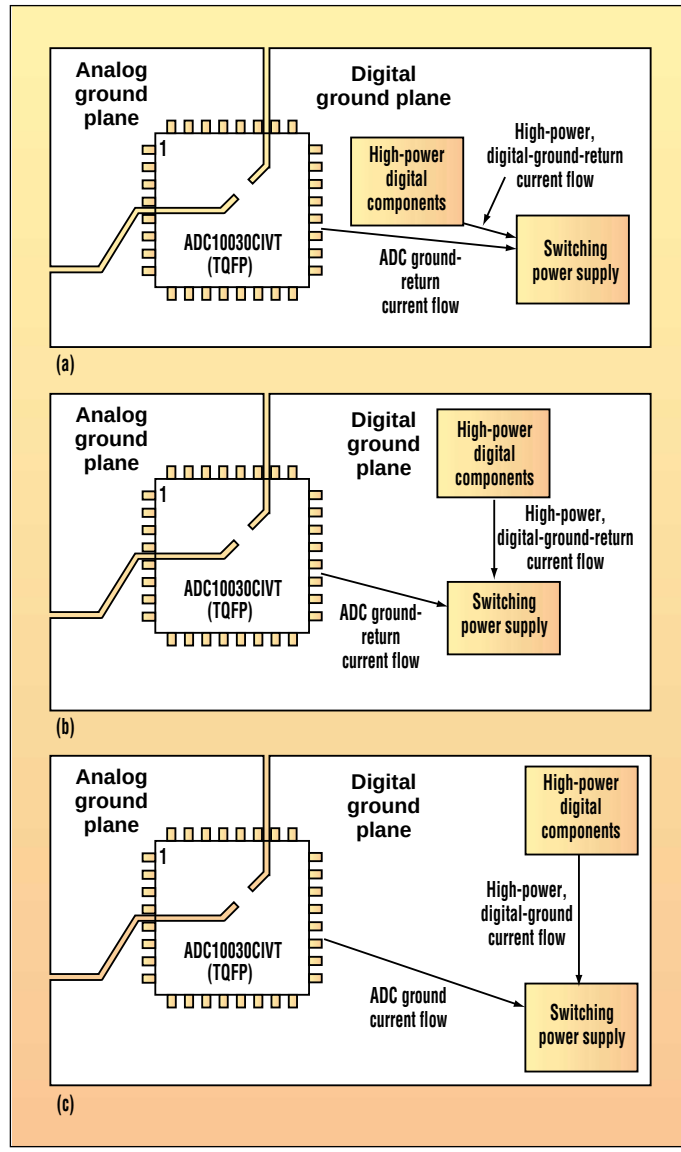
On the other hand, if you must use a switching supply without a linear regulator, filter the ADC supply voltages well and locate the switching supply as far as practically possible from the ADC. The ADC ground current and high-power digital ground-current paths should not run in parallel with each other. They also should be kept as physically far as practically possible from each other.

Figures 7a and 7b show examples of poor layouts. If the ADC and high-power digital ground-return paths are common, the high-power digital ground-current fluctuations can cause voltage fluctuations in the ground path that are seen at the ADC. These ground voltage fluctuations appear in the ADC input as noise. Figure 7c shows better positioning of these components.

The analog and digital ground planes should not overlap each other. Current in the digital ground plane may couple energy into the analog ground plane, adding noise to the analog circuitry. Since the grounds don't overlap each other, it makes sense to use a single layer for the analog and the digital ground planes. Digital noise can be coupled into the analog circuitry if digital components are placed over the analog ground plane, or vice versa. Place analog components over the analog ground plane and digital components over the digital ground plane to keep digital noise out of the analog circuitry.

You'll get the best high-frequency performance with a physically straight signal path. A path that folds back upon itself can lead to capacitive and inductive coupling that can cause unwanted feedback, resulting in increased distortion and noise. The best layout is one that produces a straight or nearly straight signal path. Also, be especially careful with inductors. Mutual inductance can change the characteristics of the circuit in which it is used. Orient inductors 90° to each other with a minimum separation equal to the length of their bodies. Alternatively, place them in line with each other, again separated by at least the length of their bodies. With high current levels, additional separation may be required.

It's not too difficult to obtain the high data-sheet performance touted for some high-speed ADCs. But it does require knowledge and application of sound design and layout rules. Proper attention to power-supply connections, voltage reference considerations, and layout and grounding go a long way toward getting there. ❐



7. A common path for the ADC and high-power digital ground returns will create ground noise at the ADC (a). These ground-return paths are well-separated, but the proximity of the switching supply to the ADC and other analog components can induce noise into the analog circuitry (b). When ground currents from properly placed switching supplies and high-power digital components aren't parallel to the ADC's ground current, noise is minimal (c).

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