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Pay Attention To The Clock And Output Bus To Improve High-Speed ADC Designs

Accounting for "analog" effects will cure "digital" gremlins found in high-speed ADC designs.

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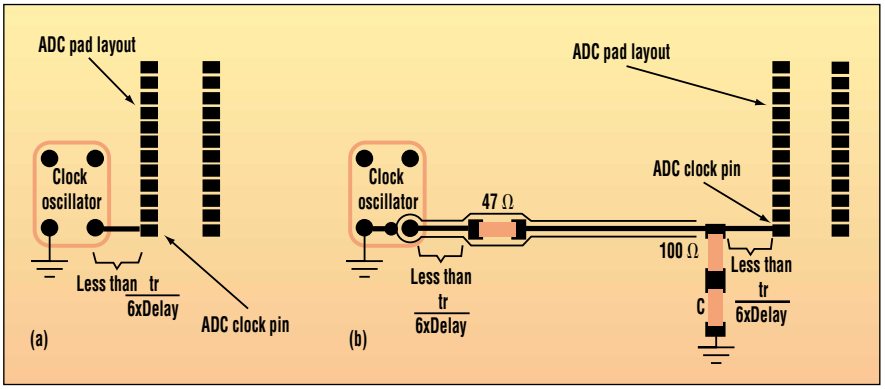
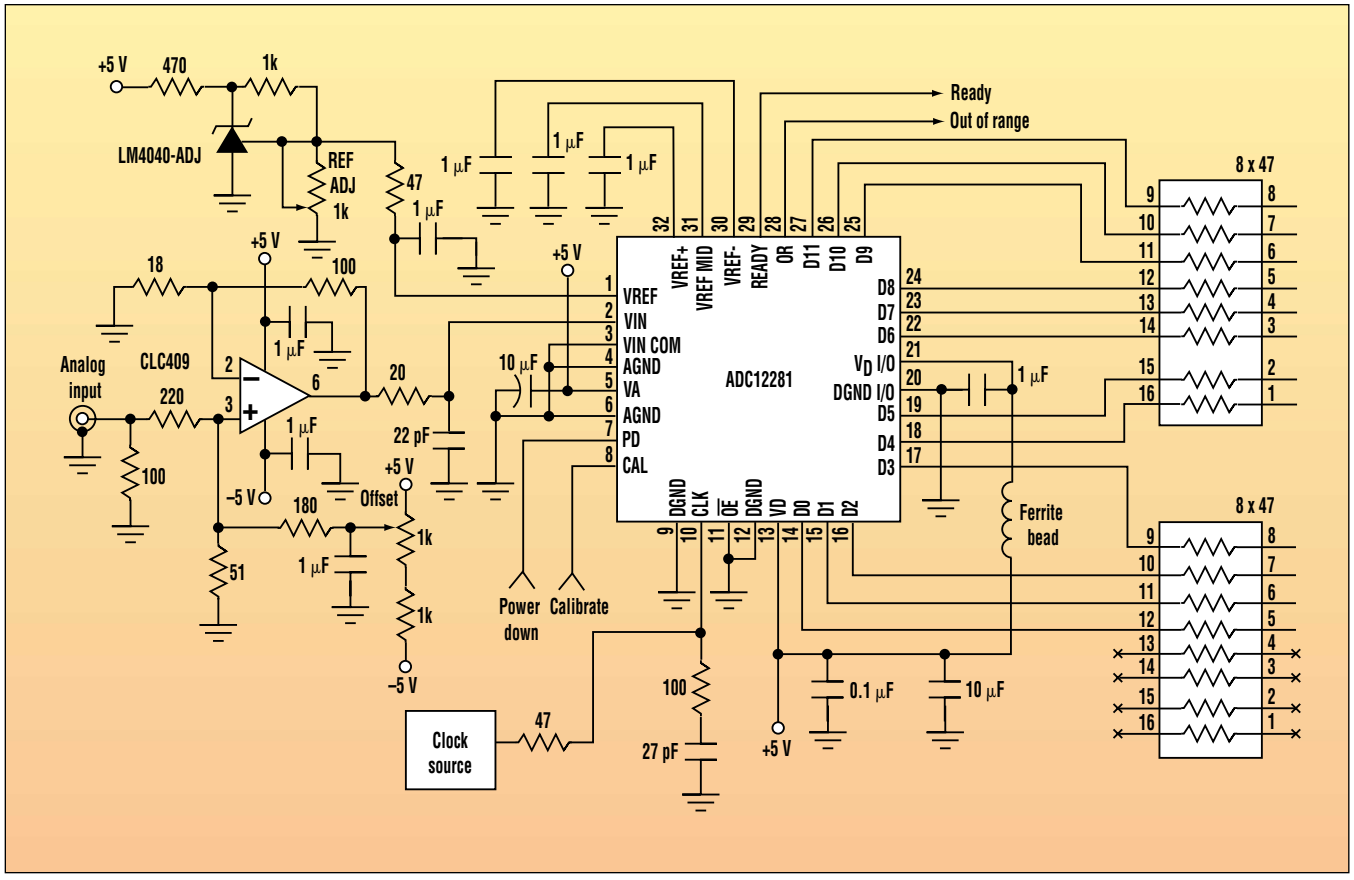
As the digital revolution increases the need for faster analog-to-digital converters (ADCs), we are faced with an ever-increasing design challenge. It's easy to pick high-speed parts off the shelf. But, getting the best possible performance from high-speed ADCs in an actual circuit requires careful attention to the design. Things that didn't cause problems at lower sample rates can almost halt efforts to use high-speed ADCs.

In my earlier articles, *"Attack the Noise Gremlins That Plague High-Speed ADCs"* (ELECTRONIC DESIGN, *Dec. 17, 1999, p. 107*), and *"Maintaining Signal Integrity Enhances ADC Circuit Performance"* (ELECTRONIC DESIGN, *May 1, p. 115*), I discussed the biasing, layout considerations, and input-signal handling to further improve high-speed ADC circuit performance. Here, I will explain how to further boost ADC performance by properly handling the ADC clock signal and digital outputs.

The importance of the clock signal to ADCs is often underestimated. Maximizing system noise performance requires a stable clock signal that's free of phase noise, also known as jitter. Clock jitter causes uncertainty in the sampling point, which results in noise at the ADC output. The SNR resulting from clock jitter is:



1. Proper clock termination will prevent clock-line reflections and resultant jitter. When the clock source is located close to the ADC's clock input, the trace can be considered a simple wire (a). For maximum jitter reduction at clock rates above 10 MHz, both ends of the clock line should be terminated (b).



2. This example of a complete ADC circuit employs the design concepts needed to obtain maximum performance from high-speed ADCs. Note that the clock line is terminated at both ends, and the ADC outputs are isolated with resistors to limit noise caused by the output switching. These resistors should be located as close to the ADC outputs as possible, preferably within a centimeter of the output pins.

$$SNR_{JITTER} = -20\log_{10}\left[\frac{\frac{V_{FSR}}{2}(2\pi F_{IN})10^{\frac{V_{IN}}{20}} \times JITTER}{\sqrt{2}}\right] \quad (1)$$

where:
SNR_{JITTER} = SNR due to jitter
V_{FSR} = ADC full-scale input in V p-p
F_{IN} = ADC sinewave input frequency in Hz
V_{IN} = ADC input level in dB relative to full scale (dBFS)
JITTER = rms jitter in seconds

SNR degradation is independent of sample rate. The total SNR becomes:

$$SNR_{TOTAL} = -20\log_{10}\sqrt{10^{\left(\frac{-SNR_{ADC}}{10}\right)} + 10^{\left(\frac{SNR_{JITTER}}{10}\right)}} \quad (2)$$

where SNR_{ADC} is the data sheet SNR value for the ADC.

For a 2-V p-p, 5-MHz input at –6 dBFS, 10 ps of clock jitter will result in an SNR_{JITTER} of 79.1 dB *(Equation 1)*. An ADC with an SNR of 59 dB will have its total SNR reduced to 58.2 dB by this 10 ps of jitter *(Equation 2)*. Increasing the signal level to 0 dBFS will result in an SNR_{JITTER} of 73.1 dB and a combined SNR of 57.4 dB. So, in this example, the SNR degradation for a –6-dBFS signal is 0.4 dB, while the SNR degradation for a full-scale signal is 0.8 dB.

While reducing the input amplitude improves the SNR due to jitter, it also increases the quantization noise level. The SNR degradation resulting from the increased quantization noise level is greater than the total signal-to-noise ratio improvement from reducing the input level. Therefore, for every dB reduction in input level, we should reduce the SNR_{ADC} formula by the same amount *(Equation 2, again)*. This will result in the best SNR performance at 0 dBFS.

The best way to improve SNR_{JITTER} is to reduce the jitter at its source. Don't allow the clock line to run parallel to any other signal-carrying line—analog or digital. Digital signals can couple energy into the clock line, increasing clock jitter. Plus, the clock line can couple clock noise into an analog trace, again reducing SNR performance. If the clock line must cross other lines, the crossing should be at 90° to reduce coupling. Note that there will still be some capacitive coupling.

Ground Considerations

It also is a good idea to run a digital ground trace (or shield) around the clock line, and to include a digital ground plane beneath the trace. At clock rates below 100 MHz, this trace should be grounded at only one point to prevent ground loops. This grounded trace and ground beneath the trace will help prevent the pick-up of other signals that might cause clock jitter, and will also reduce the clock energy radiation.

At frequencies above 100 MHz, the trace around the clock line should be grounded at many places. This provides a low-impedance path to ground from any point on the guard ring. If you don't do this at high frequencies, the ring becomes an inductance that

picks up and radiates the clock signal.

A well-designed crystal-based clock source is required for minimum clock jitter. To limit the noise due to sampling jitter to 1/2 LSB, maximum jitter from all sources must not exceed:

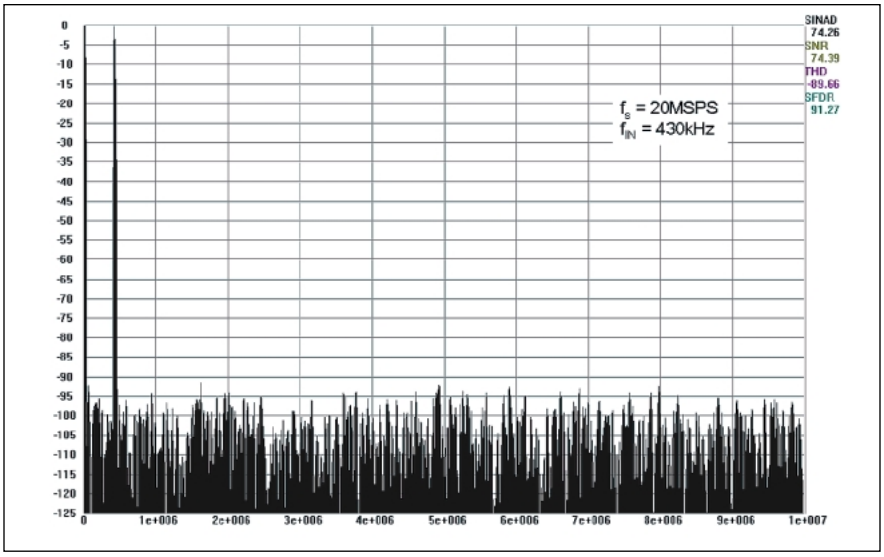
$$\text{Maximum Jitter} = \left[\frac{1}{2^{(n+1)}\pi f}\right] \text{seconds (rms)} \qquad (3)$$

where:
A = peak amplitude of input signal
n = ADC resolution (number of bits)
f = maximum signal-input frequency in Hz.

High-speed ADCs usually have specifications for maximum aperture jitter, which is the uncertainty introduced by the ADC itself. Subtract this from the maximum jitter found in Equation 3 to determine the jitter that may be allowed from the clock source. Building a clock oscillator from logic gates, as is done for many digital circuits, isn't satisfactory for an ADC clock. Such circuits exhibit too much jitter. A well-designed crystal oscillator will provide much better jitter performance.

To minimize introduction of jitter into the clock line, keep the clock trace from the clock source to the ADC as short as possible. The trace can be considered a simple wire if the distance between the clock source and the ADC's clock input is less than Distance = Rise time / (6 x Delay) where "Delay" is the propagation rate of the signal on the board, and is about 150ps/inch (6ps/mm) on a board of FR4 material. If the distance between the clock source and the ADC's clock input is greater than this, the wire must be treated as a transmission line with both ends of that line terminated.

The characteristic impedance of the typical printed circuit board trace is usually in the area of 100 Ω. Assuming a 50-Ω clock source, insert a 47- to 51-Ω resistor in series with the clock line at the source. This resistor should be as close to the clock source as possible and at least within the distance described above. *(Fig. 1b)*.



3. Here is one of the displays from the WaveVision software. This software simplifies dynamic measurements on fast ADC designs. SINAD, SNR, THD, and SFDR can be seen at a glance.

Termination Techniques

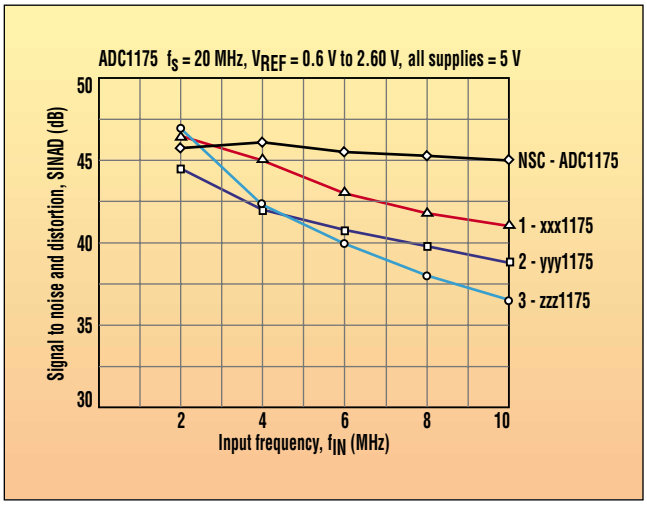
In many cases, the termination at only the clock source is adequate. But at clock rates above 10 MHz, it's best to terminate the ADC end of the line too. This termination is a 100-Ω resistor in series with a capacitor to ground, located within 1/8 of the ADC clock pin's clock-frequency wavelength *(Fig. 1b, again)*. The capacitor prevents dc loading of the clock source. Such loading could result in insufficient clock amplitude. This loading could instead bring about an effective change of clock duty cycle within the ADC. The value of the capacitor should provide a capacitive reactance of around 50 to 100 Ω at the clock frequency. A higher impedance won't allow the resistor to provide any termination. Too low an impedance will result in the capacitor failing to charge sufficiently in order to build enough amplitude for triggering the ADC.

Furthermore, proper clock-line termination will reduce the overshoot and undershoot, which can upset the operation of the ADC, thereby preventing its normal functioning. Many semiconductor devices won't operate correctly if their inputs exceed the supply rails.

The rise and fall times of the clock signal affect the ADC noise performance as well. Slow rise and fall times will result in the uncertainty of when the input is sampled, having the effect of adding clock jitter within the ADC.

Very-fast rise and fall times, on the other hand, can inject noise into the ADC substrate. This can add to the input noise of the ADC. Look for the manufacturer's recommended clock rise and fall times on the data sheet. The value of the capacitor in series with the clock-line terminating resistor near the ADC can be varied somewhat to adjust clock rise and fall times.

Just as noise can be injected into the analog-signal and voltage-reference inputs, the switching of the outputs also can inject noise back into the ADC input. Any capacitance connected to the ADC outputs must be charged and discharged by these outputs. Whatever logic device is connected to the ADC outputs will have capacitance, as will the interconnecting traces. The larger this total capacitance, the more current will flow in the interconnecting lines and the ADC outputs.



4. "Equivalent" parts from various manufacturers aren't always equal, even when they fit the same socket. This graph shows the SINAD variation in four devices verses the input frequency.

Consider Ground Bounce

High-speed ADC outputs can change at rates up to the clock frequency, injecting currents into the ADC substrate every time any of the outputs change states. The injection of these current pulses into the ADC die-substrate causes the ADCs internal ground to bounce, adding noise to the ADC input.

To minimize this effect, connect the input of only a single logic gate to each ADC output. Place a resistor in series with each ADC output line to limit the flow of current in these output lines. The value of these resistors isn't critical. Still, the time constant of this resistance, the capacitance between them, and the driven logic input should be less than the ADC clock period. Generally, a resistor of 47 to 100 Ω will work nicely.

The addition of these resistors will limit the noise injection into the substrate that would otherwise be caused by the output switching. These resistors should be as close to the ADC outputs as possible, preferably within a centimeter of the output pins. Locating the driven logic device close to these resistors will help too, as the shorter lines means less capacitance. A circuit with the suggestions from this and the previous articles is shown in Figure 2.

Choosing an ADC that has the performance you need is very important. The trick is to determine the performance of a given ADC under the conditions you want to use it.

For example, you might need a minimum 45-dB signal to noise and distortion (SINAD) over a 4- or 5-MHz bandwidth, but this parameter is specified only at one frequency. Fortunately, many data sheets have typical characteristic curves that can help. While these curves are just typical and offer no guarantees, they can clue you in on the expected performance trend of certain variables, such as input frequency.

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Many manufacturers provide evaluation boards to help you gauge the performance of their products. National Semiconductor even provides complete evaluation systems for its high-speed ADCs, making measurement of dynamic performance parameters very simple. The WaveVision software comes with the evaluation system, but also can be downloaded free from National's website, *www.national.com/appinfo/adc/*. It can be used to perform FFTs and calculate dynamic performance from any sampled data file *(Fig. 3)*.

"Equivalent" parts from different manufacturers aren't necessarily equal, even though they may function in the same socket. SINAD verses input frequency is plotted for some high-speed "equivalent" ADCs *(Fig. 4)*. SINAD was chosen for plotting because this specification is considered a critical high-speed ADC performance parameter. These devices are all the popular "1175" 8-bit, 20-Msample/s ADCs from four different suppliers, evaluated on the same board. They all fit the same socket, but aren't really equivalent. Before changing suppliers of "equivalent" parts, be sure to check out the alternative product in your socket.

When all is said and done, maximizing high-speed ADC system performance isn't a trivial task. But, attention to some fundamental principles will facilitate the optimization of your system's performance.

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