Circuit Layout Techniques And Tips (Part IV of VI)
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Layout Techniques To Use As The ADC Accuracy And Resolution Increase

Initially, analog-to-digital converters (ADCs) rose from an analog paradigm where a large percentage of the physical silicon was analog. As design topologies evolve this paradigm shifted to where slower speed ADCs were predominately digital. Even with this on-chip shift from analog to digital the PCB layout practices have not changed. Now, as always, when the layout designer is working with mixed-signal circuits, key layout knowledge is still needed in order to implement it effectively. This article will look at the PCB layout strategies required for ADCs using successive approximation register (SAR) and Sigma-Delta topologies.

SAR Converter Layout

SAR ADCs can be found with 8-, 10-, 12-, 16-bit and sometimes 18-bit resolutions. Originally, the process and architecture for these converters was bipolar with R-2R ladders. But recently these devices have migrated to a CMOS process with a capacitive-charge distribution topology. Needless to say the system layout strategy for these converters has not changed with this migration. The basic approach to layout is consistent except for higher-resolution devices. These devices require more attention to prevent digital feedback from the serial, or parallel, output interface of the converter.

The SAR converter is predominately analog in terms of circuitry and the amount of real estate dedicated to the different domains on the chip (see Fig. 1.)

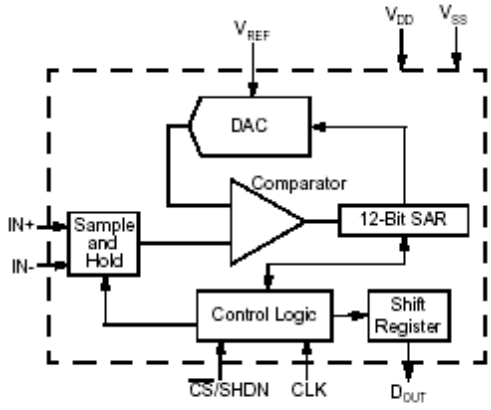
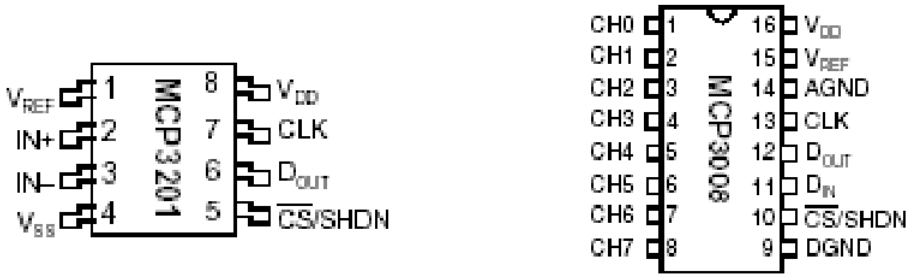


Fig. 1: 12-bit CMOS SAR ADC Uses Charge Distribution Across A Capacitive Array

Within this block diagram the sample and hold, comparator, most of the DAC and 12-bit SAR are analog. The remaining portions of the circuit are digital. As a consequence, most of the power and current needed for this converter is used for the internal analog

circuitry. There is very little digital current coming from the device with the exception of the small amount of switching that occurs in the DAC and at the digital interface.

These types of converters can have several pins for the ground and power connections. The pin names are often misleading in that the analog and digital connections can be differentiated with the pin label. These labels are not meant to describe the system connections to the PCB, but rather they identify how the digital and analog currents come off the chip. Knowing this information and understanding that the primary real estate consumed on the chip is analog, it makes sense to connect the power and ground pins on the same planes, e.g. analog planes (see Fig. 2.)



Microchip, 12-bit, 1 channel, SAR **Microchip, 10-bit 8 channel SAR**

Fig. 2: The SAR Converter, Regardless Of Resolution, Usually Has At Least Two Ground Connects: AGND And DGND. The Converters Here Are The MCP4008 And MCP3001

With these devices the ground is usually directed off the chip with two pins: AGND and DGND while the power is taken from a single pin. When implementing the PCB layout using these chips, the AGND and DGND should be connected to the analog ground plane with analog and digital power pins also connected to the analog power plane, or at least connected to the analog power train with proper by-pass capacitors as close to each pin as possible. The only reason that these devices would have only one ground pin and one positive supply pin, as with the MCP3201, is due to package limitations, but separate grounds enhance the probability of getting good and repeatable accuracy from the circuit.

With all of the converters the power supply strategy should be to connect all grounds, positive supply and negative supply pins to the analog plane. In addition, the ‘COM’ pin or ‘IN’ pin associated with the input signal should be connected as close to the signal ground as possible.

Higher resolution SAR converters (16- and 18-bits) require a little more consideration in terms of separating the digital noise from the quiet analog converter and power planes. When these devices are interfaced to a microcontroller, external digital buffers should be used in order to achieve clean operation.

Although these types of SAR converters typically have internal double buffers at the digital output, external buffers are used to further isolate the digital bus noise from the analog circuitry in the converter (see Fig.3.)

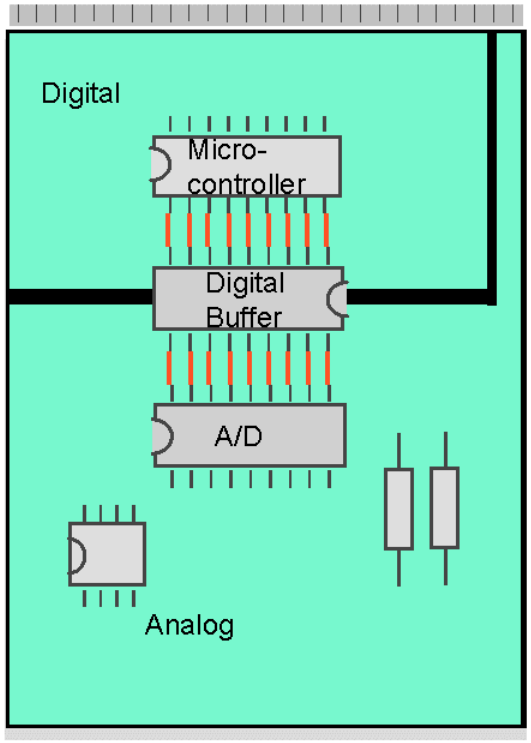


Fig. 3: With High-Resolution SAR ADCs Converter Power And Ground Should Be Connected To The Analog Planes. The Digital Output Should Be Buffered Using External 3-State Output Buffers, Providing Isolation Between Analog And Digital Sides

Precision Sigma-Delta Layout Strategies

The silicon area of the precision Sigma-Delta ADC is predominately digital. In the early days this type of converter was being produced this shift in the paradigm prompted users to separate the digital noise from the analog noise by using the PCB planes. As with the SAR ADC these types of ADCs can have multiple analog- and digital-ground and power pins. Once again the common tendency of a digital or analog design engineer is to try separating these pins into separate planes.

Unfortunately, this tendency is misguided, particularly if you intend to solve critical noise problems with the 16-bit to 24-bit accuracy devices.

With high-resolution Sigma-Delta converters that have a 10-Hz data rate, the clock (internal or external) to the converter could be as high as 10-MHz or 20-MHz. This high-

frequency clock is used for switching the modulator and running the oversampling engine. With these circuits the AGND and DGND pins are connected together on the same ground plane, as is the case with the SAR converter, and the analog and digital power pins are connected together, preferably on the same plane. The requirements on the analog and digital power planes are the same as with high-resolution SAR converters.

A ground plane is mandatory, which implies that a double-sided board is needed at minimum and on this board the ground plane should cover at least 75% of the area, if not more. The purpose of this ground plane layer is to reduce grounding resistance and inductance as well as to provide a shield against EMI and RFI. If circuit interconnect traces need to be put on the ground-plane side of the board, they should be as short as possible and perpendicular to the ground current return paths.

Conclusion

You can get away without separating the analog and digital pins of low precision ADC, with 6-, 8-, or maybe even 10-bit resolution. But as the resolution/accuracy increases with your converter selection the layout requirements also become more stringent. In both cases, with high resolution SAR ADCs converters and Sigma-Delta converters these devices need to be connected directly to the lower noise analog ground and power planes.