www.elecdesign.com
Electronic Design
The Authority on Emerging Technologies for Design Solutions

Maintaining Signal Integrity Enhances ADC Circuit Performance

Careful use of the driving amplifier optimizes high-speed ADC input circuitry and minimizes noise and distortion.

Nicholas Gray
NATIONAL SEMICONDUCTOR CORP.

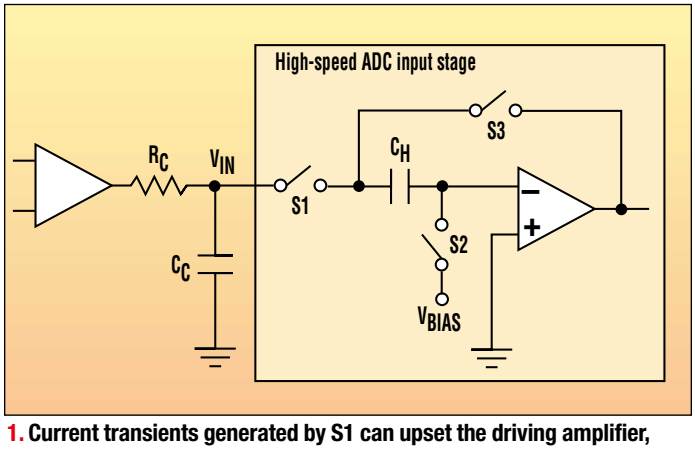
The digital revolution has created a growing need for analog-to-digital converters (ADCs). The world's analog information must change into digital form for processing. At the same time, advances in IC processing technology and monolithic ADC design techniques have lowered the cost while increasing the performance of high-speed ADCs. As a result, it is easier to use converters that have a higher resolution than what is actually needed to meet system performance requirements.

A designer who needs a 20-Msample/s ADC with a signal-to-noise and distortion ratio (SINAD) of 58 dB, for example, might think that a 10-bit ADC is required. But past experience has demonstrated a lack of 10-bit converters with a 58-dB SINAD specification. Many recent 10-bit ADCs do meet the 58-dB SINAD/9.3 effective-number-of-bits (ENOB) requirement, however *(see the table)*.

Other designers have found 10-bit ADCs that meet their specification requirements, but then they discovered that they couldn't get the advertised performance in their circuit. Frustrated, they had to turn to a 12-bit converter. Similar statements can be made for ADCs of any resolution.

In my earlier article, "Attack The Noise Gremlins That Plague High-Speed ADCs" *(*ELECTRONIC DESIGN, *Dec. 17, 1999, p. 107)*, I discussed the biasing and layout considerations needed to enhance ADC performance. Here, I'll explain how to optimize the ADC input circuitry to minimize noise and distortion.

Most of today's high-speed ADCs have sampling switches connected to



1. Current transients generated by S1 can upset the driving amplifier, resulting in additional noise at the ADC input. For best results, use R_C and C_C to isolate and filter the input sampling switch from the driving amplifier. The R_CC_C time constant must pass the highest input frequencies without significant attenuation or phase shift.

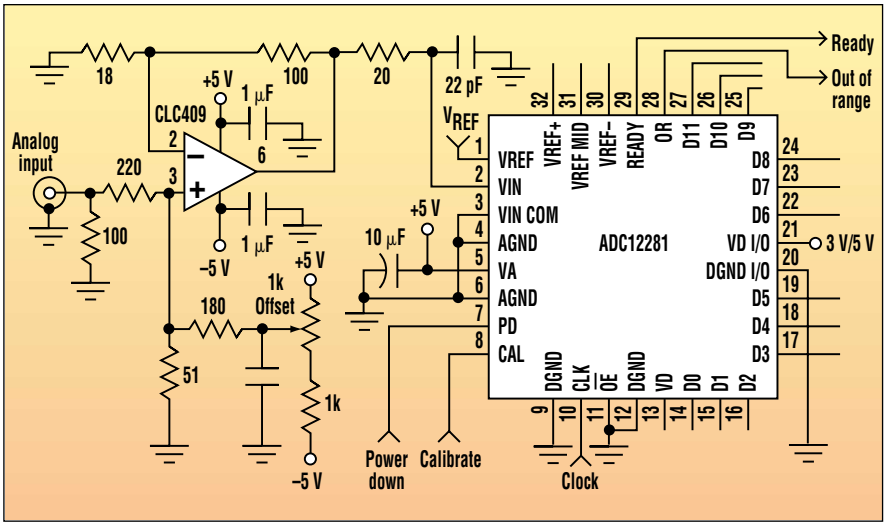
their analog input pins. When these switches open and close, current transients are generated that appear at the ADC's analog-signal input pin(s). This can upset the driving amplifier as it tries to correct for these transients, resulting in noise added at the ADC input. These input switches are part of the track-and-hold circuit at that input *(Fig. 1)*.

Circuit Operation

During the sample phase, S1 and S2 in Figure 1 are closed and S3 is open. This charges capacitor C_H to a potential of $V_{IN} - V_{BIAS}$. During the next clock phase, all three switches toggle. Capacitor C_H is connected across the amplifier, which holds the voltage for conversion. If there's a voltage across S1 just before it closes, a transient is generated at the ADC input.

Those transients can disturb the output of the amplifier driving this input. The amplifier tries to correct its output voltage to compensate, but the transient is gone by the time the amplifier reacts. If this reaction time plus amplifier-settling time is long enough, the ADC input might not settle before the input switch opens. The result is the acquisition of an erroneous voltage that adds noise to the signal being converted, resulting in a degradation of the converter's noise performance.

R_C and C_C filter the clock-rate transients that come out of the ADC input, thereby preventing them from upsetting the driver. R_C needs to be large enough to isolate the amplifier from the ADC input. But the R_CC_C time constant must be short enough to allow the highest input frequencies to pass without significant attenuation or phase shift.



2. This representative driving circuit for a sampling ADC has an RC configuration in the amplifier's output and input attenuation. This circuit is designed to drive a 12-bit, 20-Msample/s ADC, but the techniques are applicable to all sampling ADCs.

Determining The Time Constant

The required time constant depends on which parameter is to be optimized. For maximum SNR performance, start with a resistor between 47 and 100 Ω. (The value is not critical.) Then calculate the capacitor value as:

$$C = \frac{1}{2 \times \pi \times R \times F_{CLK}} \quad (1)$$

Unfortunately, the best total harmonic distortion (THD) and spurious-free dynamic-range (SFDR) performance is obtained when R = 0 Ω and C = 0 pF. Component choice is easy if the plan is to optimize either SNR or THD and SFDR. But in many applications, the signal should be optimized to noise and distortion, designated as either SINAD or S/(N+D). Here, SINAD is defined as a ratio expressed in dB. It's the input signal's rms value as it appears at the output to the rms value of all other spectral components below half the clock frequency. This includes harmonics, but not dc. SINAD is found to be:

$$SINAD = -20\log\sqrt{10^{\frac{-SNR}{10}} + 10^{\frac{THD}{10}}} \quad (2)$$

The SNR in Equation 2 is assumed to be positive, while THD is thought to be negative. The result is negative exponents for both terms. In terms of maximizing SINAD performance, the best R_CC_C time constant depends upon the specific ADC and its clock rate, as well as the specific type of amplifier, the pc-board layout, and board material. Because of these many factors, particularly the layout dependence, the optimum time constant is best determined em-

EXAMPLES OF HIGH-SPEED 10-BIT ADCS AVAILABLE WITH ENOB OF 9.0 AND HIGHER

Supplier	Product	Sample rate (MSPS)	Power supply (Volts)	PWR (mW)	SINAD (dB)	ENOB (bits)	SNR (dB)
						Approx. 4-MHz input	
National	ADC10321	20	5	98	59	9.5	60
Burr-Brown	ADS820	20	5	195	59	9.5	60
Philips	TDA8762	20	5	380	58.3[1]	9.4	59
National	ADC10030	30	5	121	58	9.3	59
ADI	AD9200	20	5	133	57	9.1	57
Intersil	HI5702	20	5	600	57	9.1	56
Intersil	HI5767	20	5	310	56	9.0	56

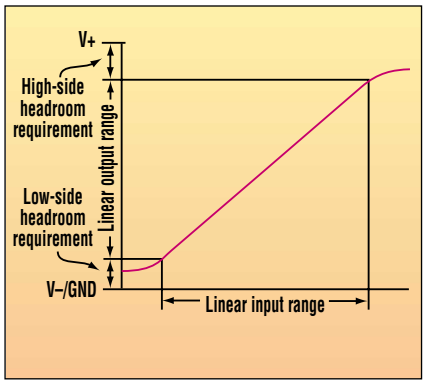
[1]SINAD not specified; calculated from ENOB

pirically. Start with a 47- to 100-Ω resistor and a capacitor determined by Equation 1. Then lower the capacitance until SINAD is maximized.

Figuring out the dynamic performance parameters like SNR, THD, SINAD, and SFDR can be done with the proper test equipment, if available. Alternatively, some ADC suppliers provide evaluation boards with free software that can perform this task. One example is the WaveVision software available from National Semiconductor. It's free and can be downloaded from the company's web site: *www.national.com/appinfo/adc/*.

Operational-amplifier phase margin usually drops as gain decreases below some device-dependent level. At small gains, it can be marginal. Too little phase margin causes ringing at the amplifier output after a fast-slewing input. Because the margin is better at higher gains, the user can get more by attenuating the input and operating the amplifier with a gain.

For most op amps, the inverting configuration is more stable than the noninverting one. Remember that not all op amps will provide optimal performance under the same conditions. One amplifier might provide its best performance at a gain of −5, while another may perform optimally with a gain between −8 and −10.



3. The amplifier supply voltage needs to be large enough to avoid headroom problems. Maintain a minimum voltage between the maximum signal peak and the power-supply rails to evade distortion. The headroom required rises with frequency.

A Typical Drive Circuit

A representative drive circuit for a high-speed ADC has an RC configuration at the amplifier's output and in its input attenuation *(Fig. 2)*. Although this particular circuit is designed to drive the ADC12281 12-bit, 20-Msample/s converter, the techniques are applicable to all sampling ADCs.

The overall gain of this circuit is unity. It has a nominal offset of +1.0 V. So an analog input signal of 2 V p-p centered at 0 V can be presented to the ADC as a 2-V p-p signal centered at +1.0 V.

The supply voltages to the amplifier driving the ADC should be high enough to avoid "headroom" problems. Headroom refers to the minimum voltage that must be maintained between the maximum signal peak and the power-supply rails in order to avoid distortion.

These problems arise because amplifiers typically lose gain and bandwidth as the output signal approaches the power-supply rails. The headroom requirement increases with signal frequency. A capacitive load, such as the input of a CMOS ADC, causes output-current requirements to rise with frequency *(Fig. 3)*.

A lot can be done to enhance circuit performance through thoughtful use of the driving amplifier. A future article will focus on clock and ADC digital-output-connection considerations that minimize noise.

Nicholas Gray *is a staff applications engineer with National Semiconductor's Data Conversion Systems Products Group, Santa Clara, Calif. He holds a BSEE degree from Gonzaga University, Spokane, Wash. Gray also has done graduate work at California State University, San Jose. He can be contacted at (408) 721-6962; e-mail: Nicholas.Gray@nsc.com.*