MP2259

1A, 16V, 1.4MHz Step-Down Converter

The Future of Analog IC Technology™

INITIAL RELEASE – SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MP2259 is a monolithic integrated step-down switch mode converter with an internal power MOSFET. It achieves 1A continuous output current over a wide input supply range with excellent load and line regulation.

Current mode operation provides fast transient response and eases loop stabilization.

Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

The MP2259 requires a minimum number of readily available standard external components. The MP2259 is available in TSOT23-6 and SOT23-6 packages.

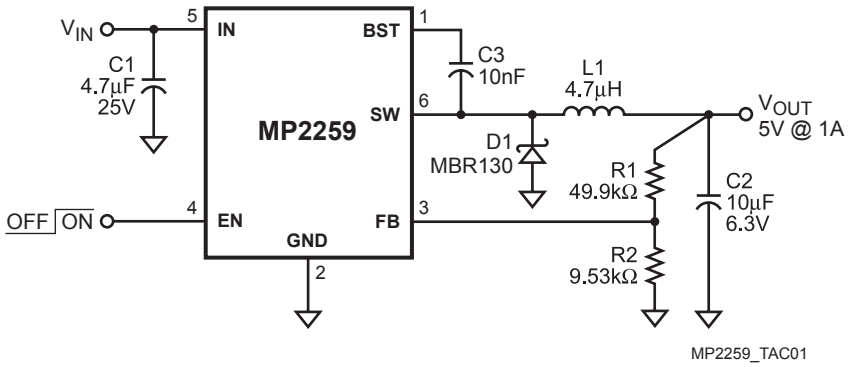
FEATURES

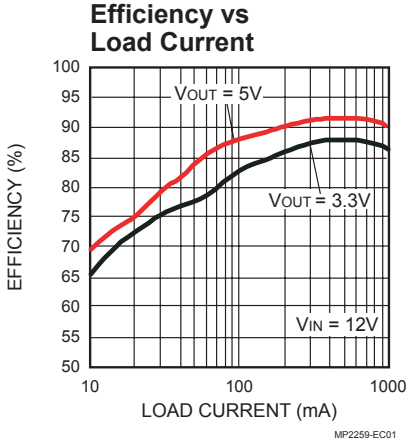
- 1A Output Current
- 0.5Ω Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- Up to 92% Efficiency
- 0.1μA Shutdown Mode
- Fixed 1.4MHz Frequency
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Wide 4.5V to 16V Operating Input Range
- Output Adjustable from 0.81V to 14V
- Available in TSOT23-6 and SOT23-6 Packages

APPLICATIONS

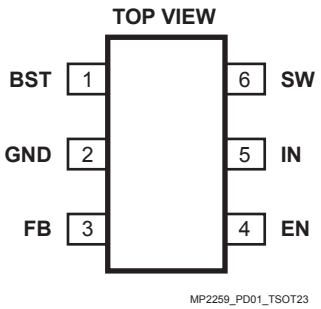
- Hand Disk Drive
- xDSL Modems Cable
- Set-Top Box

TYPICAL APPLICATION



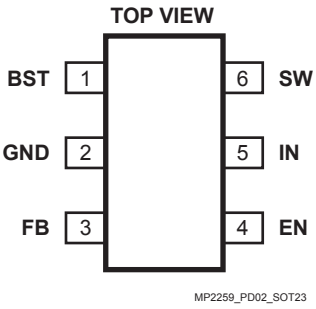


PACKAGE REFERENCE



Part Number*	Package	Temperature
MP2259DJ	TSOT23-6	–40°C to +85°C

* For Tape & Reel, add suffix –Z (eg. MP2259DJ–Z)
For RoHS compliant packaging, add suffix –LF (eg. MP2259DJ–LF–Z)



Part Number*	Package	Temperature
MP2259DT	SOT23-6	–40°C to +85°C

* For Tape & Reel, add suffix –Z (eg. MP2259DT–Z)
For RoHS compliant packaging, add suffix –LF (eg. MP2259DT–LF–Z)

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 20V
V_{SW} ..... –0.3V to V_{IN} + 0.3V
V_{BS} ..... V_{SW} + 6V
All Other Pins ..... –0.3V to +6V
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... –65°C to +150°C

Recommended Operating Conditions (2)

Supply Voltage V_{IN} ..... 4.5V to 16V
Output Voltage V_{OUT} ..... 0.81 to 14V
Operating Temperature ..... –40°C to +85°C

Thermal Resistance (3)	θ_{JA}	θ_{JC}	
TSOT23-6	220	110	°C/W
SOT23-6	220	110	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	4.5V ≤ V_{IN} ≤ 16V	0.790	0.810	0.830	V
Feedback Current	I_{FB}	V_{FB} = 0.8V		10		nA
		V_{FB} = 2V		2		µA
Switch-On Resistance (4)	$R_{DS(ON)}$			0.5		Ω
Switch Leakage		V_{EN} = 0V, V_{SW} = 0V			10	µA
Current Limit (4)				1.8		A
Oscillator Frequency	f_{SW}	V_{FB} = 0.6V		1.4		MHz
Fold-back Frequency		V_{FB} = 0V		460		KHz
Maximum Duty Cycle		V_{FB} = 0.6V		85		%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Minimum On-Time (4)	t_{ON}			100		ns
Under Voltage Lockout Threshold Rising			2.5	2.8	3.1	V
Under Voltage Lockout Threshold Hysteresis				200		mV
EN Input Low Voltage					0.4	V
En Input High Voltage			1.2			V
EN Input Current		V_{EN} = 2V		2		µA
		V_{EN} = 0V		0.1		
Supply Current (Shutdown)		V_{EN} = 0V		0.1		µA
Supply Current (Quiescent)		V_{EN} = 2V, V_{FB} = 1V			1.0	mA
Thermal Shutdown (4)				150		°C

Note:
4) Guaranteed by design.

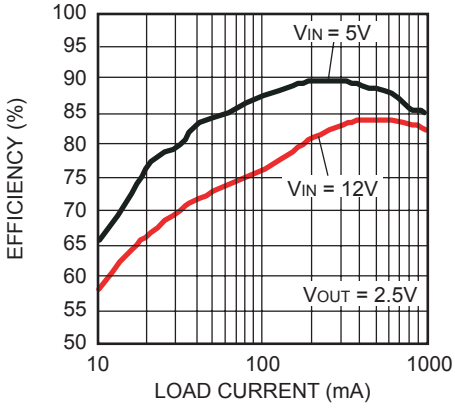
PIN FUNCTIONS

Pin #	Name	Description
1	BST	Bootstrap. This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between SW and BS pins to form a floating supply across the power switch driver.
2	GND	Ground. This pin is the voltage reference for the regulated output voltage. For this reason care must be taken in its layout. This node should be placed outside of the D1 to C1 ground path to prevent switching current spikes from inducing voltage noise into the part.
3	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 250mV.
4	EN	On/Off Control Input. Pull above 1.2V to turn the device on.
5	IN	Supply Voltage. The MP2259 operates from a +4.5V to +16V unregulated input. C1 is needed to prevent large voltage spikes from appearing at the input.
6	SW	Switch Output.

TYPICAL PERFORMANCE CHARACTERISTICS

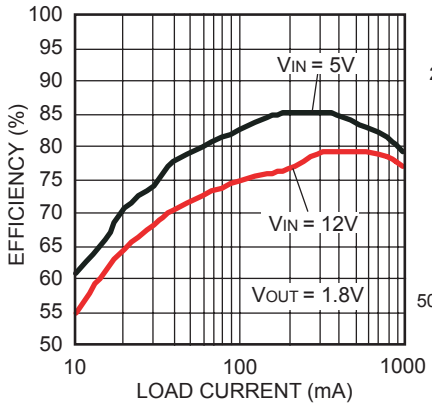
V_{IN} = 5V, V_{OUT} = 1.8V, L = 4.7µH, C1 = 4.7µF, C2 = 10µF, T_A = +25ºC, unless otherwise noted.

Efficiency vs Load Current



MP2259-TPC01

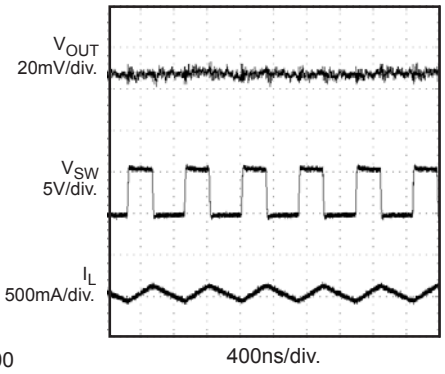
Efficiency vs Load Currents



MP2259-TPC02

Steady State Test

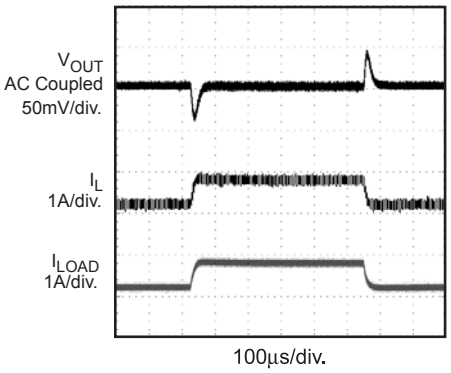
V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 0.5A



MP2259-TPC03

Load Transient Test

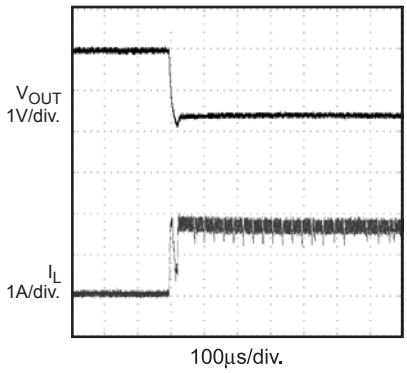
V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 0.2A to 0.8A step at 0.8A/µs



MP2259-TPC04

Short Circuit Entry

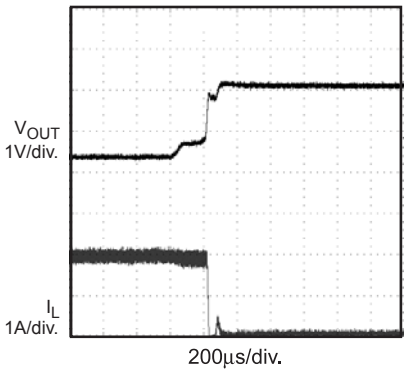
V_{IN} = 5V



MP2259-TPC05

Short Circuit Recovery

V_{IN} = 5V



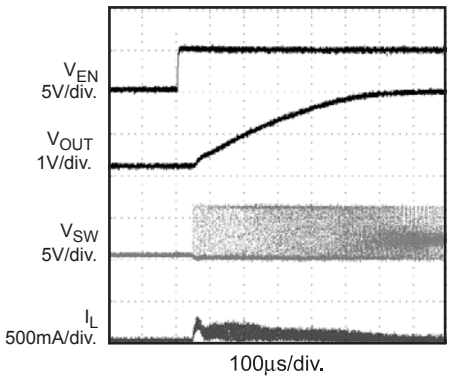
MP2259-TPC06

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 4.7µH, C1 = 4.7µF, C2 = 10µF, T_A = +25ºC, unless otherwise noted.

Start-up through Enable

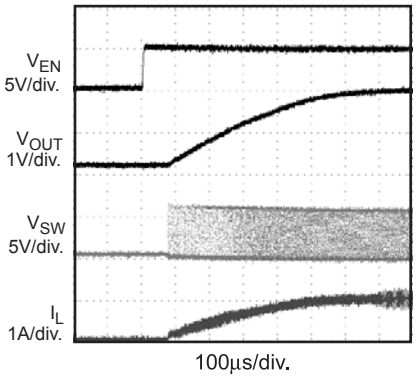
V_{IN} = 5V, V_{OUT} = 1.8V, No Load



MP2259-TPC07

Start-up through Enable

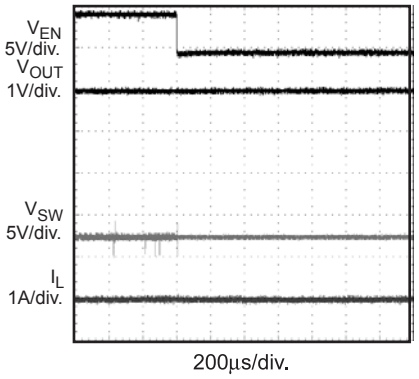
V_{IN} = 5V, V_{OUT} = 1.8V,
I_{OUT} = 1A Resistive Load



MP2259-TPC08

Shut-down through Enable

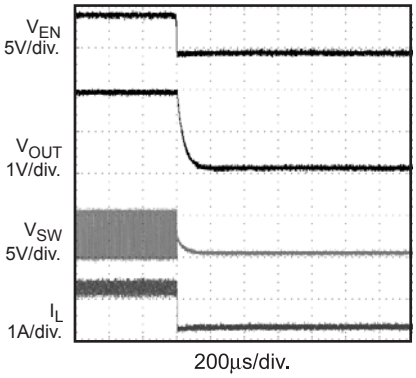
V_{IN} = 5V, V_{OUT} = 1.8V, No Load



MP2259-TPC09

Shut-down through Enable

V_{IN} = 5V, V_{OUT} = 1.8V,
I_{OUT} = 1A Resistive Load



MP2259-TPC10

OPERATION

The MP2259 is a current mode buck regulator. with EA output voltage proportional to the peak inductor current.

At the beginning of a cycle, M1 is off. The EA output voltage is higher than the current sense amplifier output, and the current comparator's output is low. The rising edge of the 1.4MHz CLK signal sets the RS Flip-Flop. Its output turns on M1 then connects the SW pin and inductor to the input supply.

The increasing inductor current is sensed and amplified by the Current Sense Amplifier. Ramp compensation is summed to Current Sense Amplifier output and compared to the Error Amplifier output by the PWM Comparator. When the sum of the Current Sense Amplifier output and the Slope Compensation signal exceeds the EA output voltage, the RS Flip-Flop is reset and M1 is turned off. The external Schottky rectifier diode (D1) conducts the inductor current.

If the sum of the Current Sense Amplifier output and the Slope Compensation signal does not exceed the EA output for a whole cycle, then the falling edge of the CLK resets the Flip-Flop.

The output of the Error Amplifier integrates the voltage difference between the feedback and the 0.8V bandgap reference. The polarity is such that a FB pin voltage lower than 0.8V increases the EA output voltage. Since the EA output voltage is proportional to the peak inductor current, an increase in its voltage increases current delivered to the output.

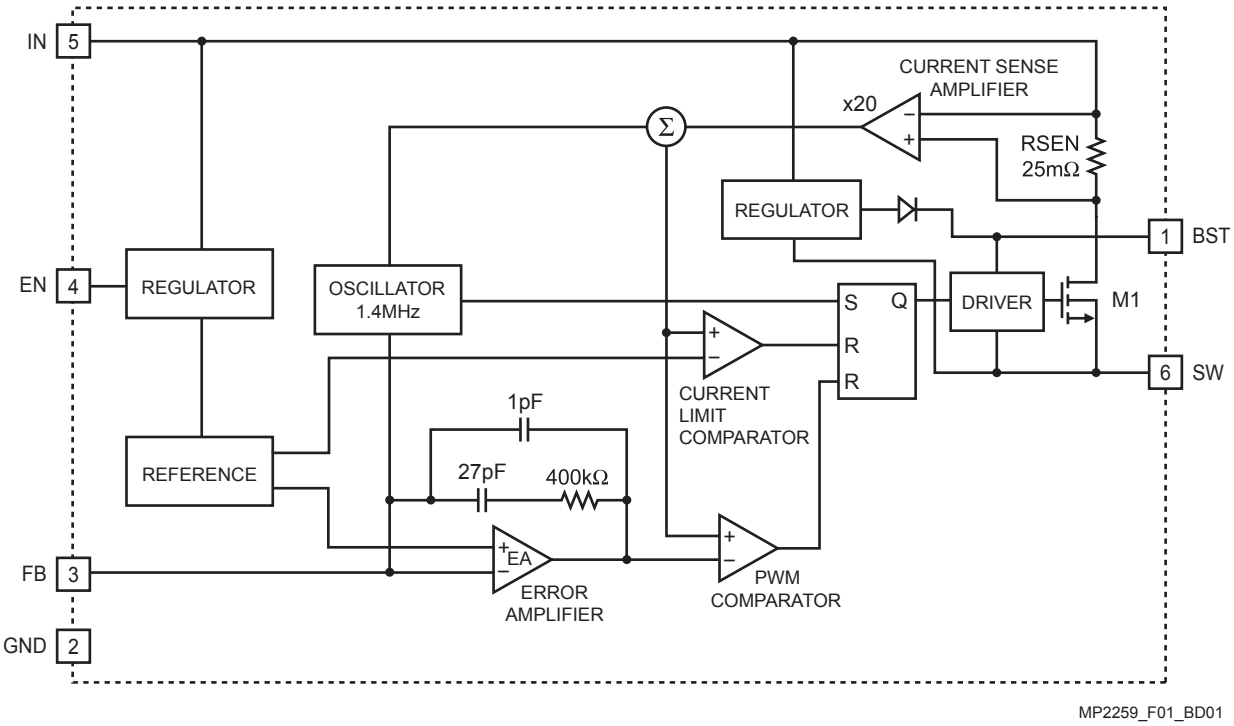


Figure 1—Functional Block Diagram

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see the schematic on front page). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Figure 1). R2 can be determined by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.81V} - 1}$$

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.8	80.6 (1%)	64.9 (1%)
2.5	49.9 (1%)	23.7 (1%)
3.3	49.9 (1%)	16.2 (1%)
5	49.9 (1%)	9.53 (1%)

Selecting the Inductor

A 1μH to 10μH inductor is recommended for most applications. For highest efficiency, the inductor's DC resistance should be less than 200mΩ. For most designs, the required inductance value can be derived from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose an inductor with a rating current higher than the maximum load current. The maximum inductor peak current can be calculated from:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, a larger inductance is recommended for improved efficiency.

Selecting the Input Capacitor

The input capacitor (C1) reduces the surge current drawn from the input and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high frequency switching current from passing through the input. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 4.7μF capacitor is sufficient.

Selecting the Output Capacitor

The output capacitor (C2) keeps output voltage ripple small and ensures loop stability. The output capacitor impedance should be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended for their low ESR characteristics. A 10μF~ 22μF capacitor is good for most applications.

PC Board Layout

The high current paths (GND, IN and SW) should be placed very close to the device with short, direct and wide traces. The input capacitor needs to be as close as possible to the IN and GND pins. The external feedback resistors should be placed next to the FB pin. Keep the switch node traces short and away from the feedback network.

External Bootstrap Diode

It is recommended that an external bootstrap diode be added when the input voltage is no greater than 5V or 5V rail is available in the system. This helps improve the efficiency of the regulator. The bootstrap diode can be a low cost one such as IN4148 or BAT54.

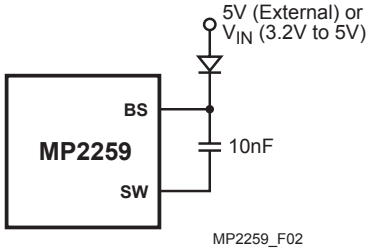
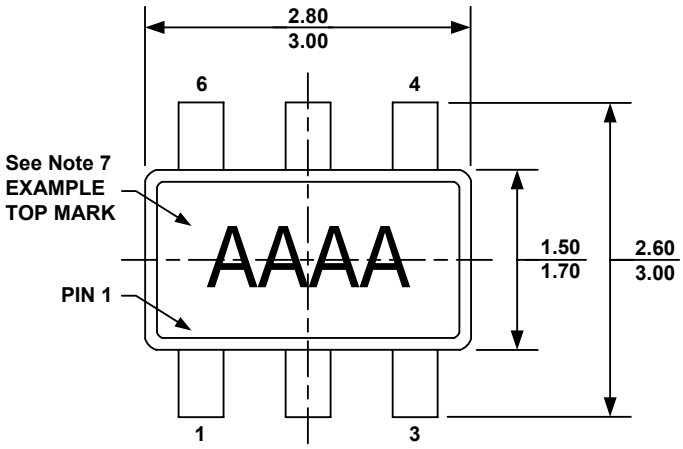


Figure 2—External Bootstrap Diode

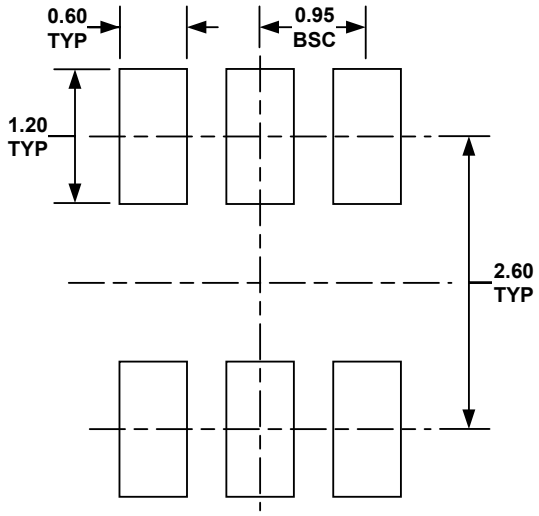
This diode is also recommended for high duty cycle operation (when $\frac{V_{OUT}}{V_{IN}}$>65%) and high output voltage (V_{OUT}>12V) applications.

PACKAGE INFORMATION

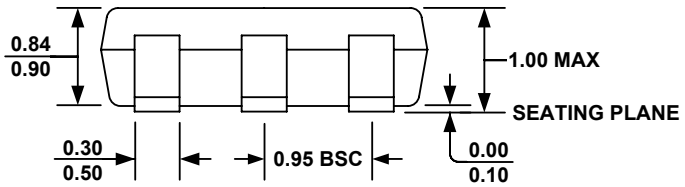
TSOT23-6



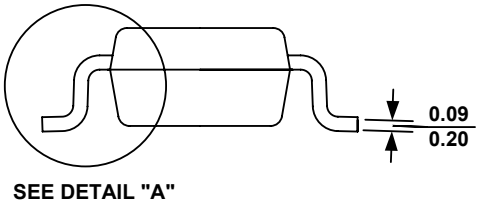
TOP VIEW



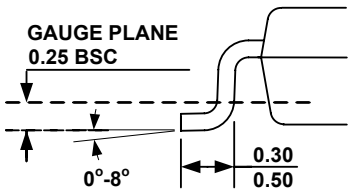
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

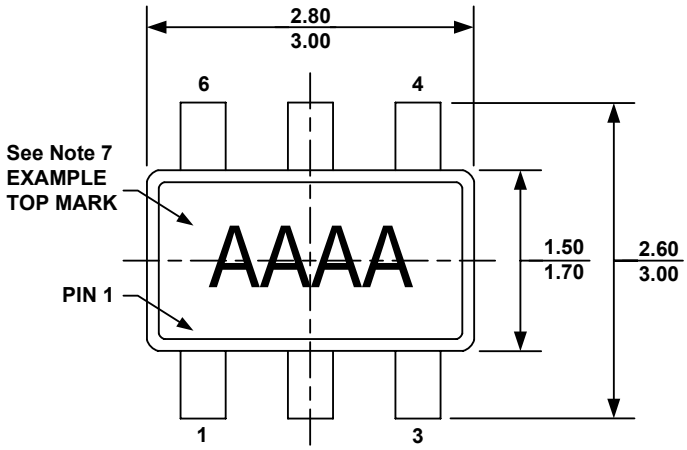


DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

SOT23-6



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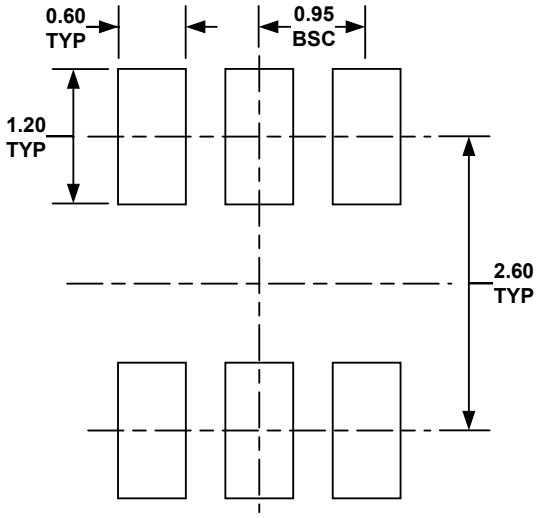

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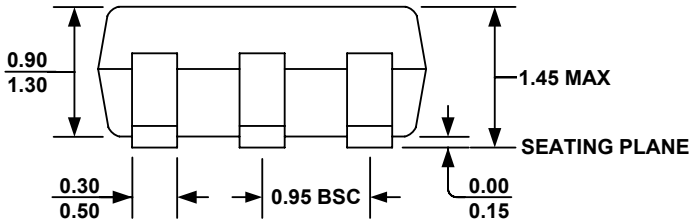
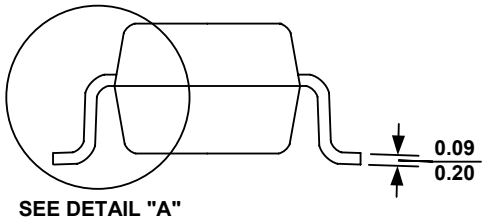
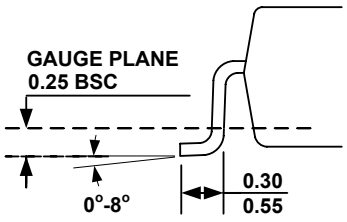


FRONT VIEW



SIDE VIEW



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