1.2.9 Understanding the Data Sheet: PowerMOS

All manufacturers of power MOSFETs provide a data sheet for every type produced. The purpose of the data sheet is primarily to give an indication as to the capabilities of a particular product. It is also useful for the purpose of selecting device equivalents between different manufacturers. In some cases however data on a number of parameters may be quoted under subtly different conditions by different manufacturers, particularly on second order parameters such as switching times. In addition the information contained within the data sheet does not always appear relevant for the application. Using data sheets and selecting device equivalents therefore requires caution and an understanding of exactly what the data means and how it can be interpreted. Throughout this chapter the BUK553-100A is used as an example, this device is a 100 V logic level MOSFET.

Information contained in the Philips data sheet

The data sheet is divided into 8 sections as follows:

* Quick reference data
* Limiting values
* Thermal resistances
* Static characteristics
* Dynamic characteristics
* Reverse diode limiting values and characteristics
* Avalanche limiting value
* Graphical data

The information contained within each of these sections is now described.

Quick reference data

This data is presented for the purpose of quick selection. It lists what is considered to be the key parameters of the device such that a designer can decide at a glance whether the device is likely to be the correct one for the application or not. Five parameters are listed, the two most important are the drain-source voltage V_{DS} and drain-source on-state resistance, $R_{DS(ON)}$. V_{DS} is the maximum voltage the device will support between drain and source terminals in the off-state. $R_{DS(ON)}$ is the maximum on-state resistance at the quoted gate voltage, V_{GS}, and a junction temperature of 25 ˚C. (NB $R_{DS(ON)}$ is temperature dependent, see static characteristics). It is these two parameters which provide a first order indication of the devices capability.

A drain current value (I_D) and a figure for total power dissipation are also given in this section. These figures should be treated with caution since they are quoted for conditions that are rarely attainable in real applications. (See limiting values.) For most applications the usable dc current will be less than the quoted figure in the quick reference data. Typical power dissipations that can be tolerated by the majority of designers are less than 20 W (for discrete devices), depending on the heatsinking arrangement used. The junction temperature (T_J) is usually given as either 150 ˚C or 175 ˚C. It is not recommended that the internal device temperature be allowed to exceed this figure.

Limiting values

This table lists the absolute maximum values of six parameters. The device may be operated right up to these maximum levels however they must not be exceeded, to do so may incur damage to the device.

Drain-source voltage and drain-gate voltage have the same value. The figure given is the maximum voltage that may be applied between the respective terminals. Gate-source voltage, $\pm V_{GS}$, gives the maximum value that may be allowed between the gate and source terminals. To exceed this voltage, even for the shortest period can cause permanent damage to the gate oxide. Two values for the dc drain current, I_D, are quoted, one at a mounting base temperature of 25 ˚C and one at a mounting base temperature of 100 ˚C. Again these currents do not represent attainable operating levels. These currents are the values that will cause the junction temperature to reach its maximum value when the mounting base is held at the quoted value. The maximum current rating is therefore a function of the mounting base temperature and the quoted figures are just two points on the derating curve ,see Fig.1.

The third current level quoted is the pulse peak value, I_{DM}. PowerMOS devices generally speaking have a very high peak current handling capability. It is the internal bond wires which connect to the chip that provide the final limitation. The pulse width for which I_{DM} can be applied depends upon the thermal considerations (see section on calculating currents.) The total power dissipation, P_{tot}, and maximum junction temperature are also stated as for the quick reference data. The P_{tot} figure is calculated from the simple quotient given in equation 1 (see section on safe operating area). It is quoted for the condition where the mounting base temperature is maintained at 25 ˚C. As an example, for the BUK553-100A the P_{tot} figure is 75 W, dissipating this amount of power while maintaining the mounting base at 25 ˚C would be a challenge! For higher mounting base temperatures the total power that can be dissipated is less.

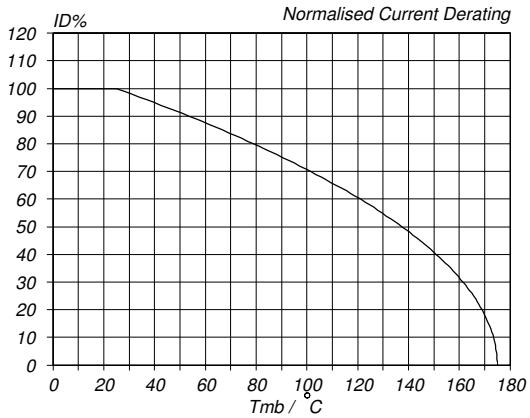

Fig.1 Normalised continuous drain current.
ID% = 100 . $I_D/I_{D25\,°C}$ = f(T_{mb}); conditions: $V_{GS} \geq 5$ V

Obviously if the mounting base temperature was made equal to the max permitted junction temperature, then no power could be dissipated internally. A derating curve is given as part of the graphical data, an example is shown in Fig.2 for a device with a limiting T_j of 175 ˚C.

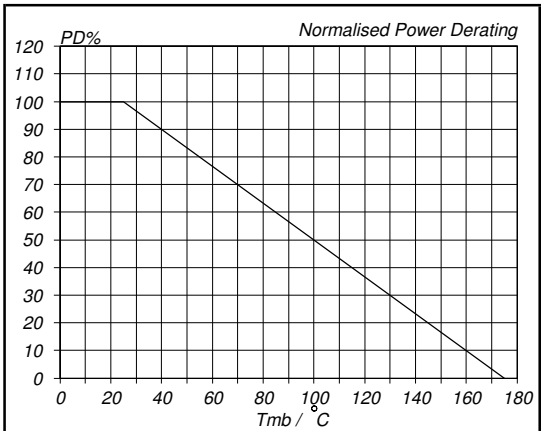

Fig.2 Normalised power dissipation.
PD% = 100 $P_D/P_{D\,25\,°C}$ = f(T_{mb})

Storage temperature limits are also quoted, usually between -40 /-55 ˚C and +150 /+175 ˚C. Both the storage temperature limits and the junction temperature limit are figures at which extensive reliability work is performed by our Quality department. To exceed these figures will cause a reduction in long-term reliability.

Thermal resistance.

For non-isolated packages two thermal resistance values are given. The value from junction to mounting base ($R_{thj\text{-}mb}$) indicates how much the junction temperature will be raised above the temperature of the mounting base when dissipating a given power. Eg a BUK553-100A has a $R_{thj\text{-}mb}$ of 2 K/W, dissipating 10 W, the junction temperature will be 20 ˚C above the temperature of its mounting base. The other figure quoted is from junction to ambient. This is a much larger figure and indicates how the junction temperature will rise if the device is NOT mounted on a heatsink but operated in free air. Eg for a BUK553-100A, $R_{thj\text{-}a}$ = 60 K/W, dissipating 1 W while mounted in free air will produce a junction temperature 60 ˚C above the ambient air temperature.

For isolated packages, (F-packs) the mounting base (the metal plate upon which the silicon chip is mounted) is fully encapsulated in plastic. Therefore it is not possible to give a thermal resistance figure junction to mounting base. Instead a figure is quoted from junction to heatsink, $R_{thj\text{-}hs}$, which assumes the use of heatsink compound. Care should be taken when comparing thermal resistances of isolated and non-isolated types. Consider the following example:

The non-isolated BUK553-100A has a $R_{thj\text{-}mb}$ of 2 K/W. The isolated BUK543-100A has a $R_{thj\text{-}hs}$ of 5 K/W. These devices have identical crystals but mounted in different packages. At first glance the non-isolated type might be expected to offer much higher power (and hence current) handling capability. However for the BUK553-100A the thermal resistance junction to heatsink has to be calculated, this involves adding the extra thermal resistance between mounting base and heatsink. For most applications some isolation is used, such as a mica washer. The thermal resistance mounting base to heatsink is then of the order 2 K/W. The total thermal resistance junction to heatsink is therefore

$R_{thj\text{-}hs}$ (non isolated type) = $R_{thj\text{-}mb}$ + $R_{thmb\text{-}hs}$ = 4 K/W

It can be seen that the real performance difference between the isolated and non isolated types will not be significant.

Static Characteristics

The parameters in this section characterise breakdown voltage, threshold voltage, leakage currents and on-resistance.

A drain-source breakdown voltage is specified as greater than the limiting value of drain-source voltage. It can be measured on a curve tracer, with gate terminal shorted to the source terminal, it is the voltage at which a drain current of 250 µA is observed. Gate threshold voltage, $V_{GS(TO)}$, indicates the voltage required on the gate (with respect to the source) to bring the device into its conducting state. For logic level devices this is usually between 1.0 and 2.0 V and for standard devices between 2.1 and 4 V.

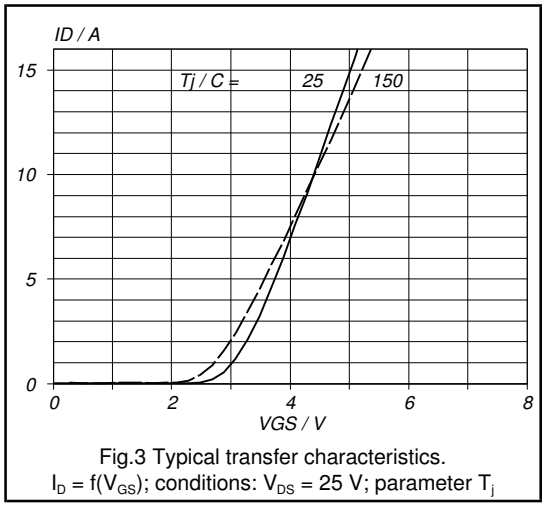

Fig.3 Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

Useful plots in the graphical data are the typical transfer characteristics (Fig.3) showing drain current as a function of V_{GS} and the gate threshold voltage variation with junction temperature (Fig.4). An additional plot also provided is the sub-threshold conduction, showing how the drain current varies with gate-source voltage below the threshold level (Fig.5).

Off-state leakage currents are specified for both the drain-source and gate-source under their respective maximum voltage conditions. Note, although gate-source leakage current is specified in nano-amps, values are typically of the order of a few pico-amps.

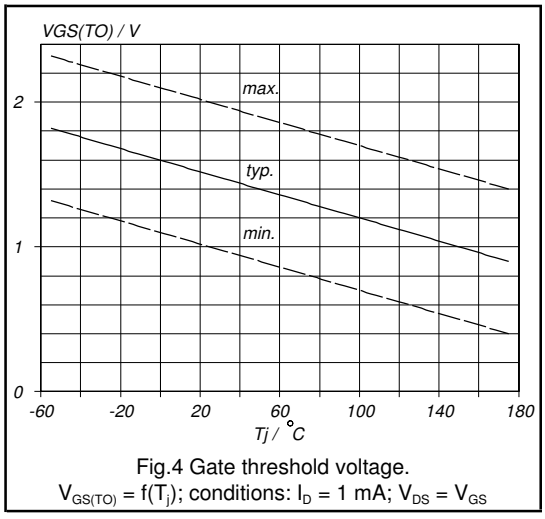

Fig.4 Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

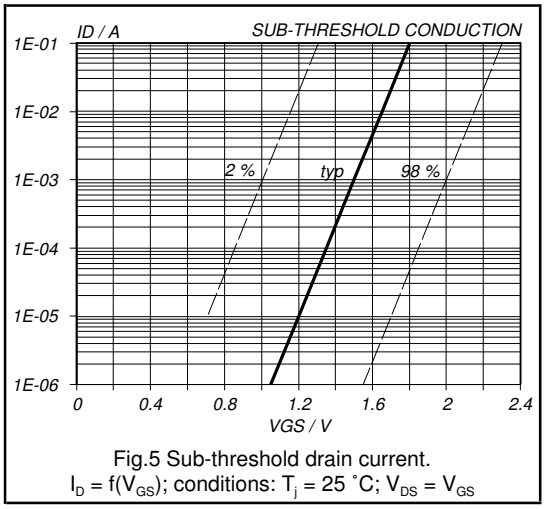

Fig.5 Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

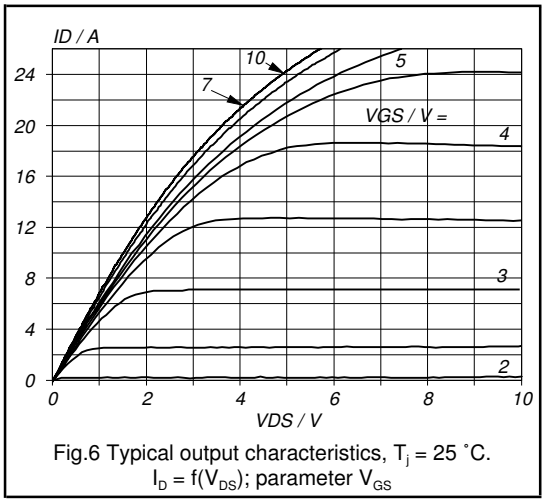

Fig.6 Typical output characteristics, T_j = 25 ˚C.
$I_D = f(V_{DS})$; parameter V_{GS}

The drain-source on-resistance is very important. It is specified at a gate-source voltage of 5 V for logic level FETs and 10 V for a standard device. The on-resistance for a standard MOSFET cannot be reduced significantly by increasing the gate source voltage above 10 V. Reducing the gate voltage will however increase the on-resistance. For the logic level FET, the on-resistance is given for a gate voltage of 5 V, a further reduction is possible however at gate voltages up to 10 V, this is demonstrated by the output characteristics, Fig.6 and on-resistance characteristics, Fig.7 for a BUK553-100A. .

The on-resistance is a temperature sensitive parameter, between 25 ˚C and 150 ˚C it approximately doubles in value. A plot of normalised $R_{DS(ON)}$ versus temperature (Fig.8) is included in each data sheet. Since the MOSFET will normally operate at a T_j higher than 25 ˚C, when making estimates of power dissipation in the MOSFET, it is important to take into account the higher $R_{DS(ON)}$.

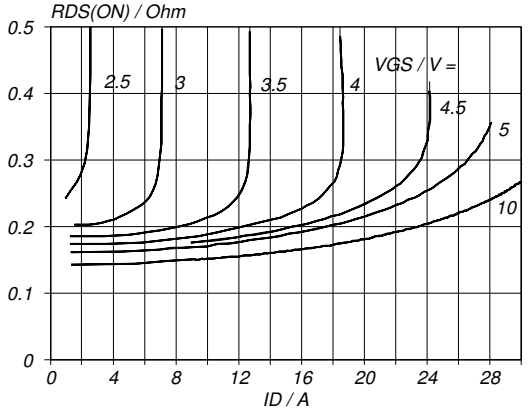

Fig.7 Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

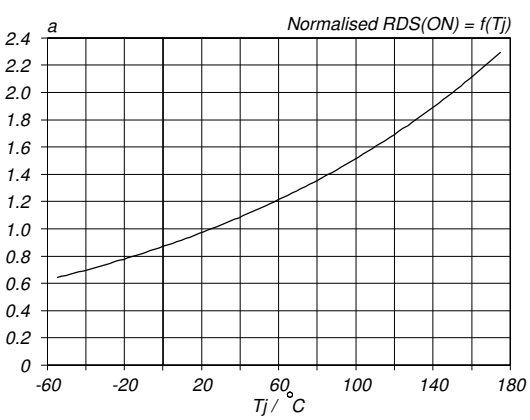

Fig.8 Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; I_D = 6.5 A; V_{GS} = 5 V

Dynamic Characteristics

These include transconductance, capacitance and switching times. Forward transconductance, g_{fs}, is essentially the gain parameter which indicates the change in drain current that will result from a fluctuation in gate voltage when the device is saturated. (NB saturation of a MOSFET refers to the flat portion of the output characteristics.) Fig.9 shows how g_{fs} varies as a function of the drain current for a BUK553-100A.

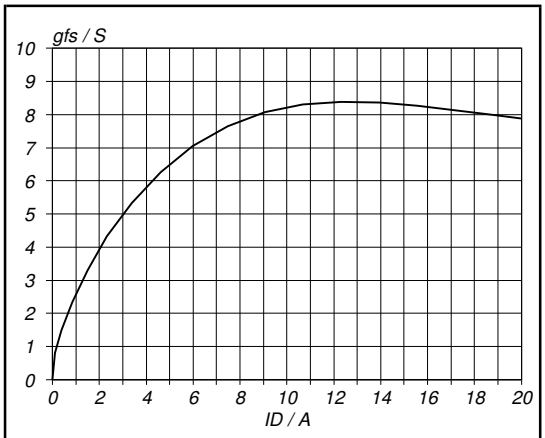

Fig.9 Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

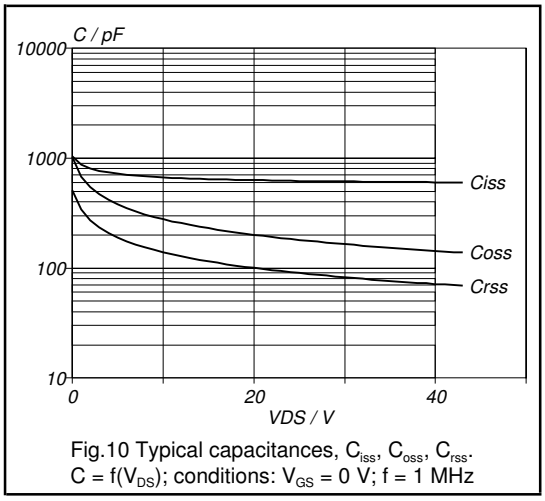

Fig.10 Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

Capacitances are specified by most manufacturers, usually in terms of input, output and feedback capacitance. The values quoted are for a drain-source voltage of 25 V. However this is only part of the story as the MOSFET capacitances are strongly voltage dependent, increasing as drain-source voltage is reduced. Fig.10 shows how these capacitances vary with voltage. The usefulness of the capacitance figures is limited. The input capacitance value gives only a rough indication of the charging required by the drive circuit. Perhaps more useful is the gate charge information an example of which is shown in Fig.11. This plot shows how much charge has to be input to the gate to

reach a particular gate-source voltage. Eg. to charge a BUK553-100A to V_{GS} = 5 V, starting from a drain-source voltage of 80 V, requires 12.4 nc. The speed at which this charge is to be applied will give the gate circuit current requirements. More information on MOSFET capacitance is given in chapter 1.2.2.

Resistive load switching times are also quoted by most manufacturers, however extreme care should be taken when making comparisons between different manufacturers data. The speed at which a power MOSFET can be switched is essentially limited only by circuit and package inductances. The actual speed in a circuit is determined by how fast the internal capacitances of the MOSFET are charged and discharged by the drive circuit. The switching times are therefore extremely dependent on the circuit conditions employed; a low gate drive resistance will provide for faster switching and vice-versa. The Philips data sheet presents the switching times for all PowerMOS with a resistor between gate and source of 50 Ω. The device is switched from a pulse generator with a source impedance also of 50 Ω. The overall impedance of the gate drive circuit is therefore 25 Ω.

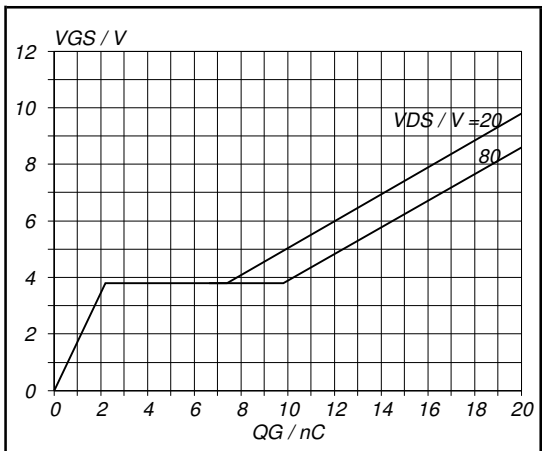

Fig.11 Typical turn-on gate-charge characteristics.
V_{GS} = f(Q_G); conditions: I_D = 13 A; parameter V_{DS}

Also presented under dynamic characteristics are the typical inductances of the package. These inductances become important when very high switching speeds are employed such that large dI/dt values exist in the circuit. Eg. turning-on 30 A within 60 ns gives a dI/dt of 0.5 A/ns. The typical inductance of the source lead is 7.5 nH, from V = -L*dI/dt the potential drop from the source bond pad (point where the source bond wire connects to the chip internally) to the bottom of the source lead would be 3.75 V. Normally a standard device will be driven with a gate-source voltage of 10 V applied across the gate and source terminals, the actual voltage gate to source on the semiconductor however would only be 6.25 V during the turn-on period! The switching speed is therefore ultimately limited by package inductance.

Reverse diode limiting values and characteristics

The reverse diode is inherent in the vertical structure of the power MOSFET. In some circuits this diode is required to perform a useful function. For this reason the characteristics of the diode are specified. The forward currents permissible in the diode are specified as 'continuous reverse drain current' and 'pulsed reverse drain current'. The forward voltage drop of the diode is also provided together with a plot of the diode characteristic, Fig.12. The switching capability of the diode is given in terms of the reverse recovery parameters, t_{rr} and Q_{rr}.

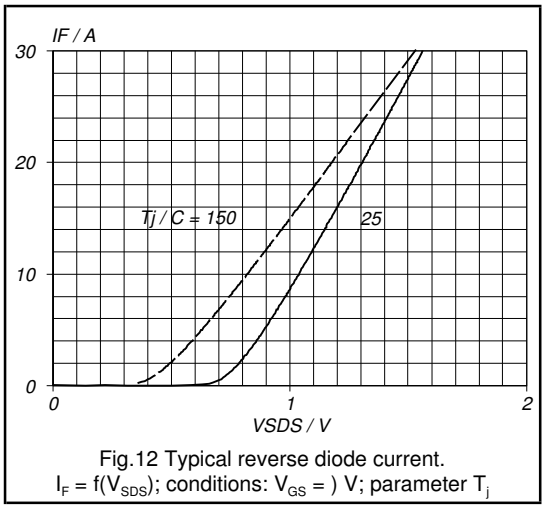

Fig.12 Typical reverse diode current.
I_F = f(V_{SDS}); conditions: V_{GS} =) V; parameter T_j

Because the diode operates as a bipolar device it is subject to charge storage effects. This charge must be removed for the diode to turn-off. The amount of charge stored is given by Q_{rr}, the reverse recovery charge, the time taken to extract the charge is given by t_{rr}, the reverse recovery time. NB. trr depends very much on the -dI_f/dt in the circuit, t_{rr} is specified in data at 100 A/µs.

Avalanche limiting value

This parameter is an indication as to the ruggedness of the product in terms of its ability to handle a transient overvoltage, ie the voltage exceeds the drain-source voltage limiting value and causes the device to operate in an avalanche condition. The ruggedness is specified in terms of a drain-source non-repetitive unclamped inductive turn-off energy at a mounting base temperature of 25 ˚C. This energy level must be derated at higher mounting base temperatures as shown in Fig.13. NB. this rating is

non-repetitive which means the circuit should not be designed to force the PowerMOS repeatedly into avalanche. This rating is only to permit the device to survive if exceptional circuit conditions arise such that a transient overvoltage occurs.

The new generation of Philips Medium Voltage MOSFETs also feature a repetitive ruggedness rating. This rating is specified in terms of a drain-source repetitive unclamped inductive turn-off energy at a mounting base temperature of 25 ˚C, and indicates that the devices are able to withstand repeated momentary excursions into avalanche breakdown provided the maximum junction temperature is not exceeded. (A more detailed explanation of Ruggedness is given in chapter 1.2.7.)

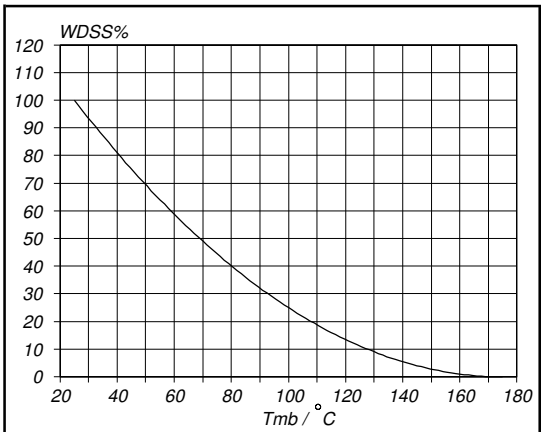

Fig.13. Normalised avalanche energy rating.
W_{DSS}% = f(T_{mb}); conditions: I_D = 13 A

Safe Operating Area

A plot of the safe operating area is presented for every PowerMOS type. Unlike bipolar transistors a PowerMOS exhibits no second breakdown mechanism. The safe operating area is therefore simply defined from the power dissipation that will cause the junction temperature to reach the maximum permitted value.

Fig.14 shows the SOA for a BUK553-100. The area is bounded by the limiting drain source voltage, limiting current values and a set of constant power curves for various pulse durations. The plots in data are all for a mounting base temperature of 25 ˚C. The constant power curves therefore represent the power that raises the junction temperature by an amount T_{jmax} - T_{mb}, ie. 150 ˚C for a device with a limiting T_j of 175 ˚C and 125 ˚C for a device with a limiting T_j of 150 ˚C. . Clearly in most applications the mounting base temperature will be higher than 25 ˚C, the SOA would therefore need to be reduced. The maximum power curves are calculated very simply.

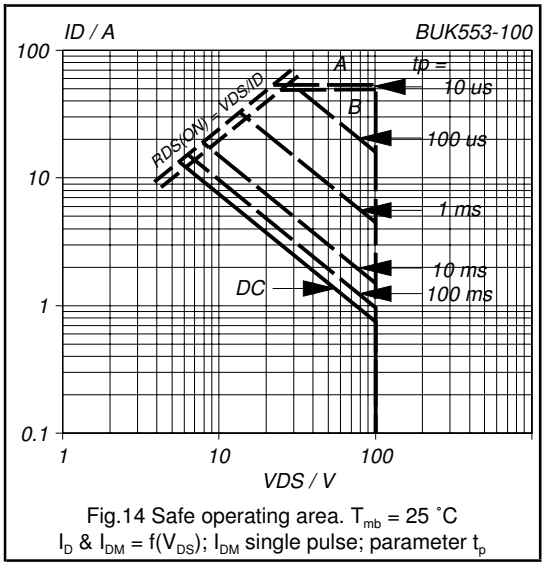

Fig.14 Safe operating area. T_{mb} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

The dc curve is based upon the thermal resistance junction to mounting base (junction to heatsink in the case of isolated packages), which is substituted into equation 1. The curves for pulsed operation assume a single shot pulse and instead of thermal resistance, a value for transient thermal impedance is used. Transient thermal impedance is supplied as graphical data for each type, an example is shown in Fig.15. For calculation of the single shot power dissipation capability, a value at the required pulse width is read from the D = 0 curve and substituted in to equation 2. (A more detailed explanation of transient thermal impedance and how to use the curves can be found in chapter 7.)

$$P_{tot(dc)} = \frac{T_{jmax} - T_{mb}}{R_{thj-mb}} \quad 1$$

$$P_{tot(pulse)} = \frac{T_{jmax} - T_{mb}}{Z_{thj-mb}} \quad 2$$

Examples of how to calculate the maximum power dissipation for a 1 ms pulse are shown below. Example 1 calculates the maximum power assuming a T_j of 175 ˚C and T_{mb} of 25 ˚C. This power equates to the 1 ms curve on the SOA plot of Fig.14. Example 2 illustrates how the power capability is reduced if T_{mb} is greater than 25 ˚C.

Example 1: 1 ms pulse at 25 ˚C for a BUK553-100A

Z_{th} = 0.32 K/W, T_{jmax} = 175 ˚C, T_{mb} = 25 ˚C

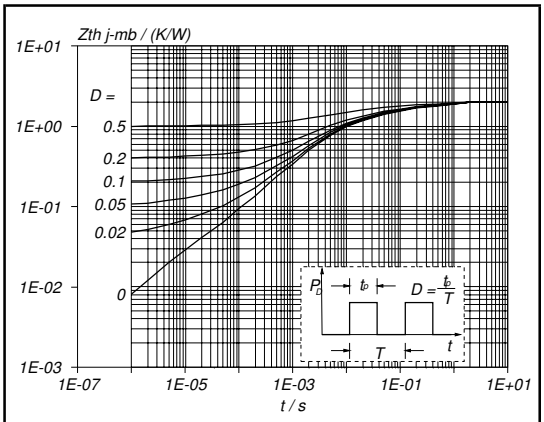

Fig.15 Transient thermal impedance.
$Z_{thj\text{-}mb}$ = f(t); parameter D = t_p/T

$$P_{\max(1\,ms\,pulse)} = \frac{175-25}{0.32} = 469\,W$$

The 469 W line is observed on Fig.13, (4.69 A @ 100 V and 15.6 A @ 30 V etc)

Example 2: 1 ms pulse at 75 ˚C for a BUK553-100A

Z_{th} = 0.32 K/W, T_{jmax} = 175 ˚C, T_{mb} = 75 ˚C

$$P_{\max(1\,ms\,pulse)} = \frac{175-75}{0.32} = 312\,W$$

Therefore with a mounting base temperature of 75 ˚C the maximum permissible power dissipation is reduced by one third compared with the 25 ˚C value on the SOA plot.

Calculating Currents

The current ratings quoted in the data sheet are derived directly from the maximum power dissipation.

$$I_D(@T_{mb})^2 \cdot R_{DS(ON)}(@T_{jmax}) = P_{tot} \qquad 3$$

substituting for P_{tot} from equation 1

$$I_D(@T_{mb}) = \left\{ \frac{T_{jmax} - T_{mb}}{R_{thj-mb} \cdot R_{DS(ON)}(@T_{jmax})} \right\}^{\frac{1}{2}} \qquad 4$$

To calculate a more realistic current it is necessary to replace T_{jmax} in equation 4 with the desired operating junction temperature and T_{mb} with a realistic working value. It is generally recommended that devices are not operated continuously at T_{jmax}. For reasons of long term reliability, 125 ˚C is a more suitable junction operating temperature. A value of T_{mb} between 75 ˚C and 110 ˚C is also a more typical figure.

As an example a BUK553-100A is quoted as having a dc current rating of 13 A. Assuming a T_{mb} of 100 ˚C and operating T_j of 125 ˚C the device current is calculated as follows:

From Fig.8

$$R_{DS(ON)}(@\,125^oC) = 1.75 \cdot R_{DS(ON)}(@\,25^oC) = 1.75 \cdot 0.18 = 0.315\,\Omega$$

$R_{thj\text{-}mb}$ = 2 K/W, using equation 4

$$I_D = \left\{ \frac{25}{2 \cdot 0.315} \right\}^{\frac{1}{2}} = 6.3\,A$$

The device could therefore conduct 6.3 A under these conditions which equates to a 12.5 W power dissipation.

Conclusions

The most important information presented in the data sheet is the on-resistance and the maximum voltage drain-source. Current values and maximum power dissipation values should be viewed carefully since they are only achievable if the mounting base temperature is held to 25 ˚C. Switching times are applicable only for the specific conditions described in the data sheet, when making comparisons between devices from different manufacturers, particular attention should be paid to these conditions.