The World Leader in High Performance Signal Processing Solutions

PC Board Layout Techniques for FAEs

High Speed, Mixed-Signal & Low Level Applications

ANALOG DEVICES

The Art of PCB Design

- **Good PCB design is a discipline that takes years to master.**
- **Reliable High-speed, mixed-signal designs require a great deal of theoretical knowledge and practical understanding to be done properly.**
- **We'll cover many important concepts at a high level today.**

Agenda

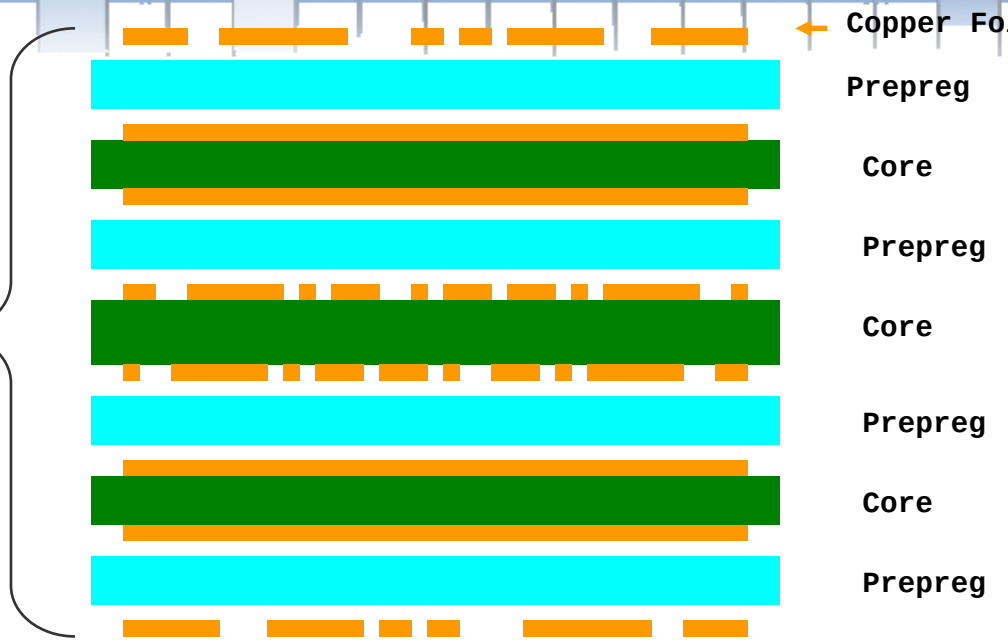
- **PCBs 101**
- **Good High-Speed PCB Design Practices**
  - The Power of Power and Ground planes
  - Proper use of decoupling capacitors
  - The True Nature of Resistors and Capacitors in High-speed Designs
  - High-speed Signal Propagation - Wires or Transmission Lines?
  - Impedance Mismatches, Series and Parallel Termination
  - Managing EMI
- **Mixed Signal PCB Layout**
  - Grounding Mixed Signal Data Acquisition System
  - Ground Plane in Mixed Signal Designs
  - Power Filtering & decoupling
  - Parasitic Consideration
  - Control Differential line impedance
- **Small Signal Layout**
  - Consider Track Resistor Loss
  - Proper grounding shielding cable
  - Minimize PCB Leakage by Guard Ring
  - Prevent PCB Heating Temperature Sensors

PCB Units of Measurement

- **PCB methodologies originated in the United States**
- **Units of measurement are therefore typically in Imperial units, not SI/metric units.**
  - **Board dimensions are commonly measured in inches.**
  - **Dielectric thickness & conductor length and width typically measured in inches and "mils".**
    - 1 mil = 0.001 inches
    - 1 mil = .0254 mm
  - **Conductor thickness measured in ounces (oz).**
    - The weigh of conductor metal in a square foot of material.
    - Typical thickness
      - 0.5oz = 17.5µm
      - 1.0oz = 35.0µm
      - 2.0oz = 70.0µm
      - 3.0oz = 105.0µm

PCB Basics
PCB Stack-up

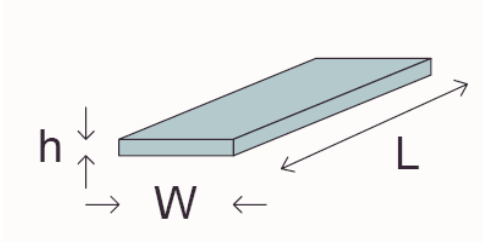
Cross Section of a typical 8-layer stack-up



- **A PCB consists of alternating layers of prepreg and core materials**
- **Materials:**
  - **Core: A thin piece of *cured* dielectric (usually FR4 : fiberglass & epoxy)**
  - **Prepreg: Short for preimpregnated. A thin piece of *uncured* dielectric (usually "FR4" : fiberglass-epoxy). Prepreg melts into an epoxy glue when heated and pressed, and then hardens / cures with the same dielectric constant as the core material.**
  - **Copper Foil : Thin piece of copper that is bonded / laminated to both sides of the core using epoxy resin.**
- **The number of layers of copper foil corresponds to the "layers of the PCB"**
  - **An 8-layer PCB has 8 layers of copper foil.**
- **Stack-up is symmetrical about the center of the board in the vertical axis to avoid mechanical stress in the board under thermal cycling.**

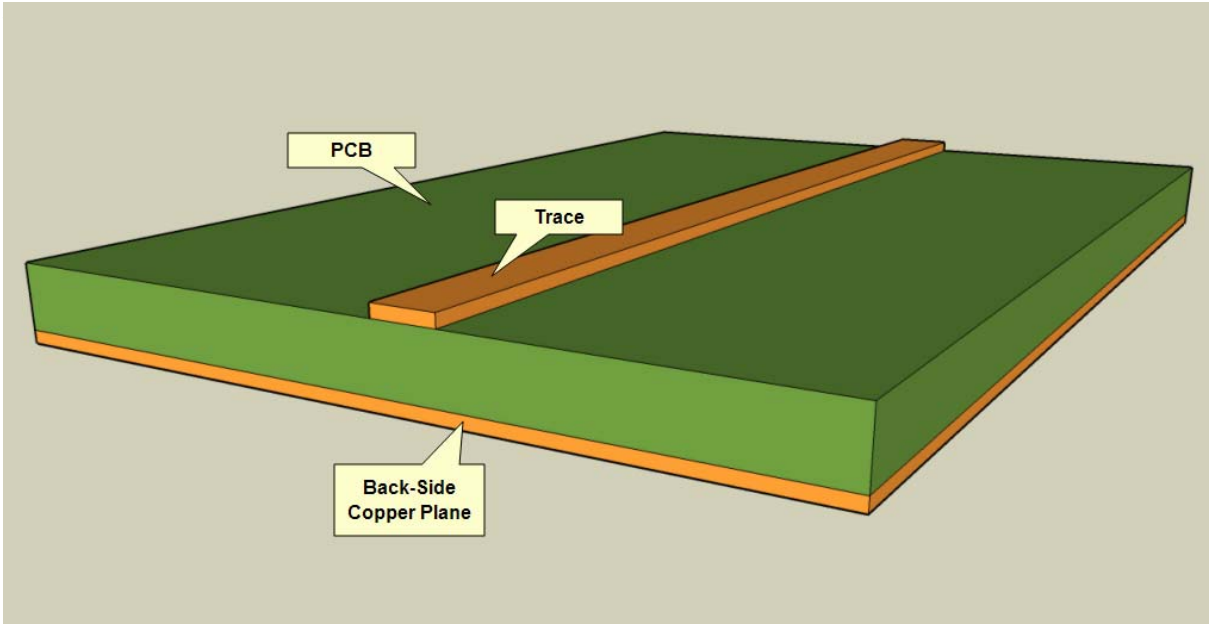
PCB (Printed Circuit Board) Anatomy

PCB Conductors : Traces



$$R = \frac{\rho \cdot L}{A} = \frac{\rho \cdot L}{h \cdot W} = Rs\frac{L}{W}$$

Cu resistivity: ρ=1.7E10-8Ωm



Source: http://circuitcalculator.com/wordpress/wp-content/uploads/2007/04/pcb-trace-geometry-1.png

- **Copper (Cu) is the most commonly used conductor in PCBs.**
  - **Traces and/or connectors may be plated in nickel followed by gold to provide a corrosion-resistant electrically conductive.**
- **Trace Width (W) and Length (L) – controlled by PCB layout engineer**
  - **Width and spacing between traces typically ≥5 mil in common fabrication processes**
- **Trace Thickness (h) – variable of fabrication process**
  - **Typically 0.5oz – 3oz**
  - **Trend towards 0.25oz**
- **Signal Integrity Tip: All of the above affect the resistance, capacitance and impedance of the trace and must be well understood for high-speed design.**

PCB Basics

PCB Conductors : Power Planes

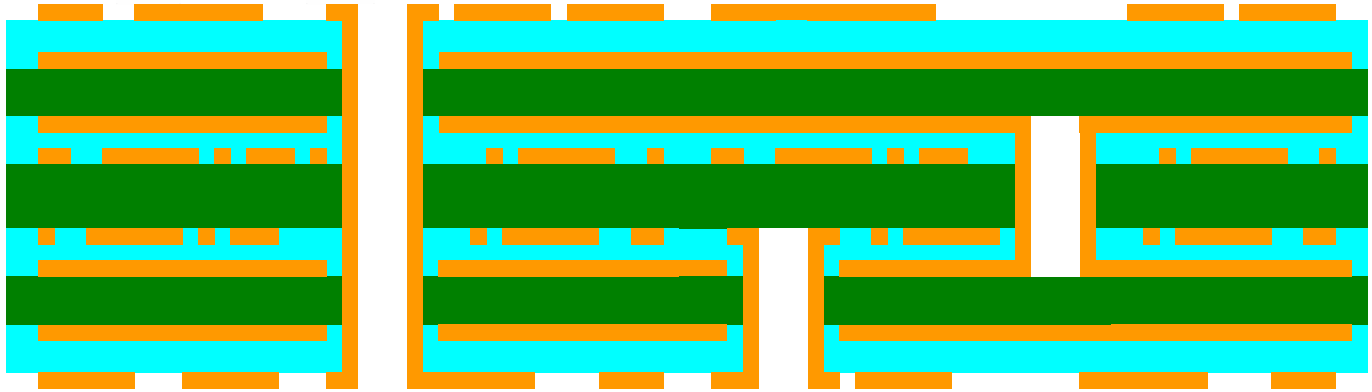
- **Power Planes**
  - A solid layer of copper used to provide power or ground.
  - Typically use thicker copper layer than signal layers to reduce resistance.
- **Why are they needed?**
  - Provide a stable, low-impedance path for power and ground signals to all devices on the PCB
  - Shield signals between layers to minimize cross-talk
- **Signal Integrity Tip: By placing power and ground on opposite sides of thin core material, we can maximize the "intra-plane capacitance". Also, this minimizes PCB warping.**

PCB Basics
PCB Insulators / Dielectrics

- **Common Dielectric Materials**
  - **FR-4 (Woven fiberglass and epoxy)**
    - Most commonly used, widely available, relatively low-cost
    - Dielectric constant (permittivity) : 4.70 Max, 4.35 @ 500 MHz, 4.34 @ 1 GHz
      - Acceptable for signals up to about 2 GHz (loss and cross-talk will increase beyond this)
    - Fairly rigid (17 GPa using Young's modulus)
  - **FR-2 (Phenolic cotton paper)**
    - Very low-cost, used in cheap consumer devices.
    - Susceptible to cracking
    - Dielectric constant (permittivity) : 4.5 @ 1 GHz
  - **CEM-3 (Woven glass and epoxy)**
    - Very similar to FR4, widely used in Japan
  - **Polyimide**
    - Good performance at high frequencies
  - **FR & CEM**
    - FR : Flame Retardant
    - CEM : Composite Epoxy Material
- **Signal Integrity Tip: Most PCB insulator materials support a relatively controlled dielectric - this is important for maintaining a constant impedance for transmission lines!**
  - **More on this soon**

Material	Dielectric constant
Vacuum	1 (by definition)
Air	1.00054
Teflon™	2.1
Polyethylene	2.25
Polystyrene	2.4–2.7
Paper	3.5
Silicon dioxide	3.7
Concrete	4.5
Pyrex (glass)	4.7 (3.7–10)
Rubber	7
Diamond	5.5–10
Salt	3–15
Graphite	10–15
Silicon	11.68

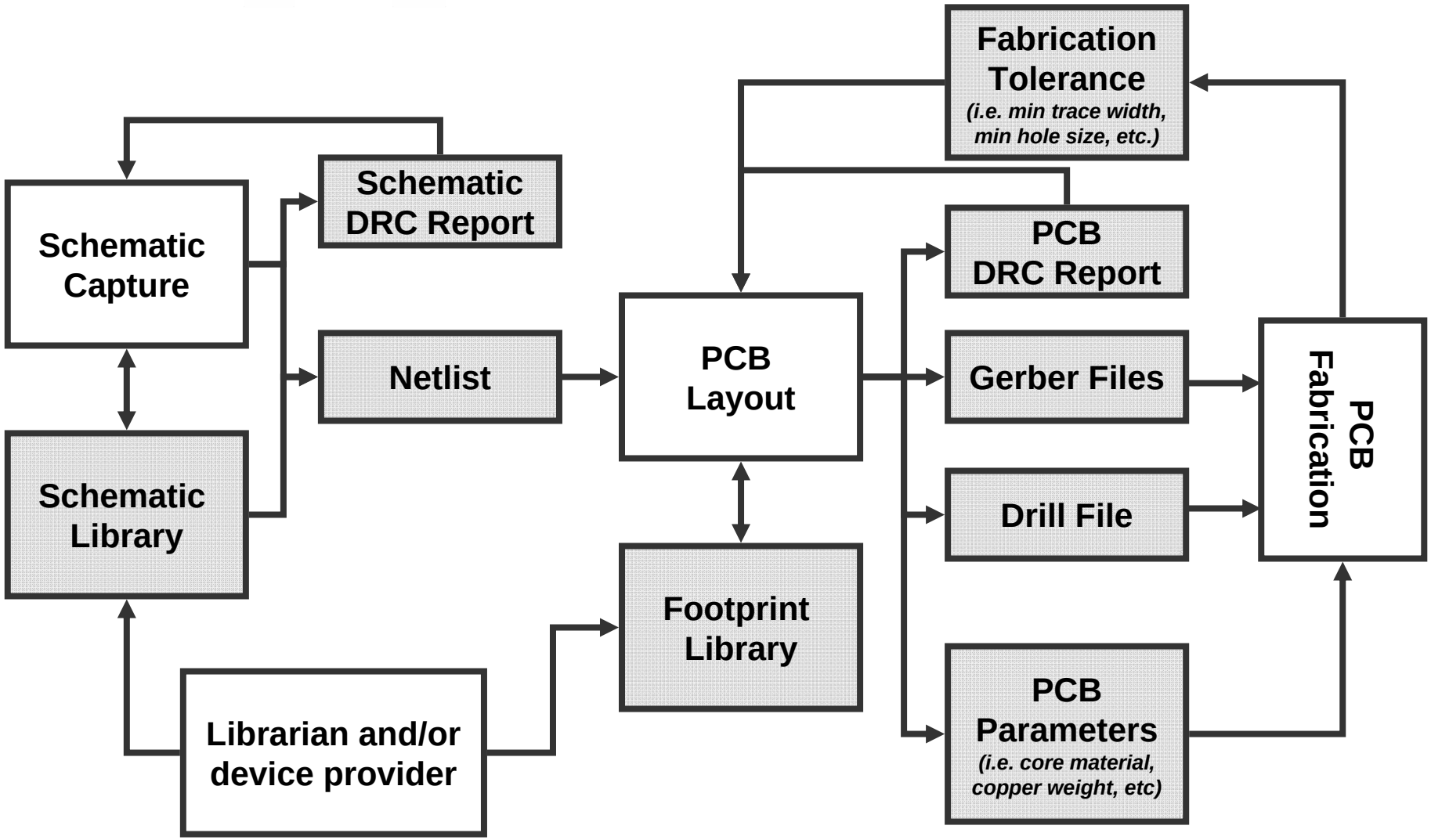
PCB Basics
Vias



- **Vias (plated holes)**
  - Used to connect layers
  - Formed by drilling or punching hole through PCB layers and plating the inside
  - Typically much larger than signal traces
- **Buried and Blind Vias**
  - Provide increased wiring density
  - Added cost to PCB fabrication – typically used only in high-volume
  - Buried vias are difficult to debug
- **Signal Integrity Tip: vias introduce capacitance and change the characteristic impedance of a trace.**

PCB Basics

Typical PCB Design Process



DRC = Design Rule Check

PCB Basics
Typical PCB Fabrication Process

1. **Receive Gerber files, Drill files and other PCB attributes from customer.**
2. **Prepare the PCB substrate and laminate (core)**
   1. **Copper film is attached to the substrate material (i.e. FR4).**
3. **Inner layer image transfer**
   1. **Etch-resist chemical is masked and cured (hardened) over copper film where copper is to remain (i.e. traces and vias).**
   2. **Un-cured chemical is washed away**
   3. **Etchants applied to copper film (typically FeCl or Ammonia). Unmasked copper is dissolved.**
   4. **Solvent applied to remove the cured etch-resist**
   5. **PCB washed to remove all residues**
4. **Laminate layers**
5. **Drilling, cleaning & plating vias**
   1. **This is how connections are made between layers**
   2. **Holes drilled through layer stack where vias are desired**
   3. **PCB immersed in plating solution where a thin layer of copper forms within holes**
   4. **Electro-plating then used to deposit around 1mil of copper**
6. **Outer layer image transfer**
7. **Apply soldermask**
8. **Silkscreen (text and graphics)**

Good High-Speed PCB Design Practices
Overview

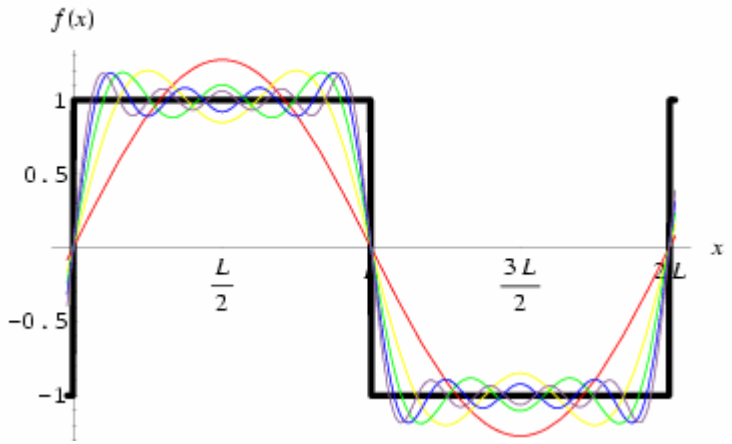
- **Some customers still design PCBs by “feel” and not using proper methodologies and/or discipline.**
- **For modern high-speed analog and digital design, it is almost impossible to produce a reliable design based on “feel”.**
- **Result may be**
  - Improper or unexpected system behavior
  - Unacceptable levels of noise in analog paths
  - System stability/reliability that varies across temperature and/or board build lot.
  - Spurious bit-errors between connected devices on same PCB
  - Large amounts of power supply and ground noise
  - Over-shoot, under-shoot and glitching on signals.

Good High-Speed PCB Design Practices
Using the Right Equipment

- A good oscilloscope with ample bandwidth is an essential tool in high-speed PCB projects.
  - Need to consider the bandwidth and sampling frequency of the device.
    - What will a 133MHz SDRAM signal look like on a low-cost scope with 200MHz bandwidth and 2GSPS sampling rate?
  - Important events like glitching, overshoot and undershoot, and power supply noise may not be properly represented on a low-cost scope.
- Remember! High-speed digital signals are square waves!
  - Square waves are rich in high-energy, odd harmonics

$$x(t) = \sin(t) + \frac{1}{3}\sin(3t) + \frac{1}{5}\sin(5t)...$$

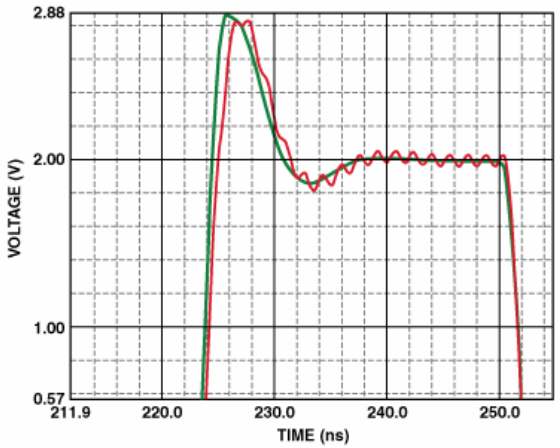
  - As process geometry decreases (130nm->90nm->65nm), rise and fall times decrease = more harmonics!



How are these related?

Good High-Speed PCB Design Practices
Power and Ground Planes

- Power and ground planes should always be used when possible. Why?
  - Provides a low-impedance path between the power supply and the devices in the system.
  - Provide shielding
  - Provide heat dissipation
  - Reduces stray inductance
- A solid, unbroken plane is best.
  - Breaks in the ground plane can introduce parasitic inductance in traces above or below the plane.
- Remember!
  - At low frequency, current will follow the path of least resistance.
  - At high frequency, current will follow the path of least inductance.

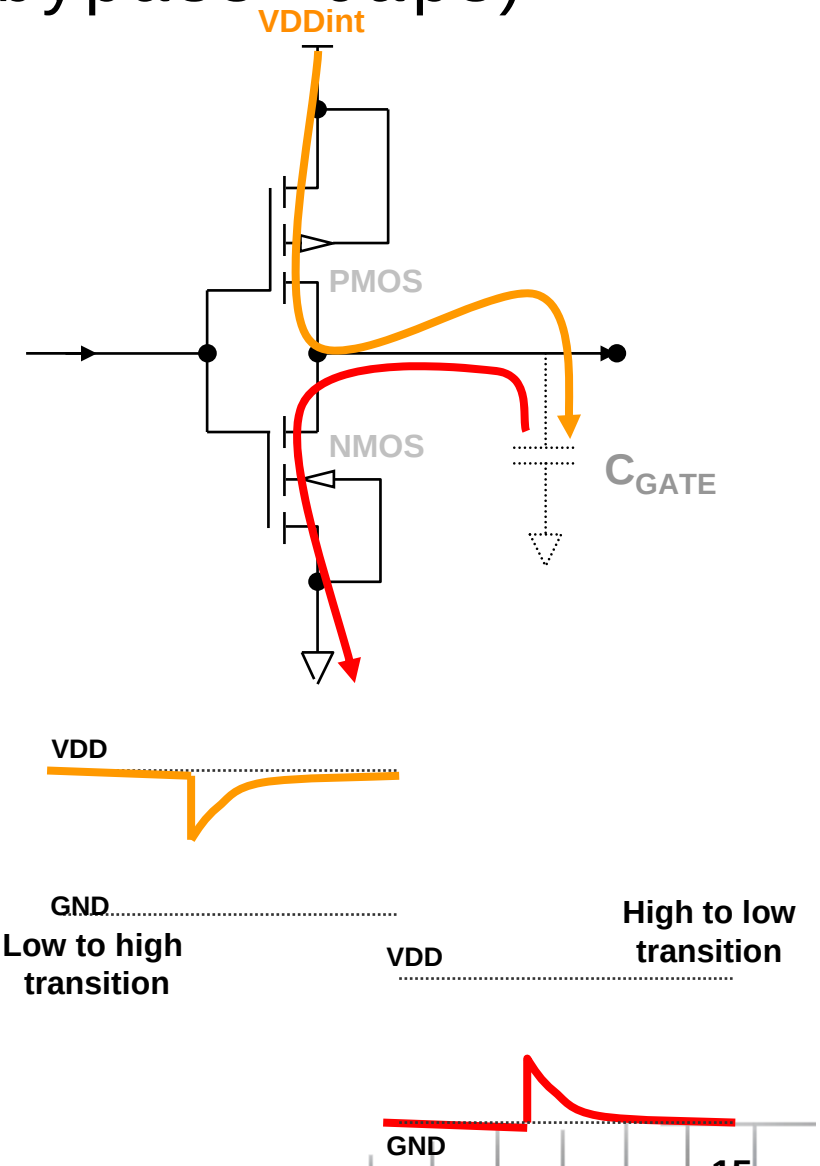


Pulse response with and without a ground plane (*source Analog Dialogue: Volume 39, September 2005*)

Generally Good PCB Design Practices

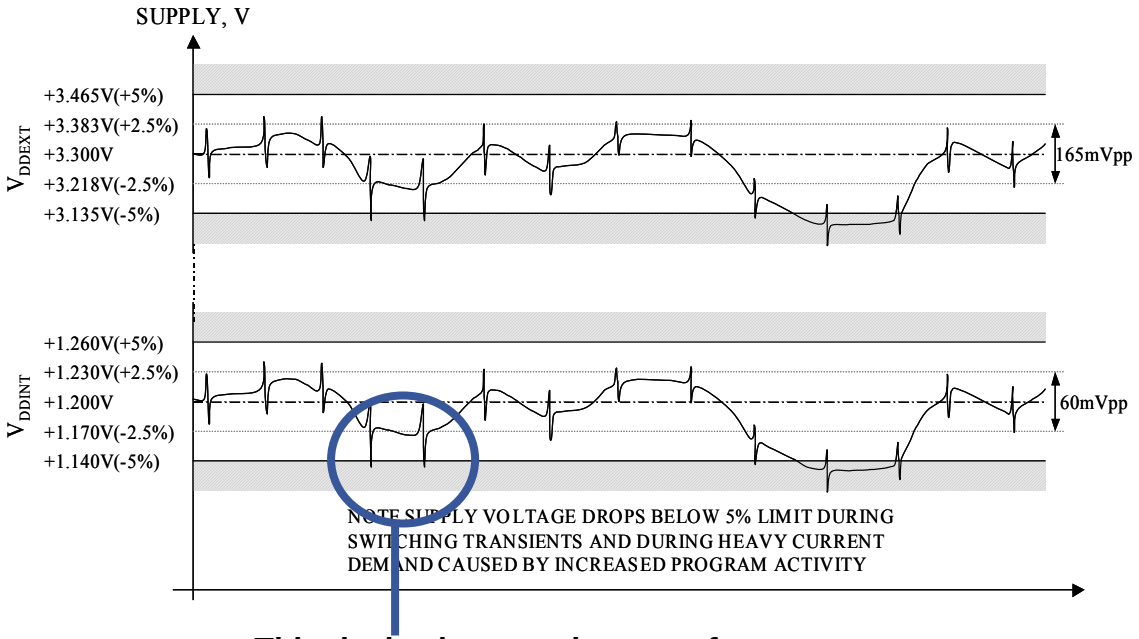
Decoupling Capacitors (or "bypass" caps)

- When gates within a device switch, there is an instantaneous change in impedance within the device.
  - Result is an instantaneous change in current.
- Decoupling capacitors provide a low-impedance current source for these instantaneous changes.
  - Reduces voltage fluctuation on the ground and power signals.
  - Helps ensure power and voltage signals are within the operating specification of the device.



Good High-Speed PCB Design Practices
Decoupling Capacitors

- **Five broad frequency bands need to be "bypassed" with high-speed devices**
  - **DC to 10kHz**
    - Taken care of by the regulator
  - **10kHz to 100kHz**
    - Taken care of by electrolytic bypass capacitors
  - **100kHz to 10MHz**
    - Taken care of by multiple 100nF (0.1uF)
  - **10MHz to 100MHz**
    - Taken care of by multiple 10nF (0.01uF)
  - **100MHz and above**
    - Taken care of by multiple 1nF & PCB Power & Ground Planes



This device is operating out of specification! Ample oscilloscope bandwidth is essential for detecting these events.

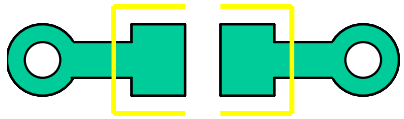
Good High-Speed PCB Design Practices
Decoupling Capacitors

- **How many decoupling capacitors are required?**
  - **System dependent!**
    - Need to consider frequency of operation, number of I/O pins switching, Capacitive load on each pin, trace impedance, junction temperature, internal chip operation, etc.
    - For processors, consider the variety of internal operations like cache, internal memory accesses, DMA, etc. etc. etc.
  - **The rule of thumb: At all frequencies from DC, to well above the highest clock frequencies, the supply pins should have less than ±5% of VDD total noise.**
  - **The tolerance of the maximum DC supply voltage drift PLUS the peak noise amplitude must be less than 5% of the nominal supply voltage.**
    - An oscilloscope with ample bandwidth is required.
- **Various methods exist for estimating the total required capacitance and how to distribute the capacitance across a number of smaller value capacitors**
  - This is a complex problem, particularly when dealing with the complexities of modern processors which contain millions of gates.
  - Numerous application notes on semiconductor websites
    - www.freescale.com/files/32bit/doc/app_note/AN2586.pdf

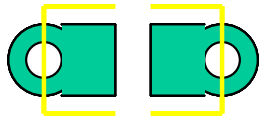
Good High-Speed PCB Design Practices

Decoupling Capacitors

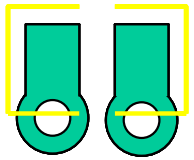
- **For best performance, minimize the inductance and resistance between the device supply pins and the decoupling capacitors.**
- **PCB traces and vias introduce impedance!**



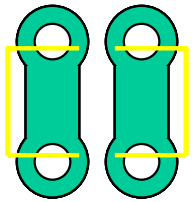
ABSOLUTELY NOT!



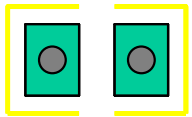
BETTER



EVEN BETTER



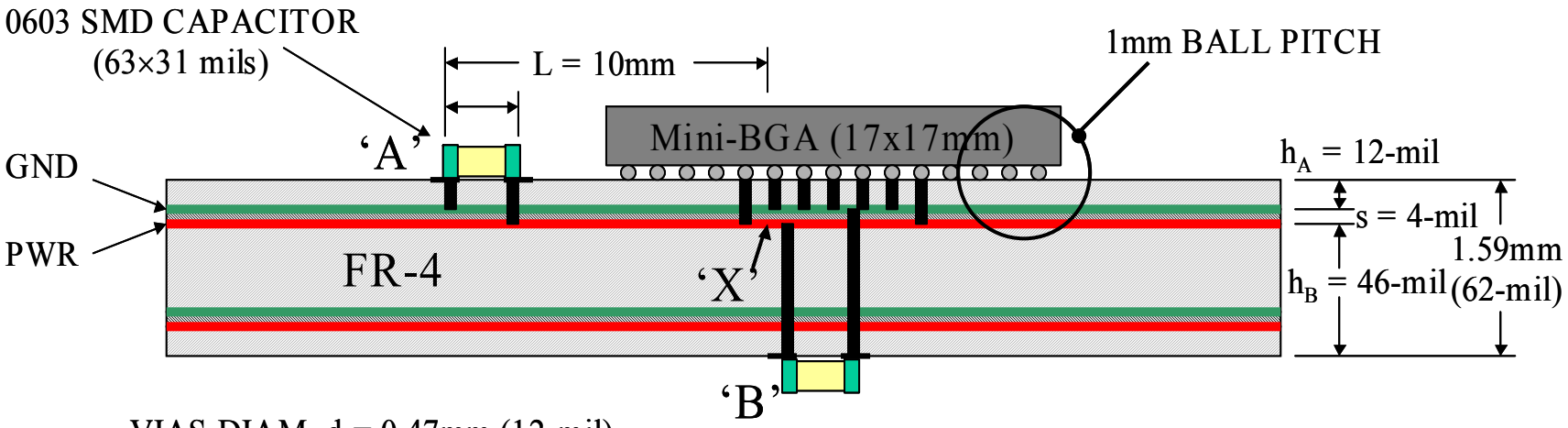
EVEN BETTER STILL



THE BEST!
SOLID VIA WITHIN PAD

Good High-Speed PCB Design Practices
Decoupling Capacitors

- **When ground/power plane pairs are used, capacitors can be just as effective on the top side of the PCB.**

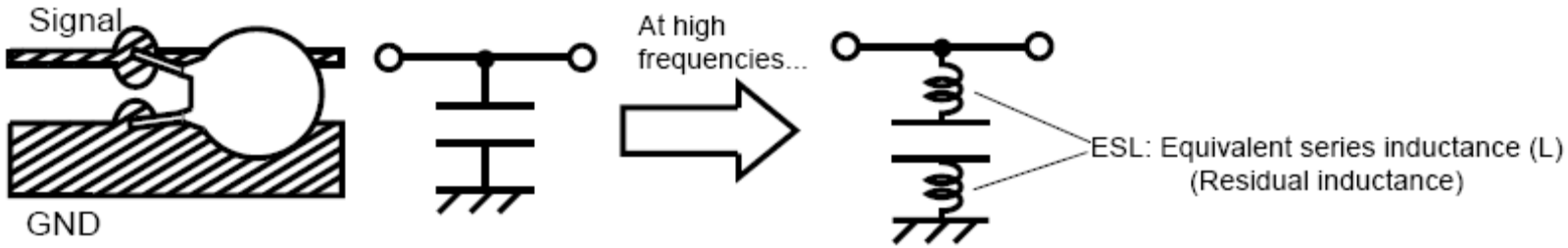


Good High-Speed PCB Design Practices
Decoupling Capacitors

- **Effective bypassing at frequencies over 100MHz…**
  - **As clock frequencies and edge rates increase it becomes more difficult to effectively bypass the power supply pins of high-frequency devices.**
    - Capacitor ESL (Effective Series Inductance) results in increasing reactance with frequency
    - Capacitor ESR (Effective Series Resistance) increases, reducing the effectiveness of capacitors
    - Capacitor parasitic mounting (pads, vias) reactance increases with frequency
    - 100nF capacitors are useless above 100MHz

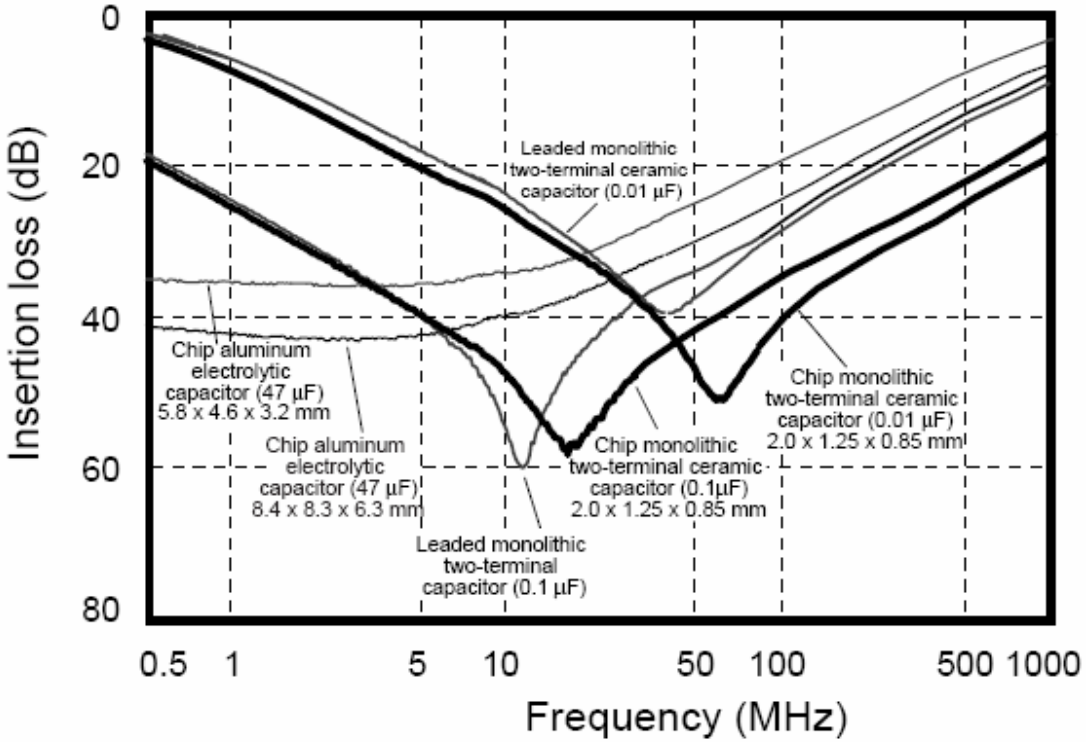
Good High-Speed PCB Design Practices
Understanding Capacitors - ESL

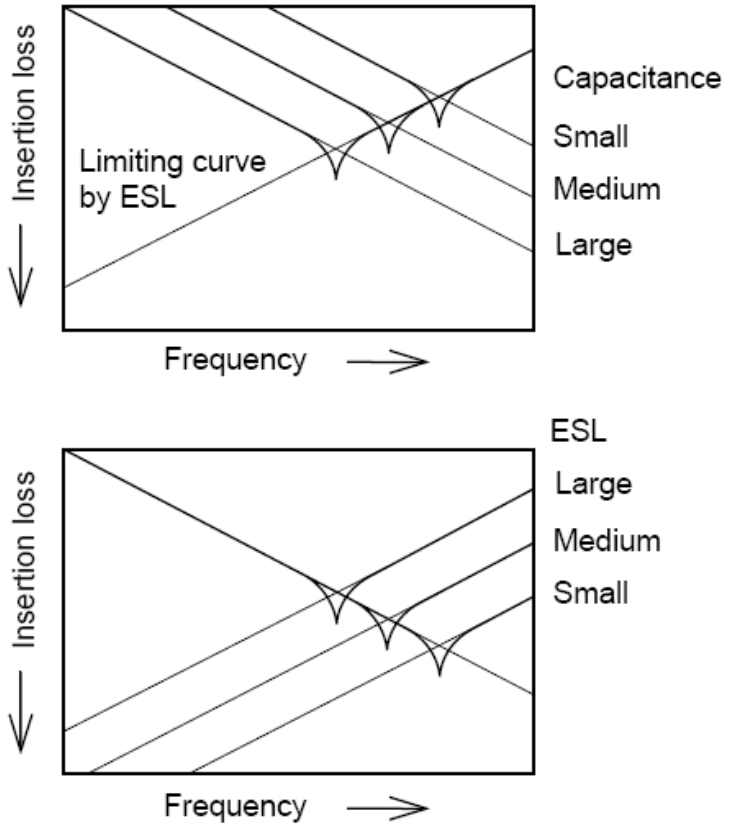
- **ESL (Effective Series Inductance) is caused by the inductance of the electrodes and leads of the capacitor.**
- **The ESL of a capacitor sets the limiting factor of how well (or fast) a capacitor can de-couple noise off a power buss.**



- **Capacitors are essentially an L-C circuit thus they have a resonant point. The ESL and the capacitance thus both affect the resonate-point of a capacitor.**
- **Capacitors with a high resonant frequency will perform**

Good High-Speed PCB Design Practices
Understanding Capacitors - ESL



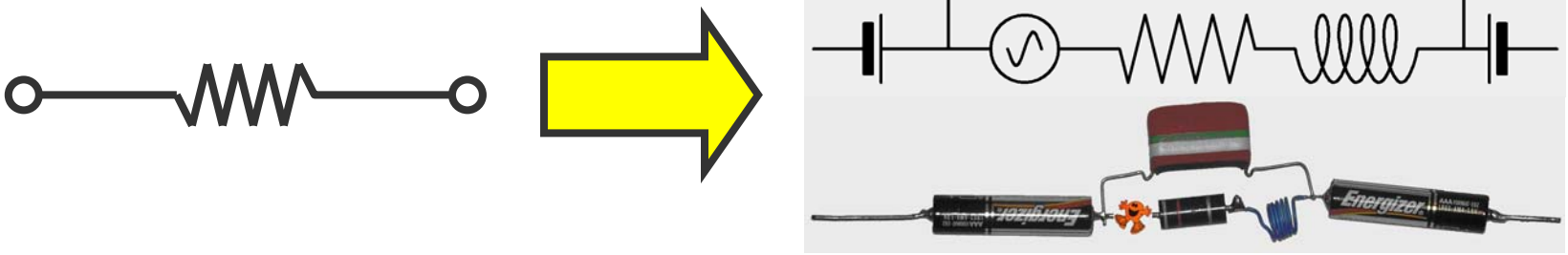


Source: www.murata.com/emc/knowhow/pdfs/te04ea-1/12to16e.pdf

Good PCB Design Practices
Understanding Capacitors

- Different types of capacitors…
  - TBA

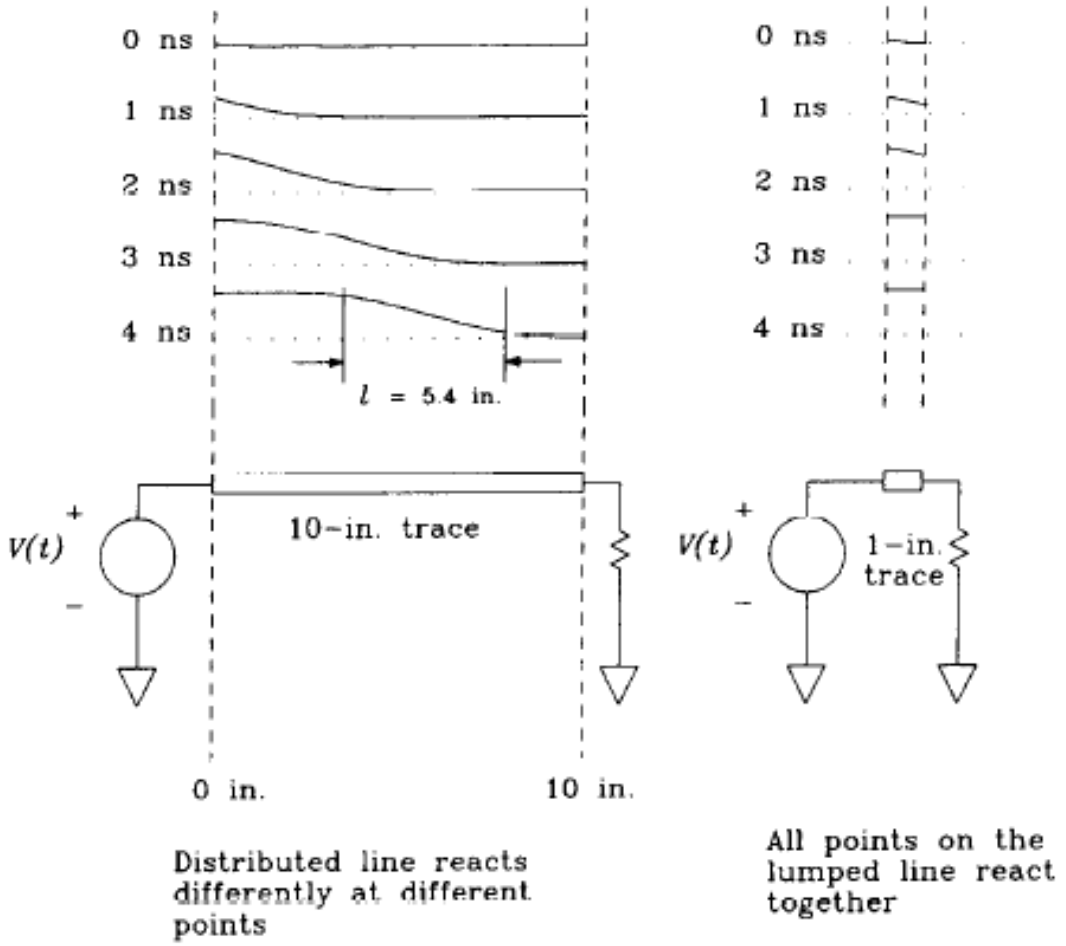
High Speed PCB Design and Layout
Understanding Resistors



- James Bryant's paper
  - TBA

High Speed PCB Design and Layout
Wire or Transmission Line?

- **Wire or Transmission Line?**
  - Wire – we consider every point of a wire to be at the same potential at any given point in time
  - Transmission Line – we consider the effects of signal propagation and assume that points along the transmission line will be at different voltage potentials as signals traverse.
- **When to treat a signal path as a transmission line?**
  - If the length is greater than 1/100 of the wavelength.
  - If the receiving device is edge sensitive.
  - If the system is not tolerant of excessive overshoot and undershoot.
  - Almost always!



Source: Johnson & Graham, High-Speed Digital Design (A Handbook of Black Magic)

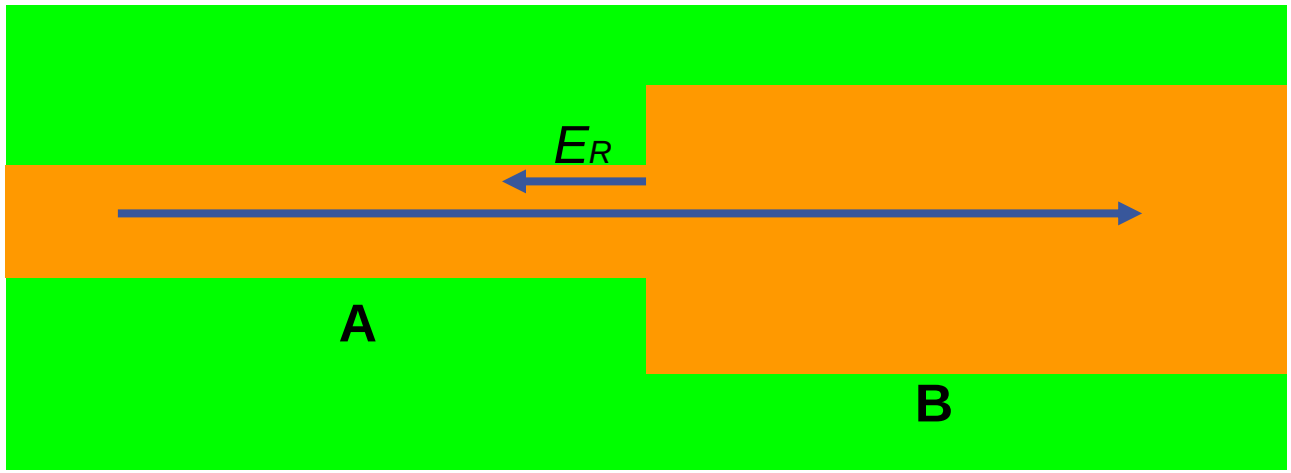
High Speed PCB Design and Layout

Propagation : Time and Distance

- **Propagation Delay : the rate at which an electrical signal travels through a medium.**
  - **Typically measured in picoseconds/inch.**
- **Electrical signals propagate at a speed dependent on the surrounding medium.**
  - **Propagation delay increases proportionally to the square root of the dielectric constant**

Medium	Delay (ps/in)	Dielectric Constant
Vacuum	Speed of light : 84.72528	1.0
Air (radio waves)	85	~1.0
Coaxial Cable (75% velocity)	113	1.8
Coaxial Cable (66% velocity)	129	2.3
FR4 PCB (outer trace)	140-180	2.8-4.5
FR4 PCB (inner trace)	180	4.5
Alumina PCB (inner trace)	240-270	8-10

High Speed PCB Design and Layout
Transmission Lines and Impedance Mismatch



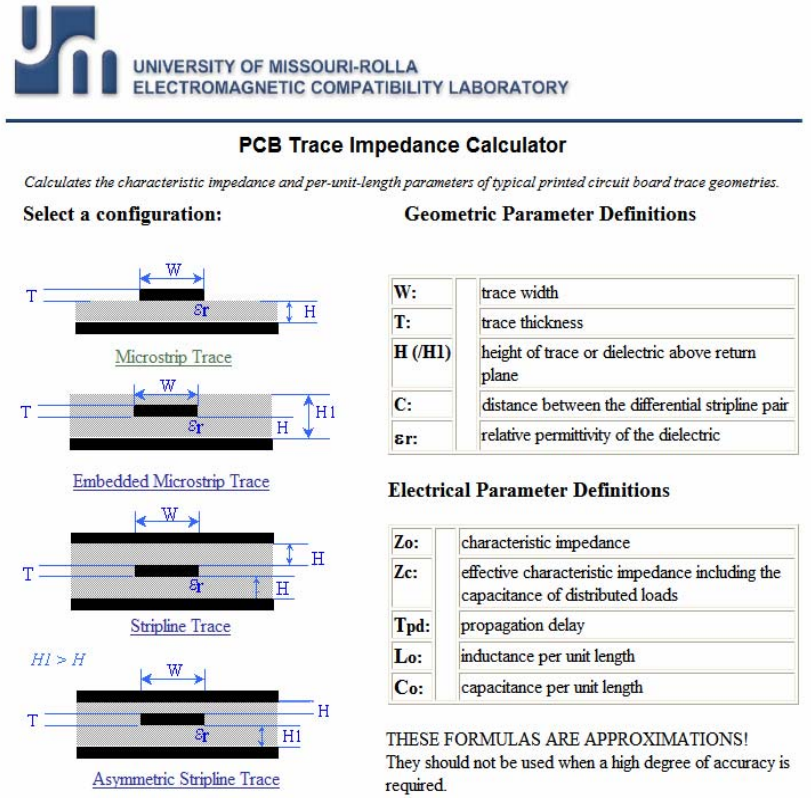
- **When the impedance of a conductor changes a portion of the signal energy is reflected.**
- **The amount of energy reflected is proportional to the difference in impedance between the two conductors.**

$$E_R \propto \frac{Z_B - Z_A}{Z_B + Z_A}$$

High Speed PCB Design and Layout
Understanding Trace Impedance

- **The physical characteristics of the PCB trace will have a large effect on the impedance.**
  - **Trace material**
  - **Width of trace**
  - **Trace thickness**
  - **Proximity to other traces and planes**
  - **Dielectric constants of surrounding materials (i.e. air, FR4, etc).**
- **Many free tools available to help estimate the impedance of a trace.**

http://emclab.umr.edu/pcbtlc2/index.html



UNIVERSITY OF MISSOURI-ROLLA
ELECTROMAGNETIC COMPATIBILITY LABORATORY

PCB Trace Impedance Calculator

Calculates the characteristic impedance and per-unit-length parameters of typical printed circuit board trace geometries.

Select a configuration:

Geometric Parameter Definitions

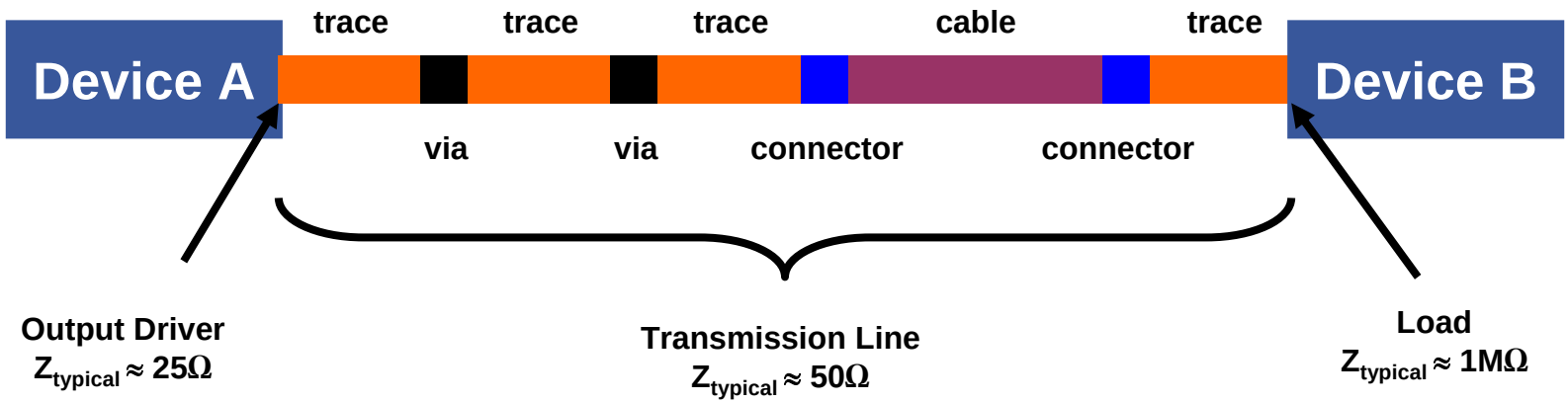
W:	trace width
T:	trace thickness
H (/H1)	height of trace or dielectric above return plane
C:	distance between the differential stripline pair
εr:	relative permittivity of the dielectric

Electrical Parameter Definitions

Zo:	characteristic impedance
Zc:	effective characteristic impedance including the capacitance of distributed loads
Tpd:	propagation delay
Lo:	inductance per unit length
Co:	capacitance per unit length

THESE FORMULAS ARE APPROXIMATIONS!
They should not be used when a high degree of accuracy is required.

High Speed PCB Design and Layout
Changes in Impedance Across Signal Path



- **Device A to Device B, a propagating signal will likely traverse multiple impedance changes.**
- **The largest mismatches will almost always occur at the source and load**
  - **Will generate large reflections!**
  - **How can we deal with this?**
- **Let's look at a story…**

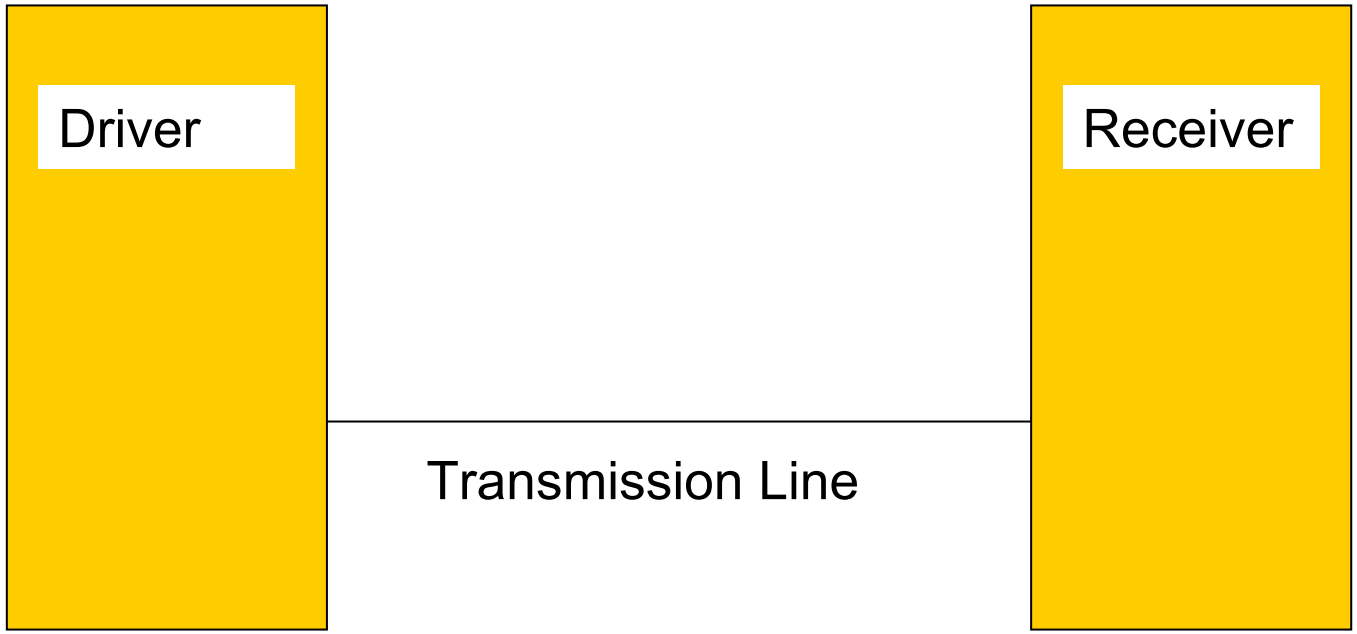
The Story of EDGAR the Energy Packet

Courtesy of Bob Kilgore

- **Edgar is a jogger**
- **He travels at a rate of 6 inches / nanosecond on a Printed Circuit Board**
- **He changes the voltage of conductors that he touches**

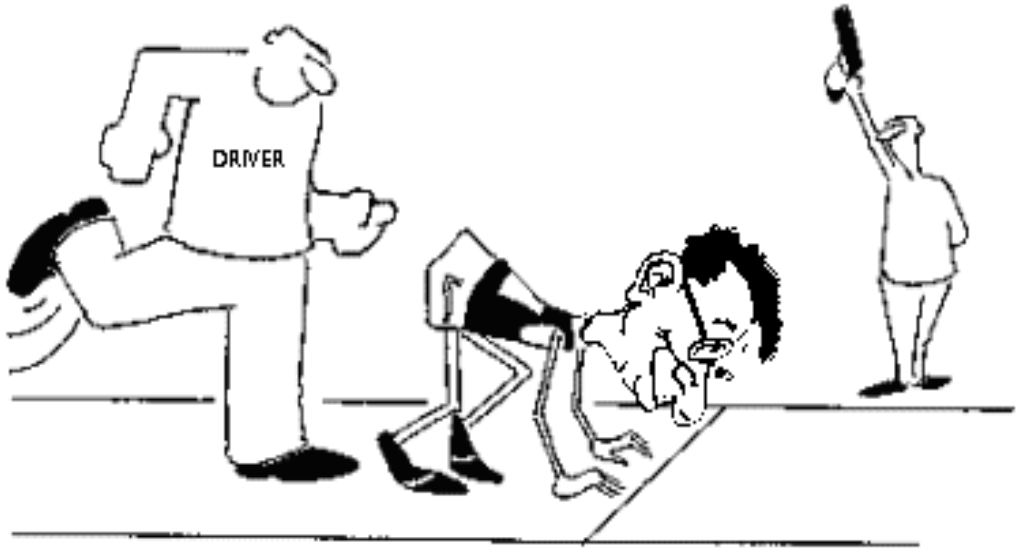
Edgar Meets The "Unterminated" Transmission line

- **Attributes:**
  - **Point to point connection**
  - **25 Ohm impedance Output Driver**
  - **50 ohm impedance Transmission Line (Z_0)**
  - **1 Meg Ohm impedance receiver**



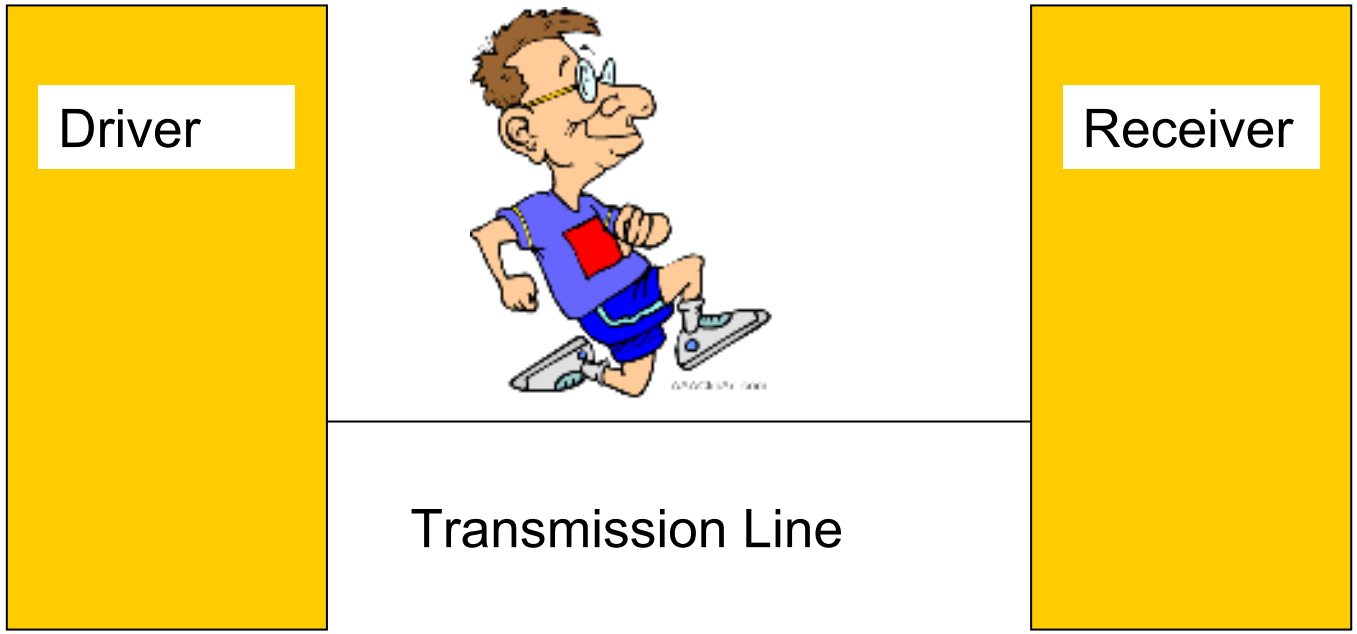
At The Start

The Driver lowers the voltage by from VDD to GND.



Edgar Starts for the Receiver

Edgar travels at 6 inches per nanosecond

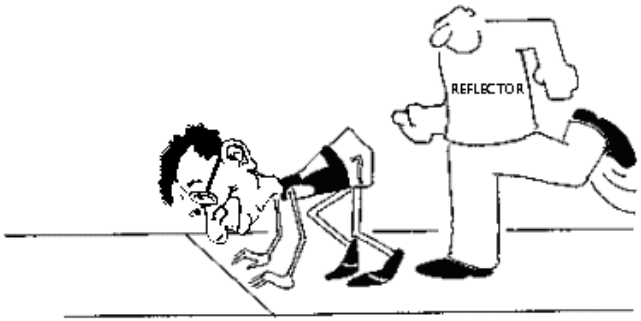


Edgar Is REFLECTED!

- **Edgar is moving from a 50Ω transmission line to 1MΩ receiver!**

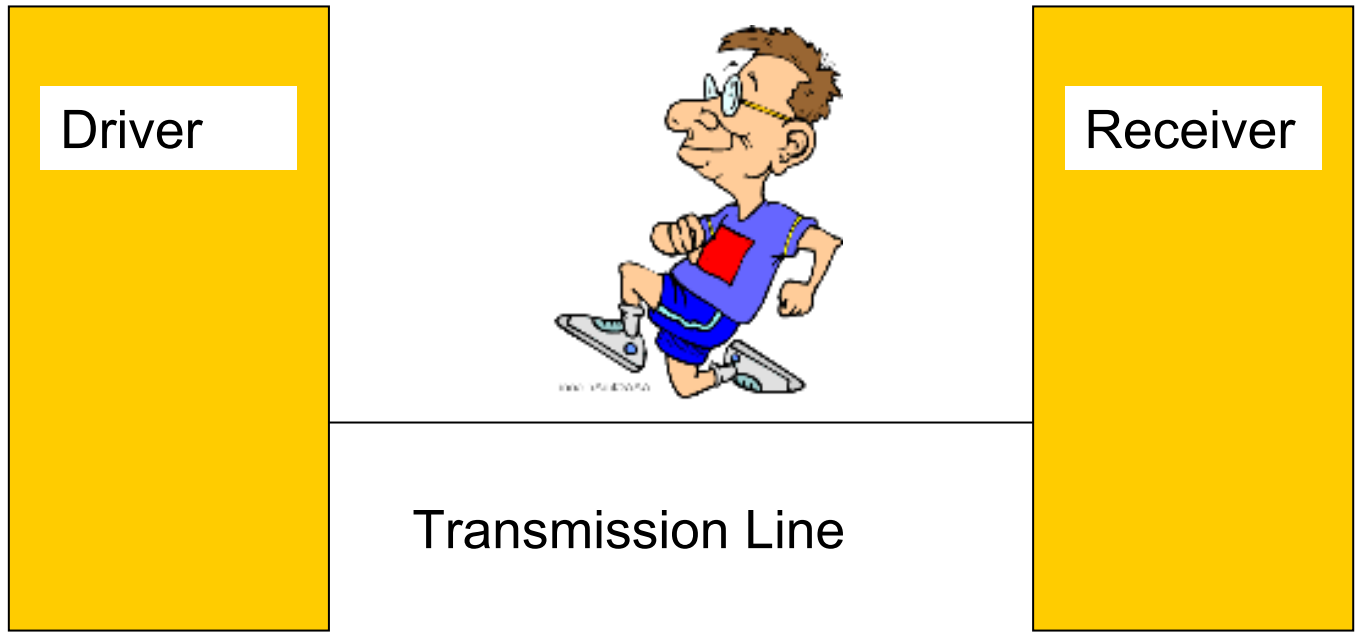
$$\frac{Z_L - Z_0}{Z_L + Z_0} = \frac{1000000 - 50}{1000000 + 50} \approx 1$$

- **Almost 100% of Edgar is reflected back towards the source!**



Edgar Returns to the Driver

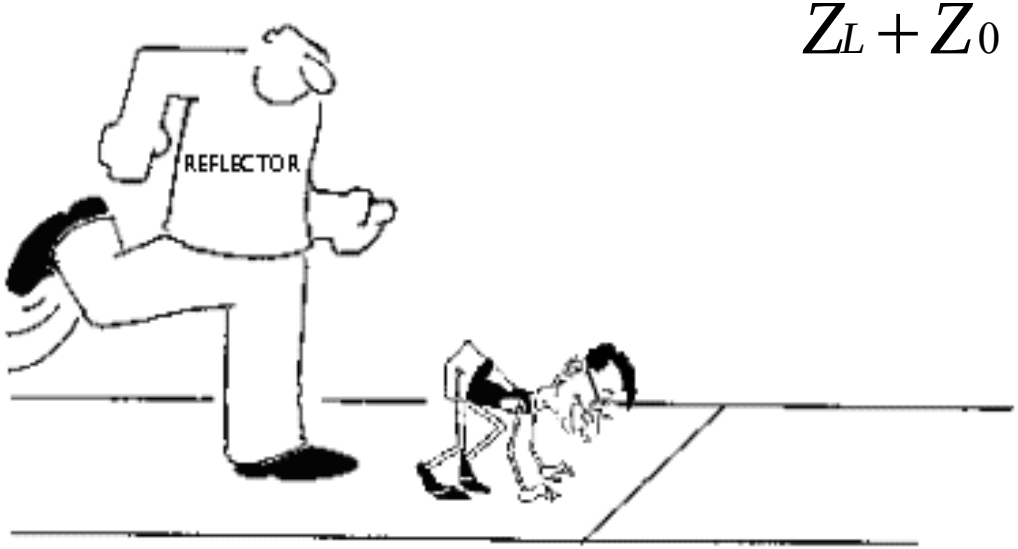
- **Edgar travels at 6 inches per nanosecond with most of his original energy!**



Edgar Finds the Next Obstacle

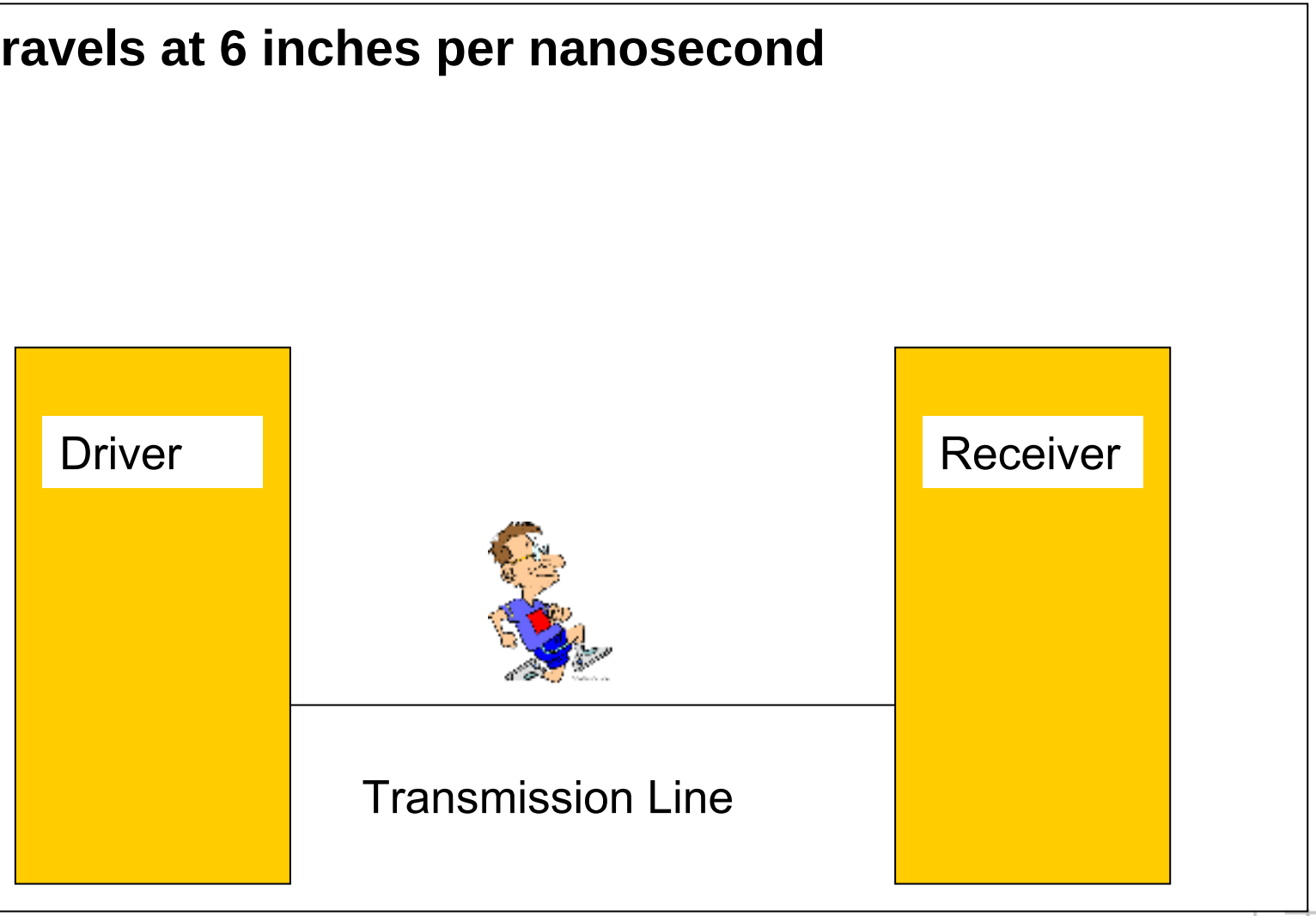
- **Edgar meets the 25Ω source driver after his return journey on the 50 ohm transmission line.**
- **The Reflected Energy is:**

$$\frac{Z_L - Z_0}{Z_L + Z_0} = \frac{25-50}{25+50} = -\frac{1}{3}$$



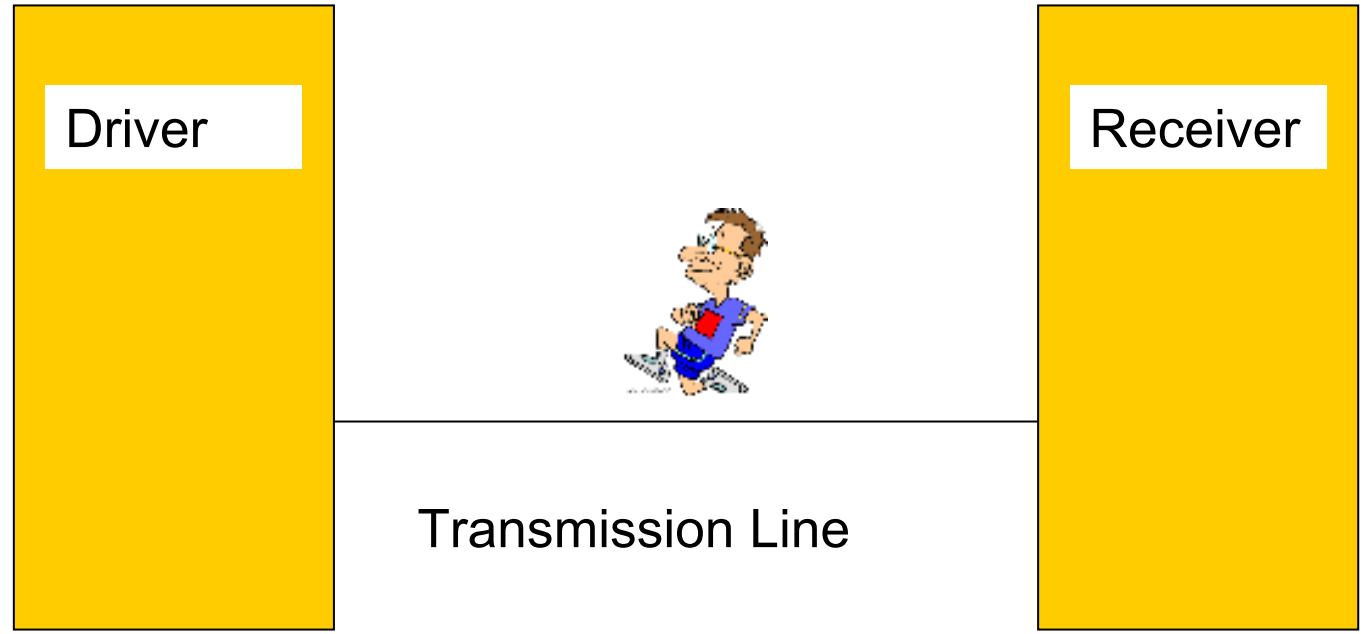
Edgar Is Sent to the Receiver Again

Edgar travels at 6 inches per nanosecond



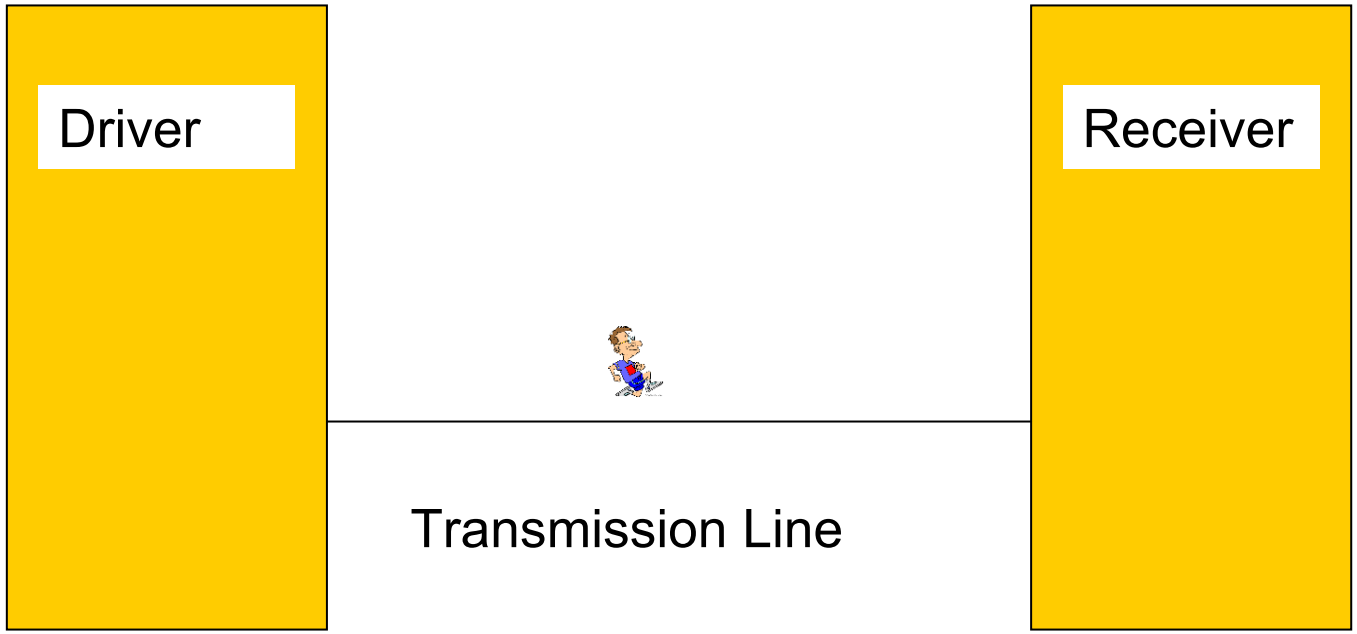
Edgar Is Sent to the Driver Again

Edgar travels at 6 inches per nanosecond



Edgar Is Sent to the Receiver a Third Time

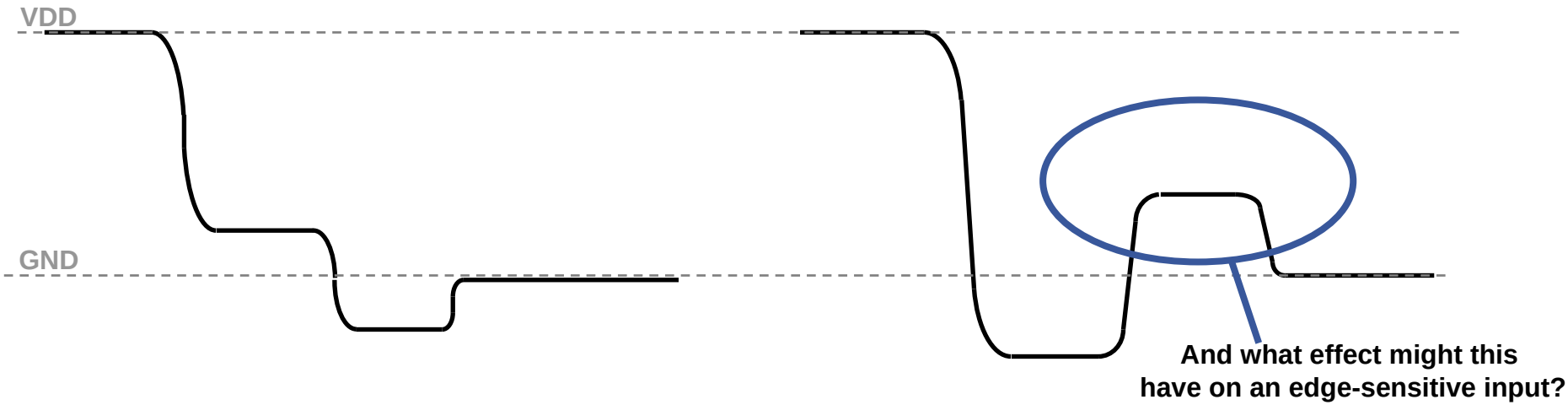
Edgar travels at 6 inches per nanosecond



What would we see on the scope?

Measured at the Driver

Measured at the Receiver



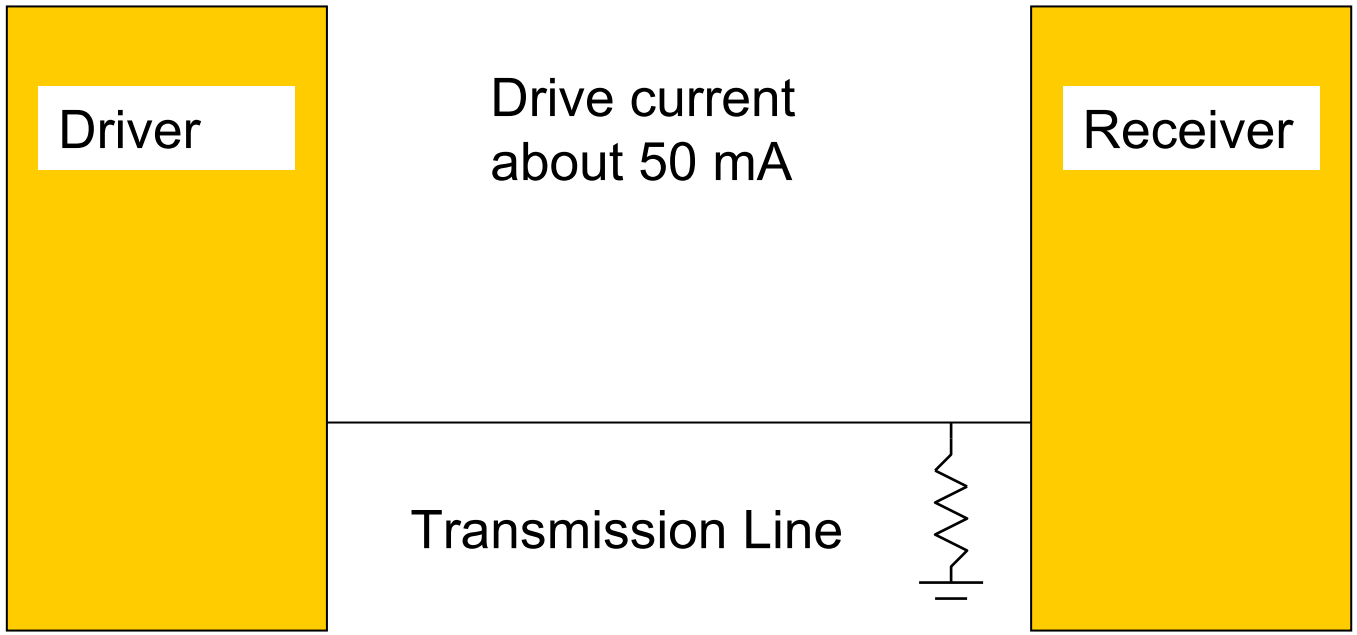
Always measure at the Receiver not the Driver!

High Speed PCB Design and Layout
Transmission Line Termination

- **Leverage Ohms' law to minimize the impedance mismatch at the source side and load of the transmission line.**
- **Managing the Source :**
  - **Source impedance is typically less than 50Ω**
  - **We can add a series resistor to the source to increase its impedance to match the transmission line.**
  - **This technique is called "serial termination"**
- **Managing the Load :**
  - **Load impedance is typically much greater than 50Ω**
  - **We can add a parallel resistor to the load to decrease its impedance to match the transmission line.**
  - **This technique is called "parallel termination"**
- **Each method has its pros and cons.**
- **A combination of both is often most effective.**

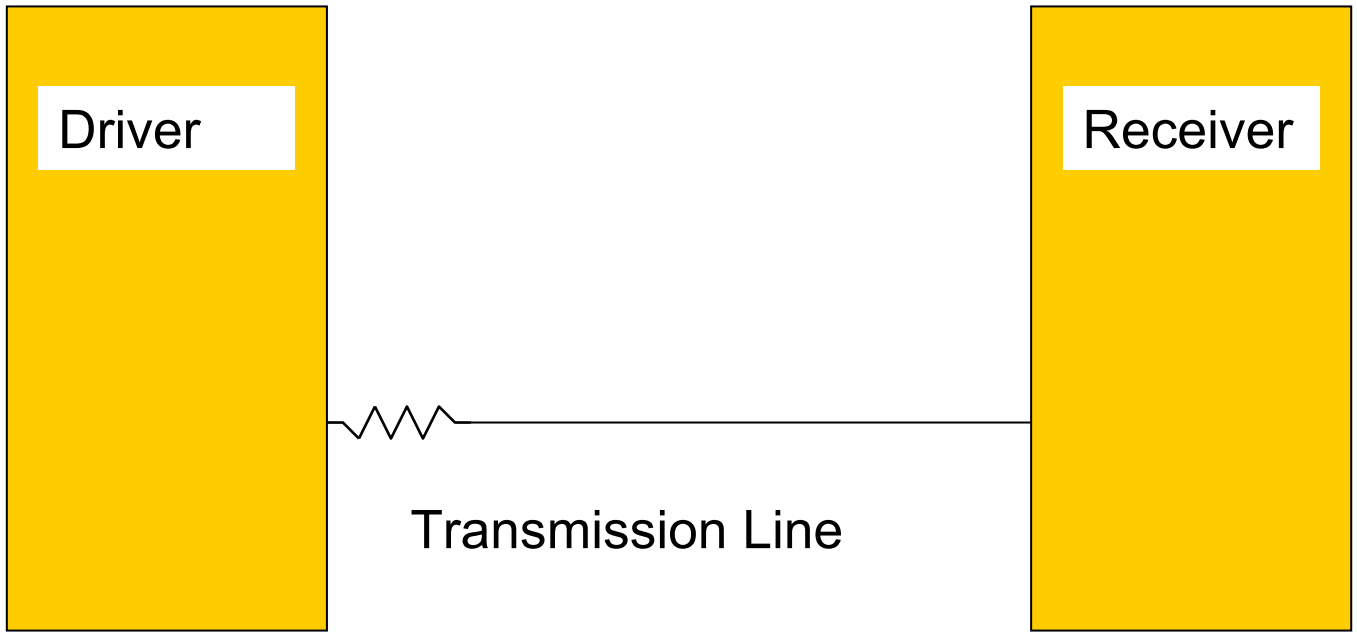
Parallel Termination

- **Parallel resistor at the receiver can work well but has:**
  - **Increases drive current and thus increases power dissipation.**
  - **Increased Crosstalk, Increased EMI.**
  - **Increased ground bounce or supply noise (depending on if the parallel resistor is pulled high or low).**



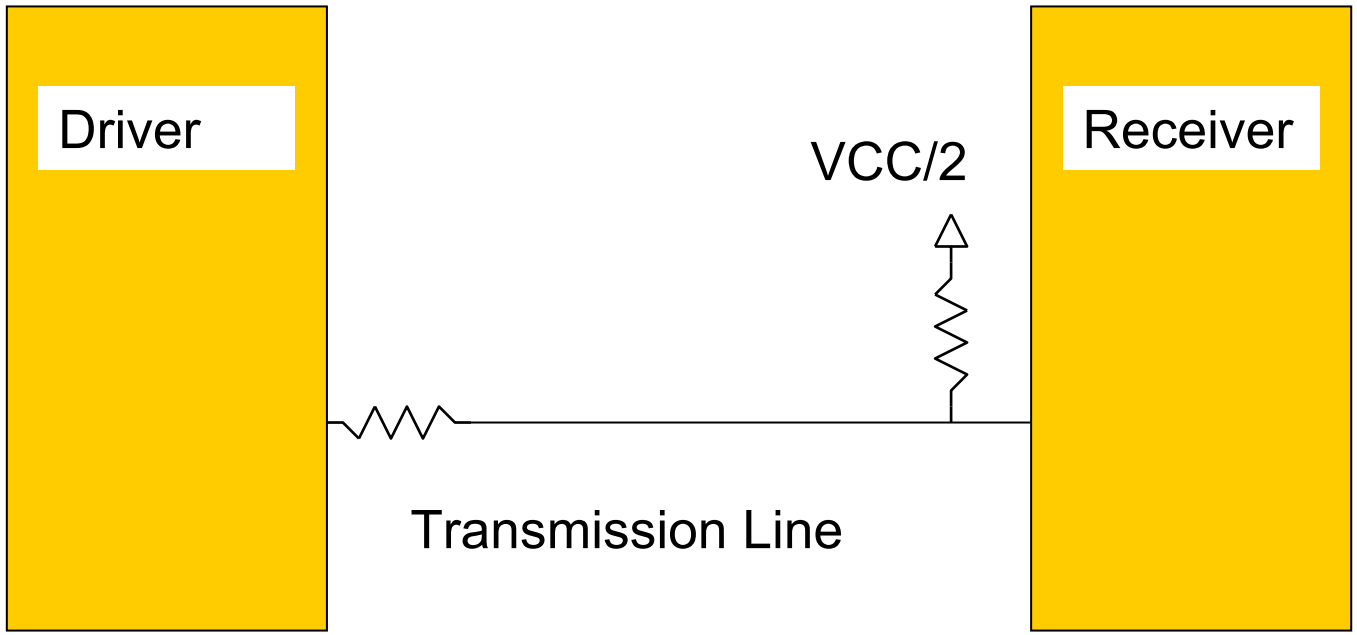
High Speed PCB Design and Layout
Series Termination

- **Series resistor at the driver is less disruptive:**
  - **…but the driver impedance is nonlinear and you lose some energy getting into the transmission line**



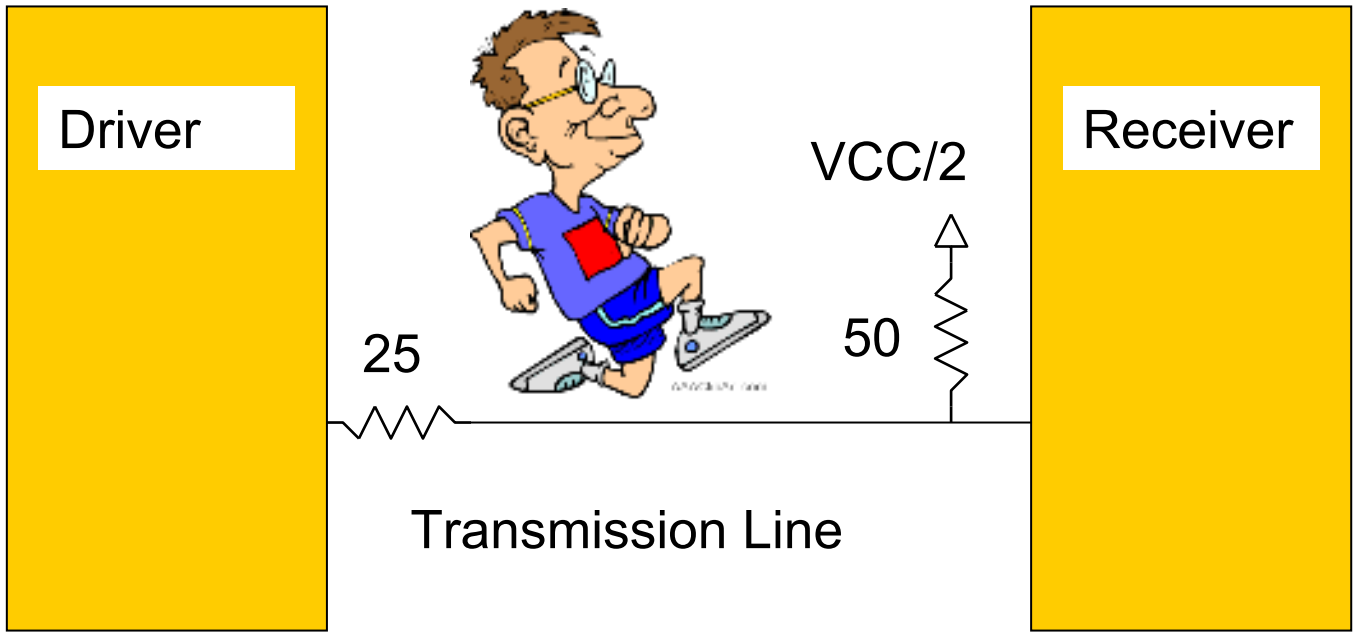
DDR SDRAM Termination

- **DDR uses Dual termination.**
- **At VCC/2 = 1.25V, Io of the driver is about 14mA**



Edgar Meets DDR in the Real World

- **The Series Resistor Plus the Drive impedance is 50 Ohms**
- **The Parallel Resistor is 50 Ohms**
- **The Transmission Line Impedance is 60 Ohms (Bad PCB)**



Edgar Finds the First Obstacle

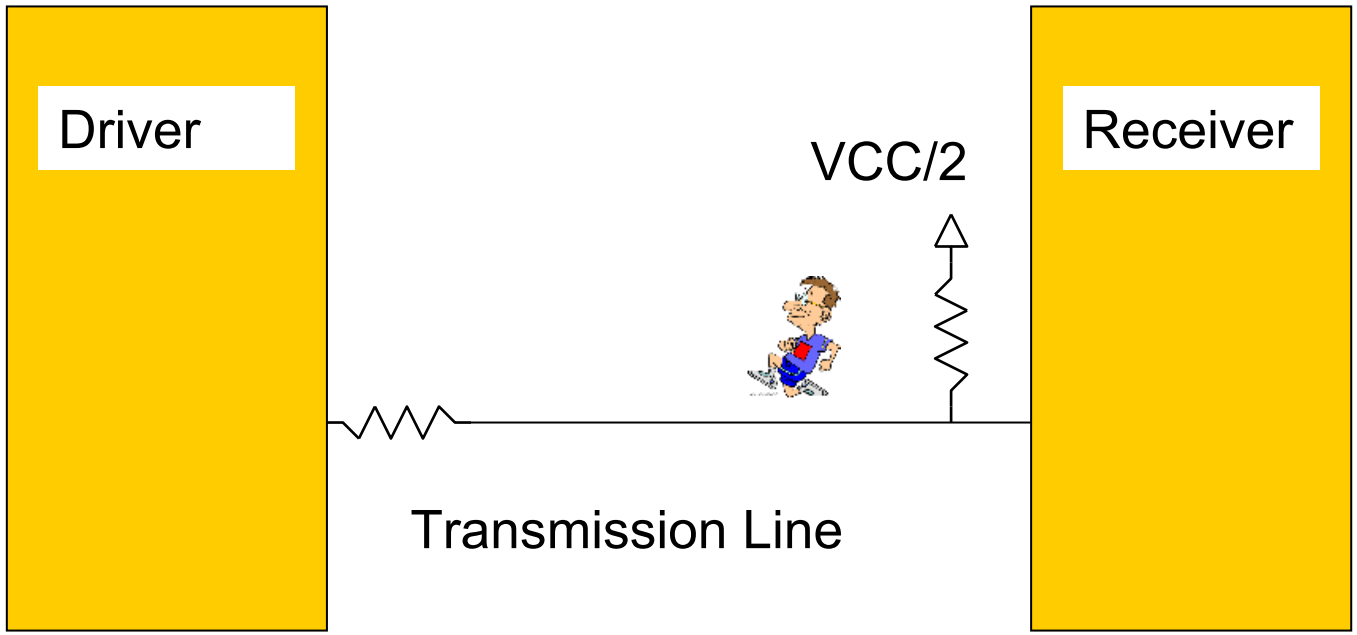
The Receiver is a 50 Ohm Load But the Transmission Line was 60 Ohms Due To FR4 Construction and Fabrication Errors

The Reflected Energy is:

$$\frac{Z_L - Z_0}{Z_L + Z_0} = \frac{50-60}{50+60} = \frac{-1}{11}$$

Edgar is Reflected

- **Edgar travels at 6 inches per nanosecond**



Edgar Finds the Next Obstacle

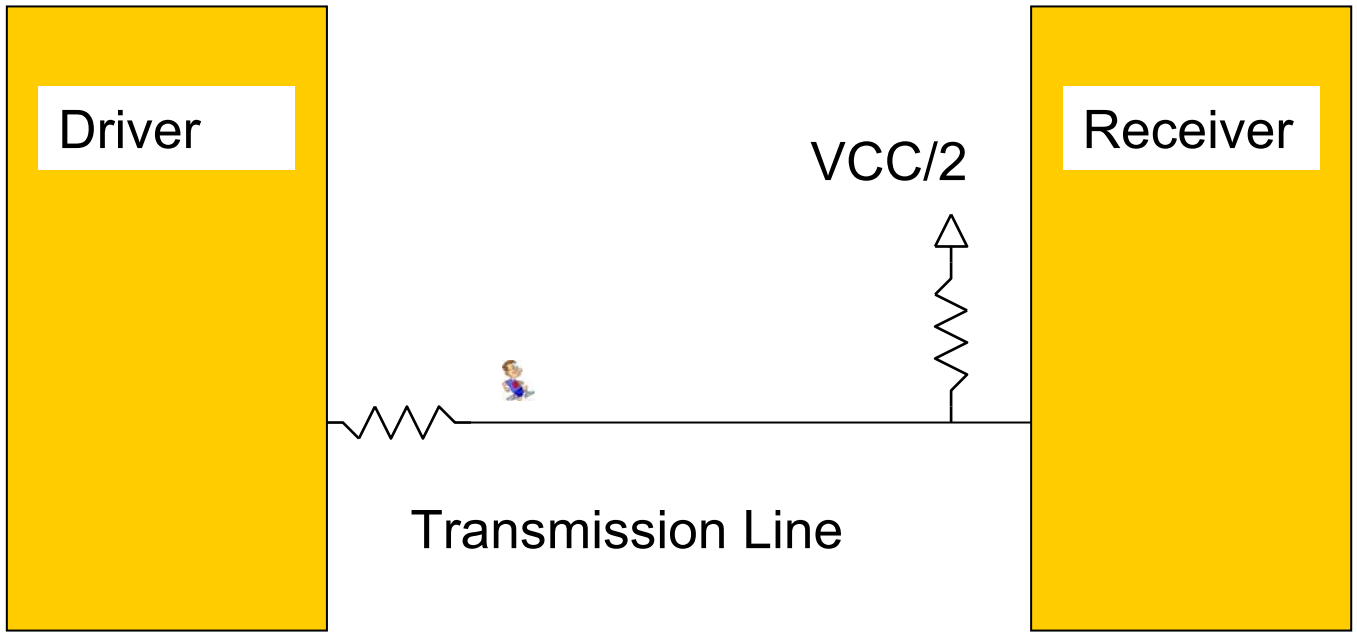
The Driver is a 50 Ohm Load But the Transmission Line was 60 Ohms Due To FR4 Construction and Fabrication Errors

The Reflected Energy is:

$$\frac{Z_L - Z_0}{Z_L + Z_0} = \frac{50-60}{50+60} = \frac{-1}{11}$$

Edgar is Reflected

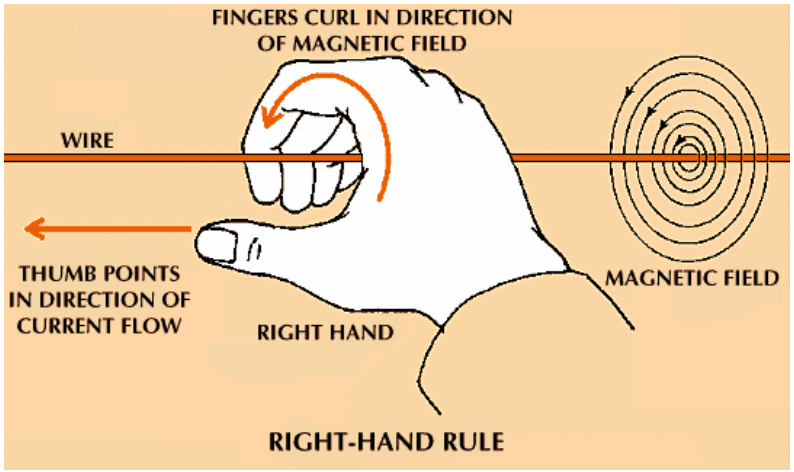
- **Edgar Travels at 6 inches per nanosecond**
- **Edgar is now about 1/100 of its original Energy**
- **Therefore Edgar changes the voltage by 1/10 or about 0.2 volts**



Good PCB Design Practices

Electro-Magnetic Emissions

- Two primary tenants of electro-magnetism
  - Current passing through a conductor generates a magnetic field.
  - Placing a conductor in a magnetic field will induce current
- The shape an intensity of a magnetic field generated by passing current through a conductor is affected by the shape of the conductor and visa versa.



Good PCB Design Practices

EMI : Electro-Magnetic Interference

- EMI typically refers to an undesirable amount of electromagnetic emission from a design.
- EMI from one device on a PCB may affect the performance of another device.
  - Digital circuits are more likely to be the source of disruptive emissions due to the handling of periodic waveforms and the fast clock/switching rates.
  - Analog circuits are more likely to be the susceptible victims due to higher gain functions.
- EMI from the entire system may affect the performance of other near-by systems.

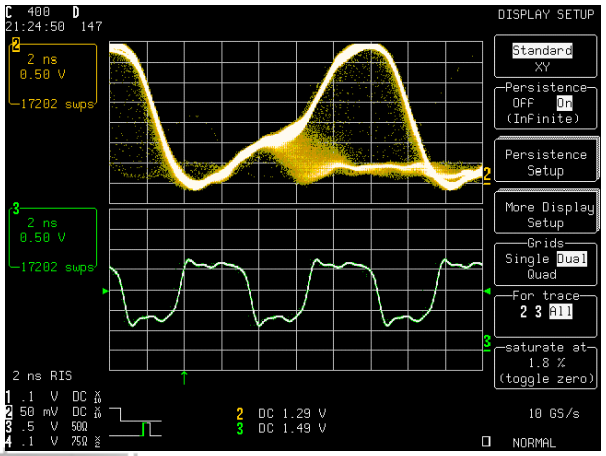
Good PCB Design Practices

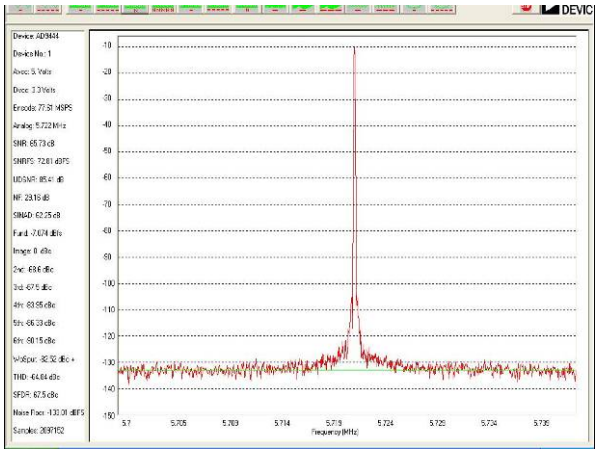
Reducing EMI in PCBs

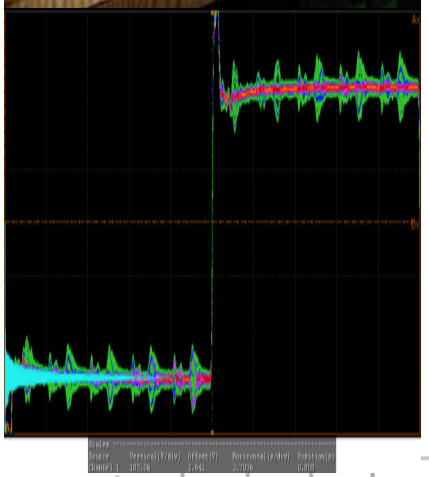
- There are many widely used techniques for minimizing the EMI of a PCB design.
- Fundamentals:
  - Power and ground planes providing shielding
    - Top and bottom ground planes can help reduce radiation from multi-layer boards by at least 10 dB.
  - Physical placement of devices on the PCB – keep analog and digital systems as far apart as possible on the PCB
  - Proper use of decoupling caps reduces power/ground noise and thus EMI from these planes.
  - Keep signal traces away from the edge of the PCB
  - Avoid right angles in PCB traces
  - Be cognizant of PCB trace resonance at fundamental frequency or harmonics due to reflections.
  - More to come…
- http://www.radioing.com/eengineer/pcb-tips.html

Getting the best performance on our PCBs

- **As amplifiers and converters' performance improved, achieve their performance on your PCB will be challenging.**
- **Layout guide & design notes training before PCB layout will save much time in debugging.**
- **Moving on today's training**
  - **Mixed Signal PCB Layout Techniques**
  - **Small Signal PCB Layout Techniques**







The World Leader in High Performance Signal Processing Solutions

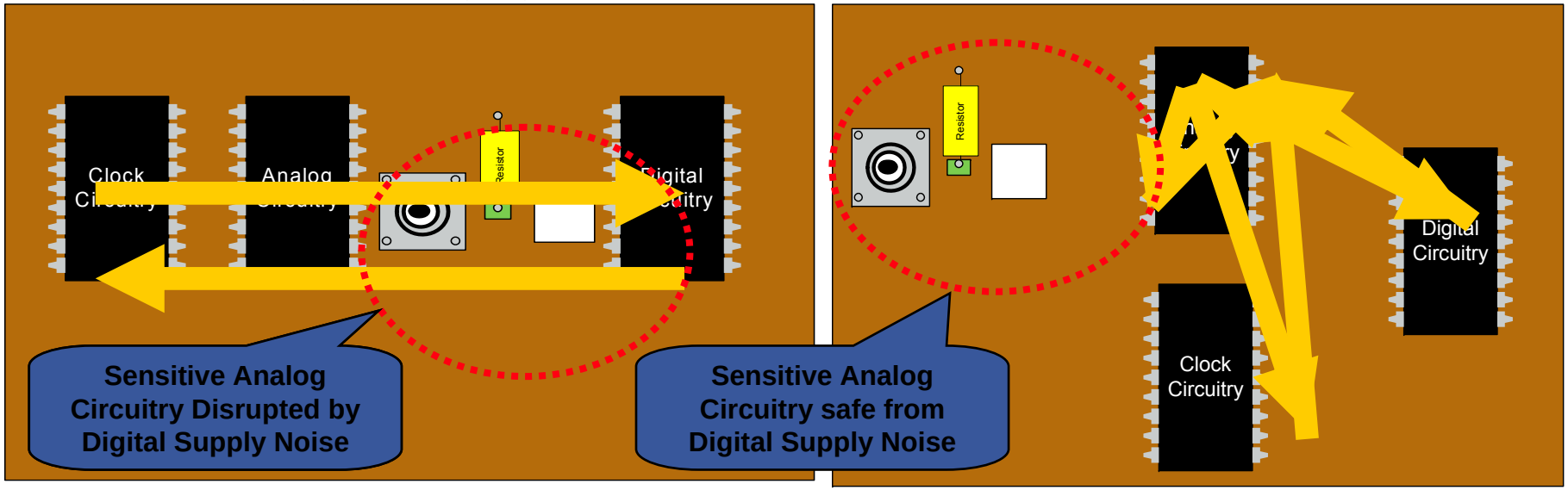
Mixed Signal PCB Layout

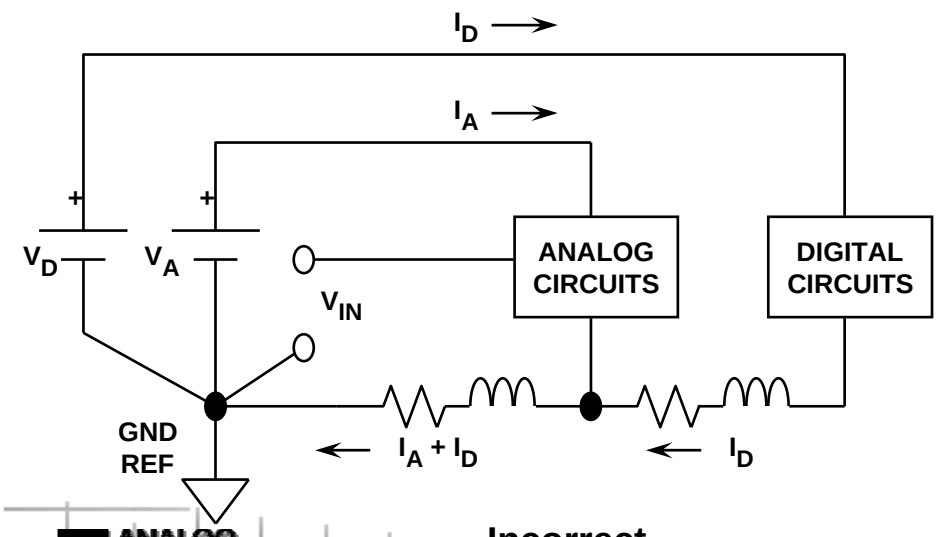
Grounding Data Acquisition System

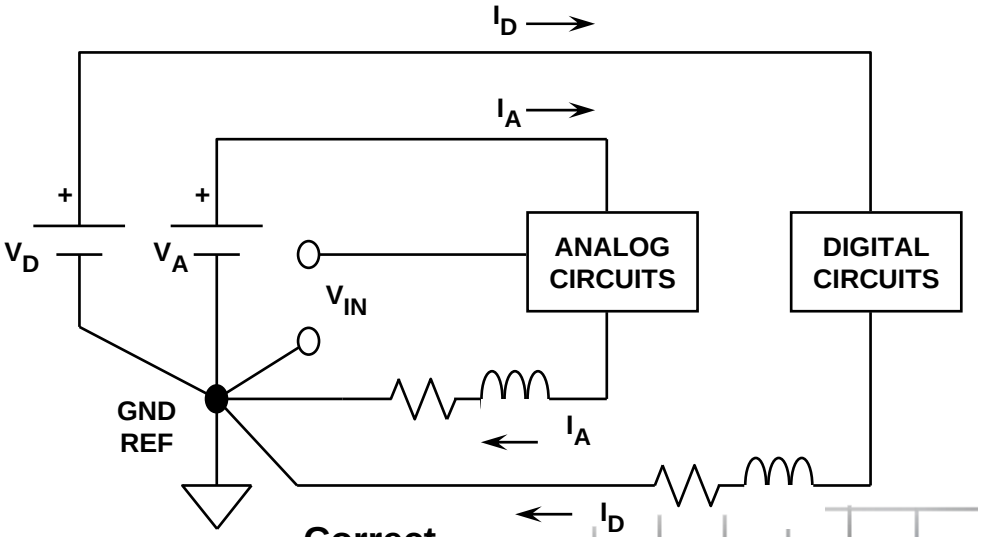
ADI

ANALOG DEVICES

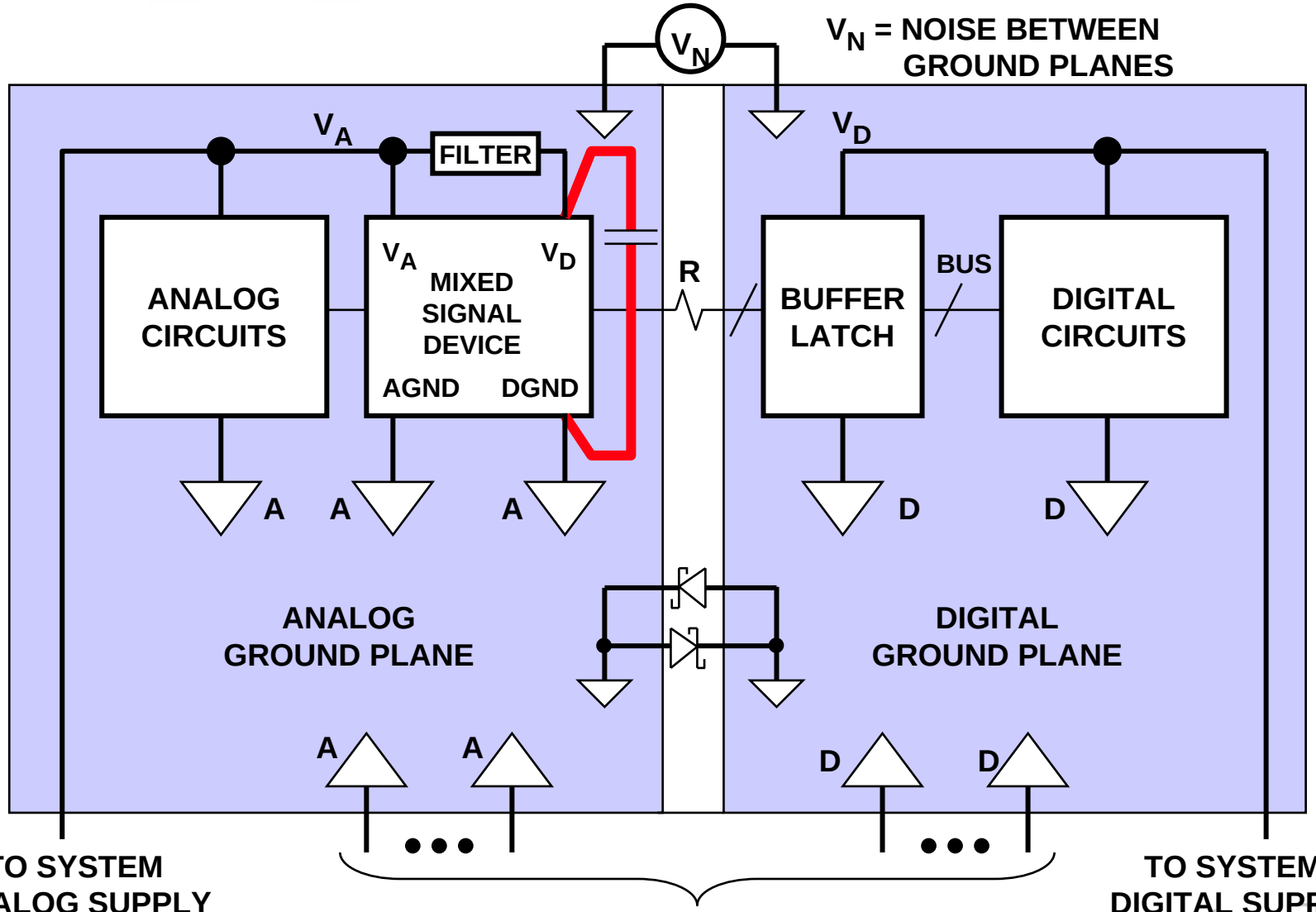
Digital Currents Flowing in Analog Return Path Create Error Voltages



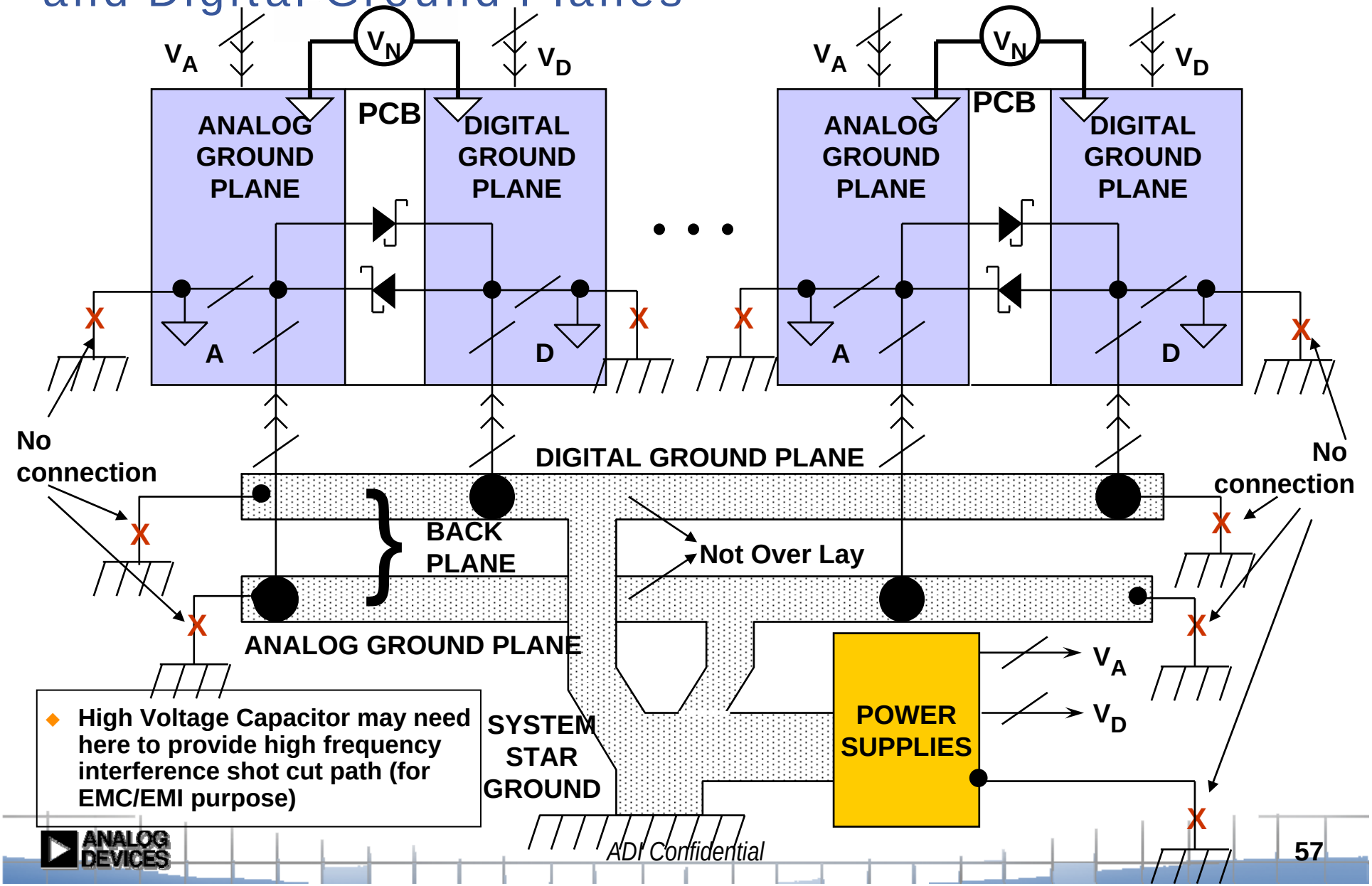


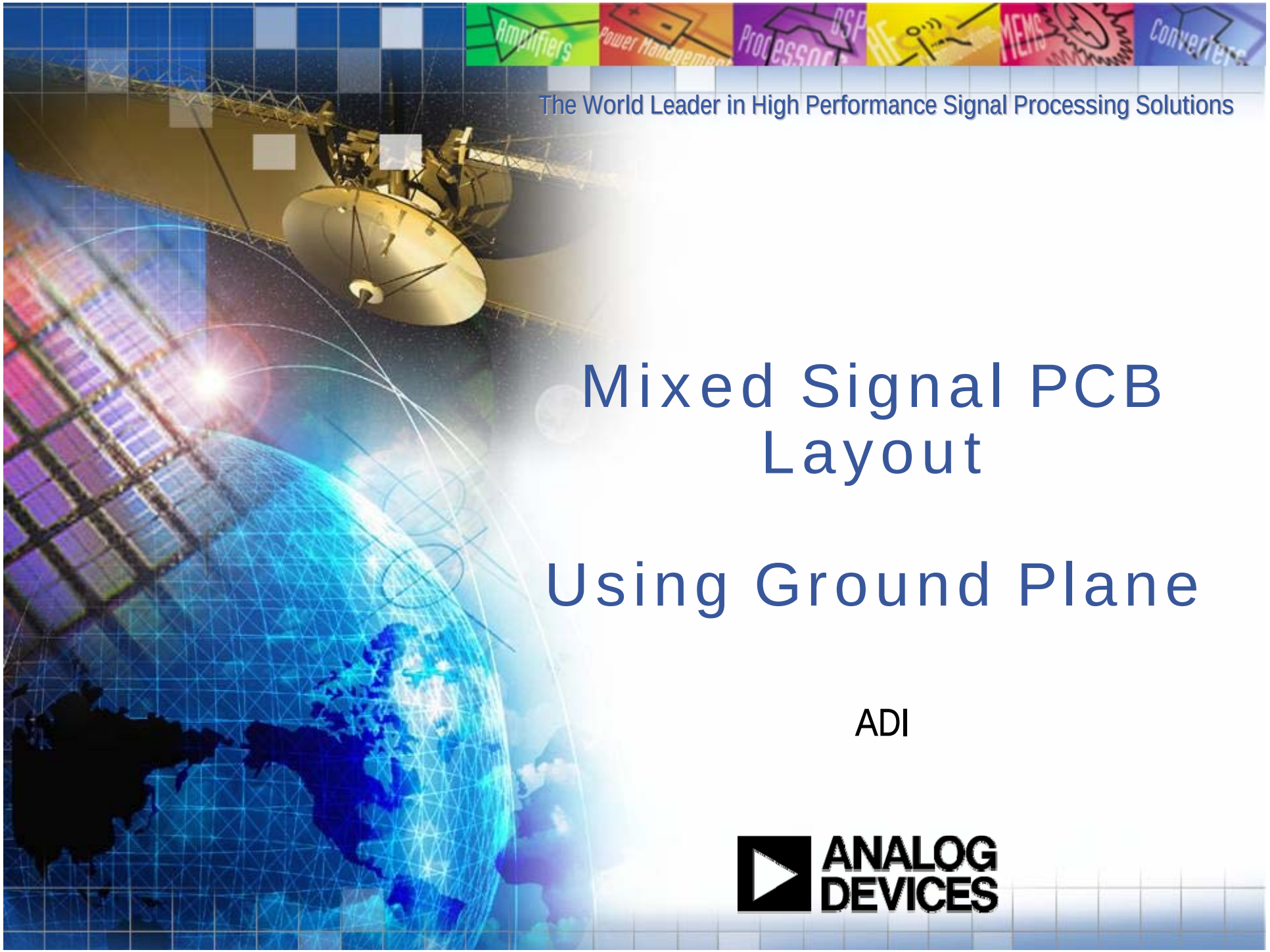


Grounding Mixed Signal ICs with Low Internal Digital Currents: Multiple PC Boards



Star Ground System which has Separated Analog and Digital Ground Planes





Mixed Signal PCB Layout

Using Ground Plane

ADI

ANALOG DEVICES

Characteristics of Ground Planes

- **Digital Radios frequently have high speed digital logic on the same board as high gain RF electronics.**
- **Shielding and Grounding are significant aspects of the receiver design.**
  - **Radiation should be shielded at the source**
  - **Ground currents should be returned to their source**
  - **Supply currents should take the path of least resistance & inductance back to the source**
- **Minimum 1 whole ground layer**
  - **One entire PCB side (or layer) is a continuous ground conductor**
    - Gives minimum ground resistance and inductance, but itn't always sufficient to solve all ground problems.
    - Breaks in ground planes can improve or degrade circuit performance – there is no general ruls
  - **Eliminate the possibility ground loops**
  - **Careful attention should be paid to layout to ensure that digital return currents do not flow through analog section of the board.**

Ground plane acts as a shield

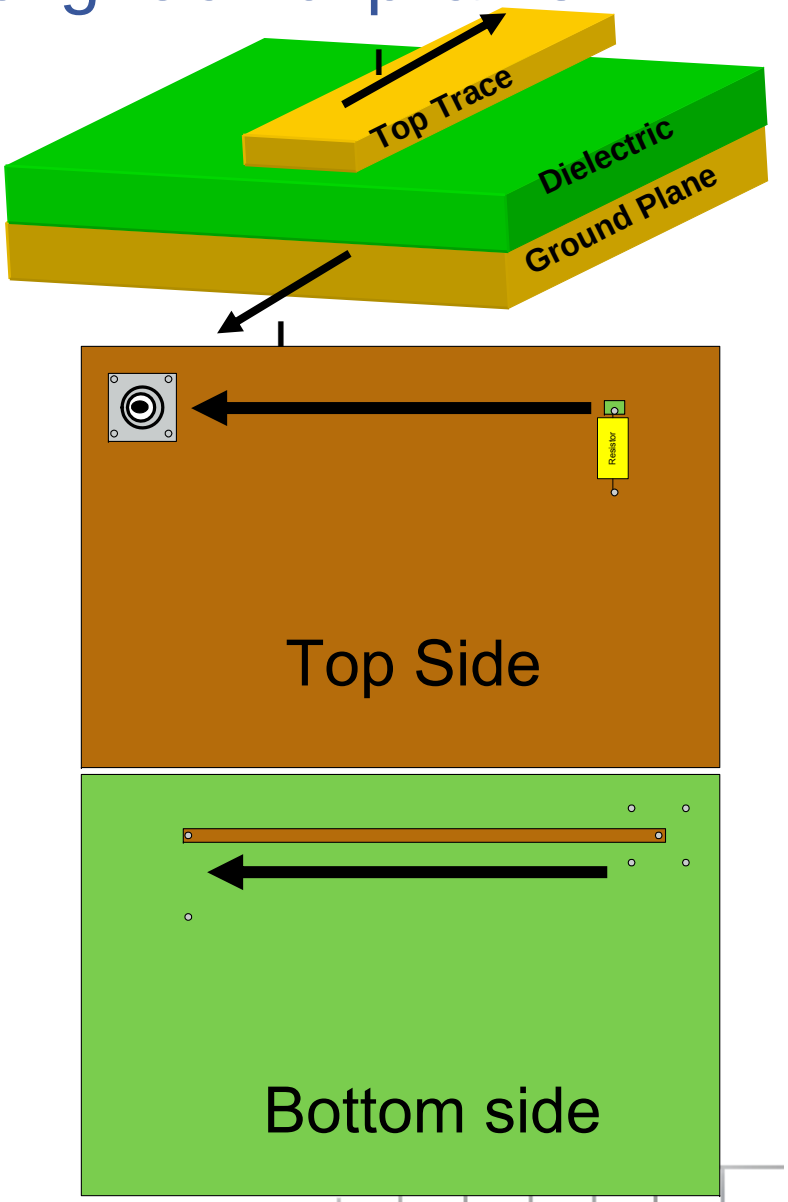
- **Using Mulit-layer (>=4) with ground and voltage plane**

How to make full use of your Ground Plane?

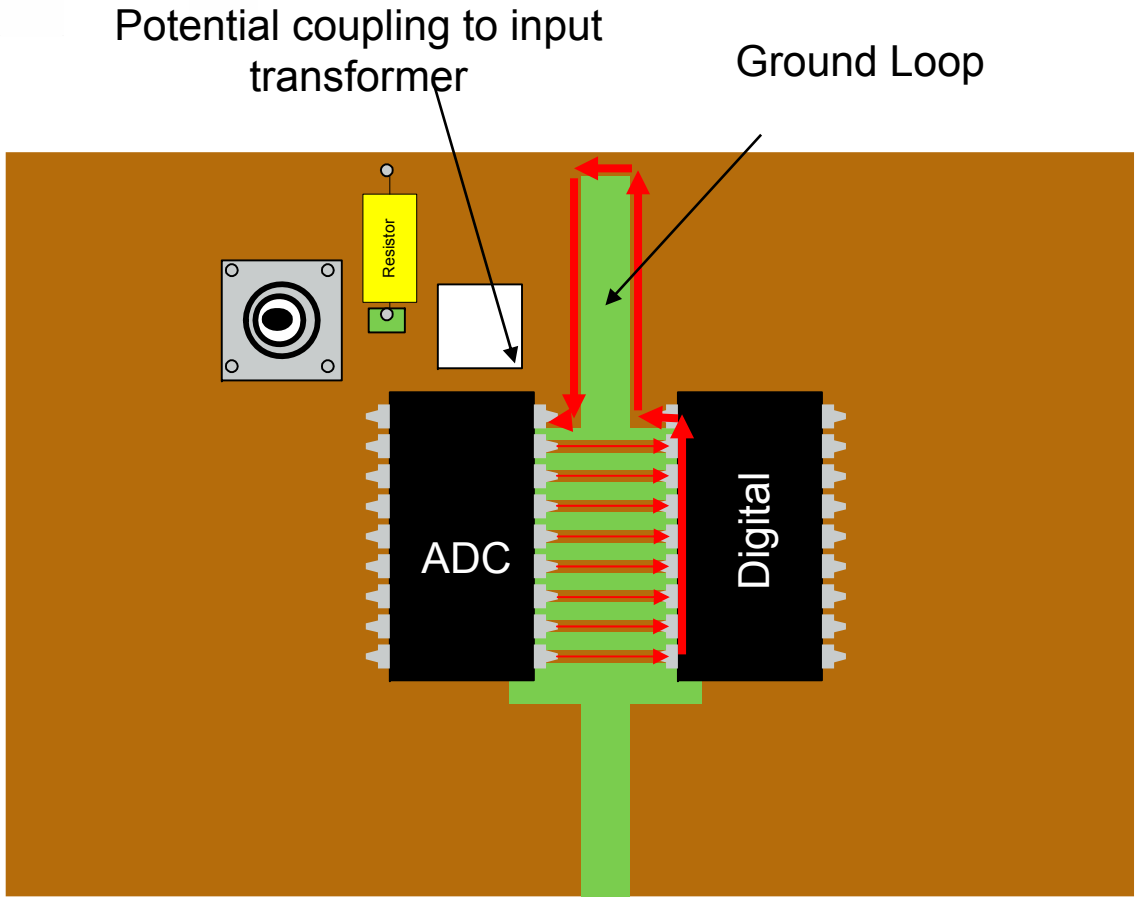
- **Provide as much ground plane as possible**
  - Especially under traces that operate at high frequency
- **Use thickest metal as feasible**
  - Reduces resistance and provides improved thermal path
  - Helps reduce resistive losses due to skin effect
- **Mount components that conduct fast rise times or high frequencies as close to the board as possible**
  - Minimize use of leaded components
- **Try to single-point the critical components into the ground plane to avoid voltage drops.**
- **Provide as much ground plane as possible**
  - Especially under traces that operate at high frequency
- **Use thickest metal as feasible**
  - Reduces resistance and provides improved thermal path)
  - Helps reduce resistive losses due to skin effect
- **Mount components that conduct fast rise times or high frequencies as close to the board as possible**
  - Minimize use of leaded components
- **Try to single-point the critical components into the ground plane to avoid voltage drops.**
  - Confine Analog circuitry to one section and digital circuitry to another.
  - Avoid running digital and analog tracks close to each other, this will help avoid coupling digital noise into analog lines.

Grounding example of solid ground plane

- **Single GND Layer for High Speed Converters PCB board.**
  - Cover empty space of TOP / Bottom layer with GND, but no small unconnected island.
  - Via to connect 2 or more GND layer, as many as possible but do not cut some plane to pieces.
- **Example**
  - The top layer is solid ground.
  - The Bottom has a trace connecting the RF connector to the load.
  - Return current flows from the load back to the RF connector, directly above the trace on the opposite side.



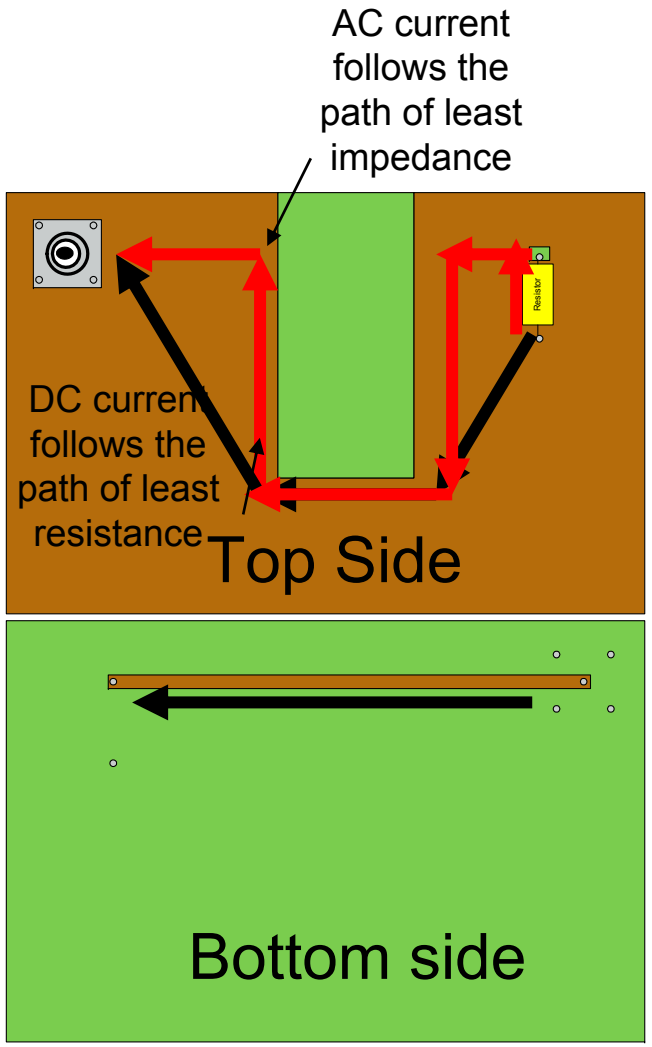
Grounding Example of split ground plane



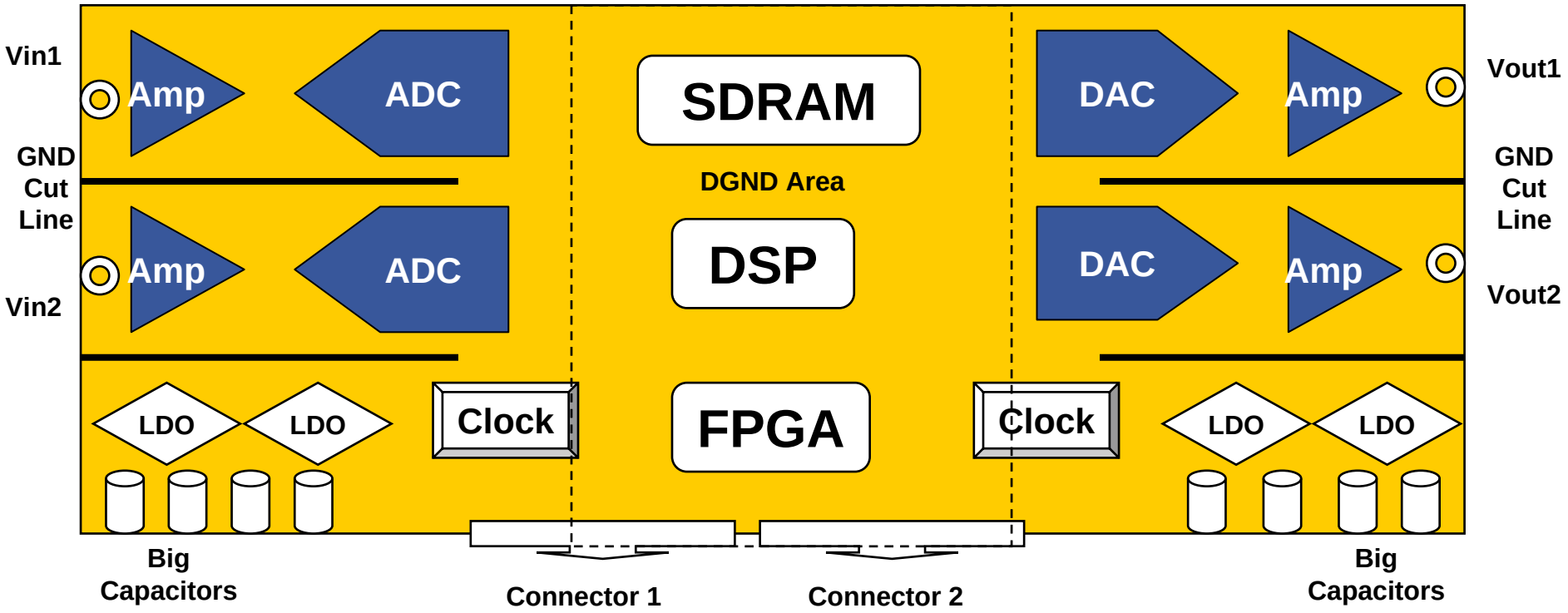
- Ground loops are introduced by splitting the two grounds.
- For example, a digital line that switches at 1 V/nS into a 10 pF load will generate a 10 mA transient.
  - If 16 lines move at the same time, this is 160 mA of switching current in the loop!

Grounding – DC current vs. AC current

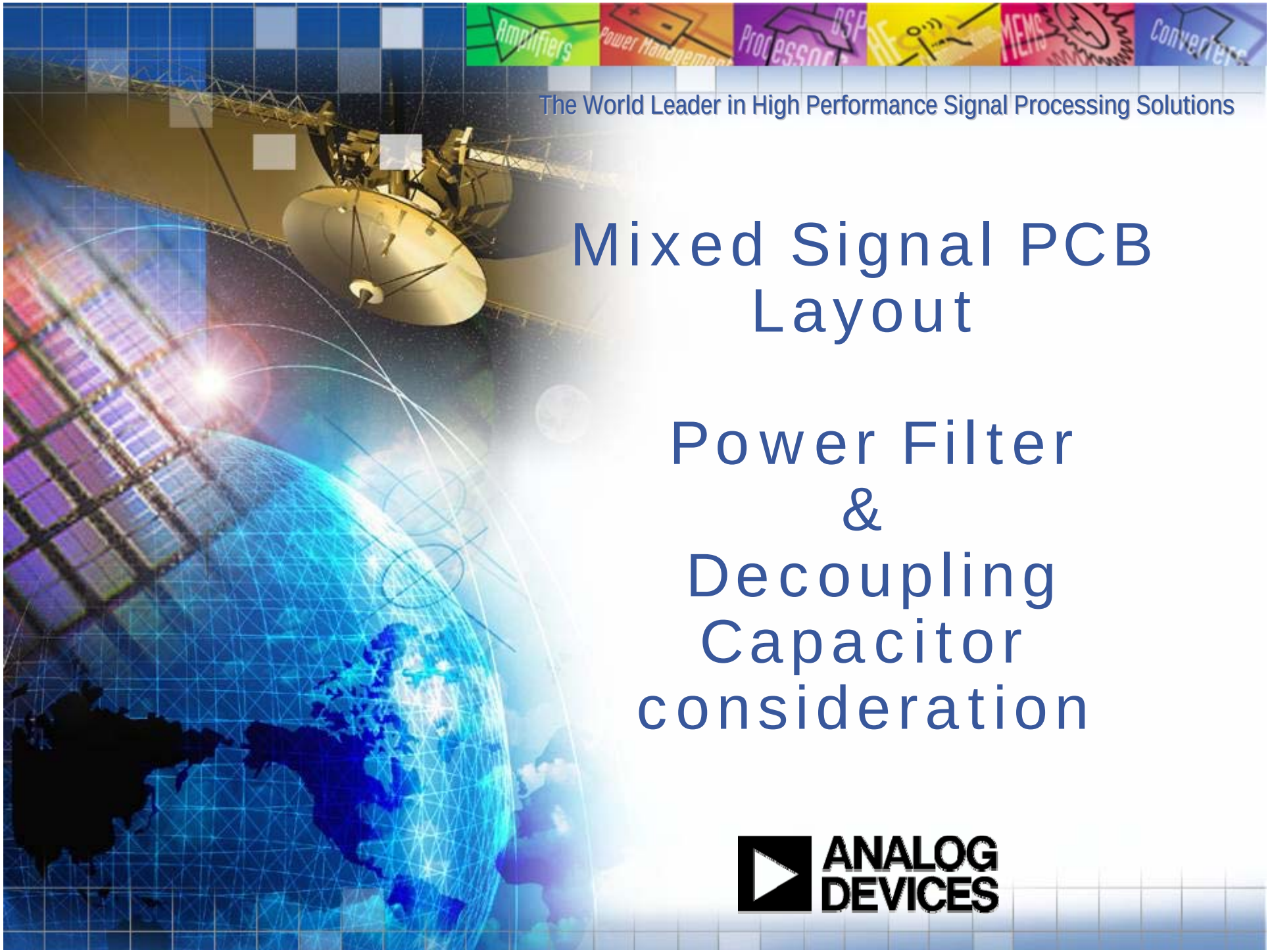
- **Single GND or Split GND plane**
  - To be simple, using signal GND layer for High Speed Converts layout (>10MHz), no AGND and DGND layer difference.
  - Separated AGND and DGND and connect with signal point only applies in low speed design (less than 1MHz).
  - Some cut lines allowed to separate difference area, but connection must be bigger than Component (>10mm width). And no signal trace cross cut lines.
  - If all frequency range are consider (IE, sampling signal from DC to 50MHz), then ground layer is difficult, need case by case study.
- **Example**
  - In a broken ground or split ground, the return currents follow the path of least impedance.
  - At DC, the current follows the path of least resistance. As the frequency increases, the current follows the path of least inductance.
  - Since there is now a 'loop' the inductance can be quite high and an EMI/RFI problem can exist.



Cut lines with good Component placement



- Separate Analog area, mixer signal area and pure digital area.
- No cross over of input and out put.
- Clock area is an independent area.
- Power supply is an independent area, especially DC-DC area.
  - DC-DC must be a corner, better in an other PCB board.
  - Cut lines must be used for DC-DC.
  - Big Capacitors must be in a corner or near PCB boundary.

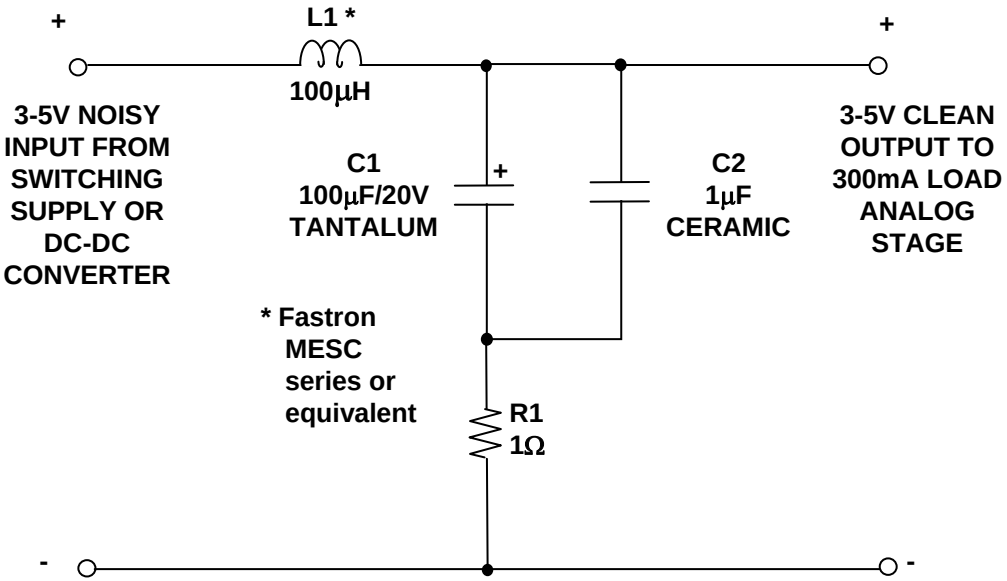


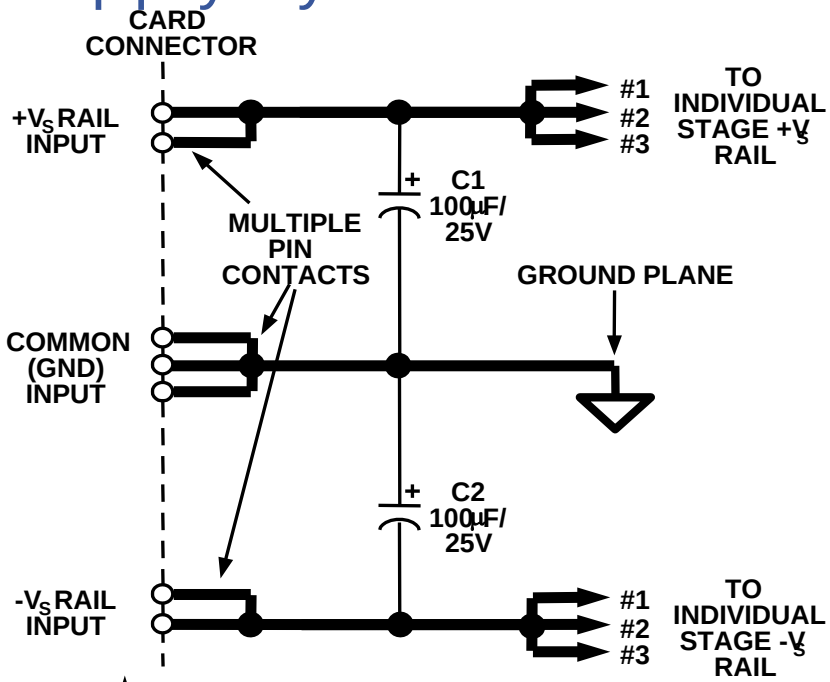
Mixed Signal PCB Layout

Power Filter & Decoupling Capacitor consideration

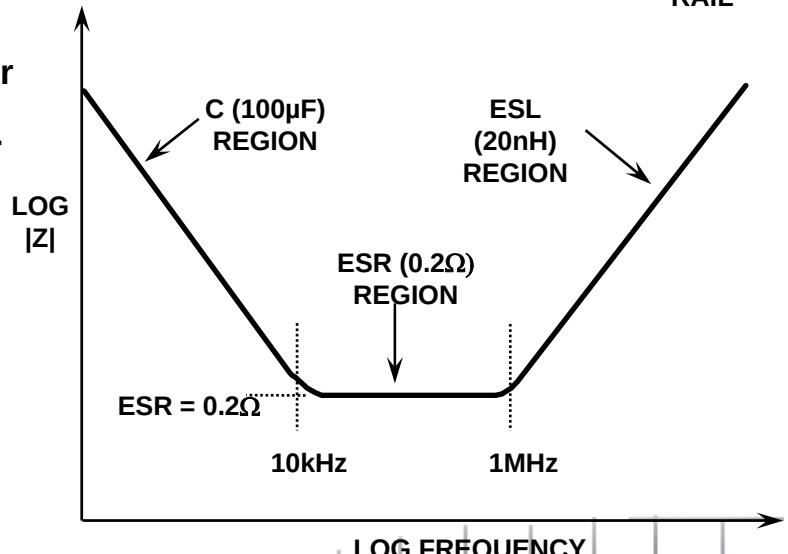
ANALOG DEVICES

Regulation priorities for power supply systems



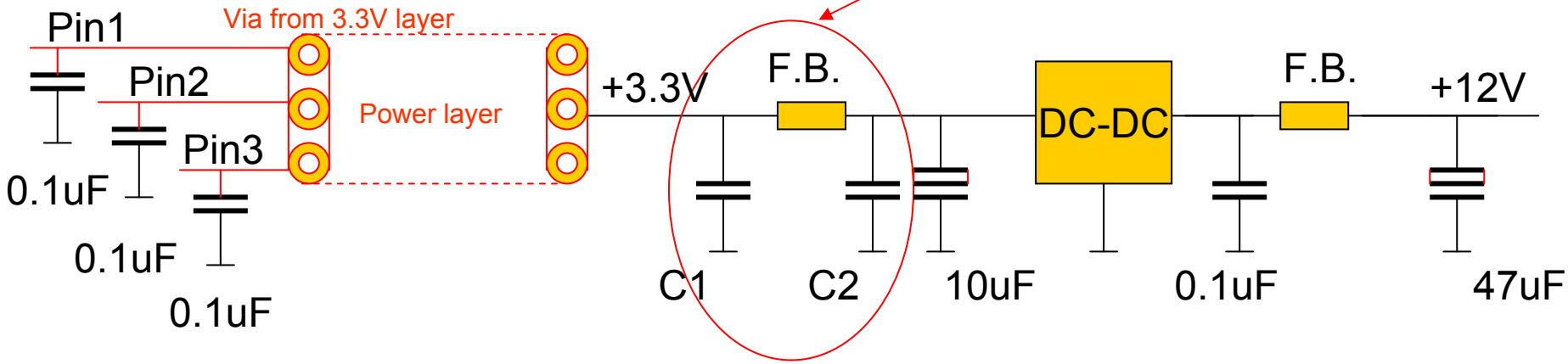


- A Card-entry Filter is useful for low medium frequency power line noise filtering in analog system
- Dual-Supply low frequency rail bypass / distribution filter for Power distribution.
- High performance analog power systems use *linear regulators*, with primary power derived from:
  - AC line power
  - Battery power systems
  - DC- DC power conversion systems
- Remember Electrolytic Capacitor Impedance vary with Frequency



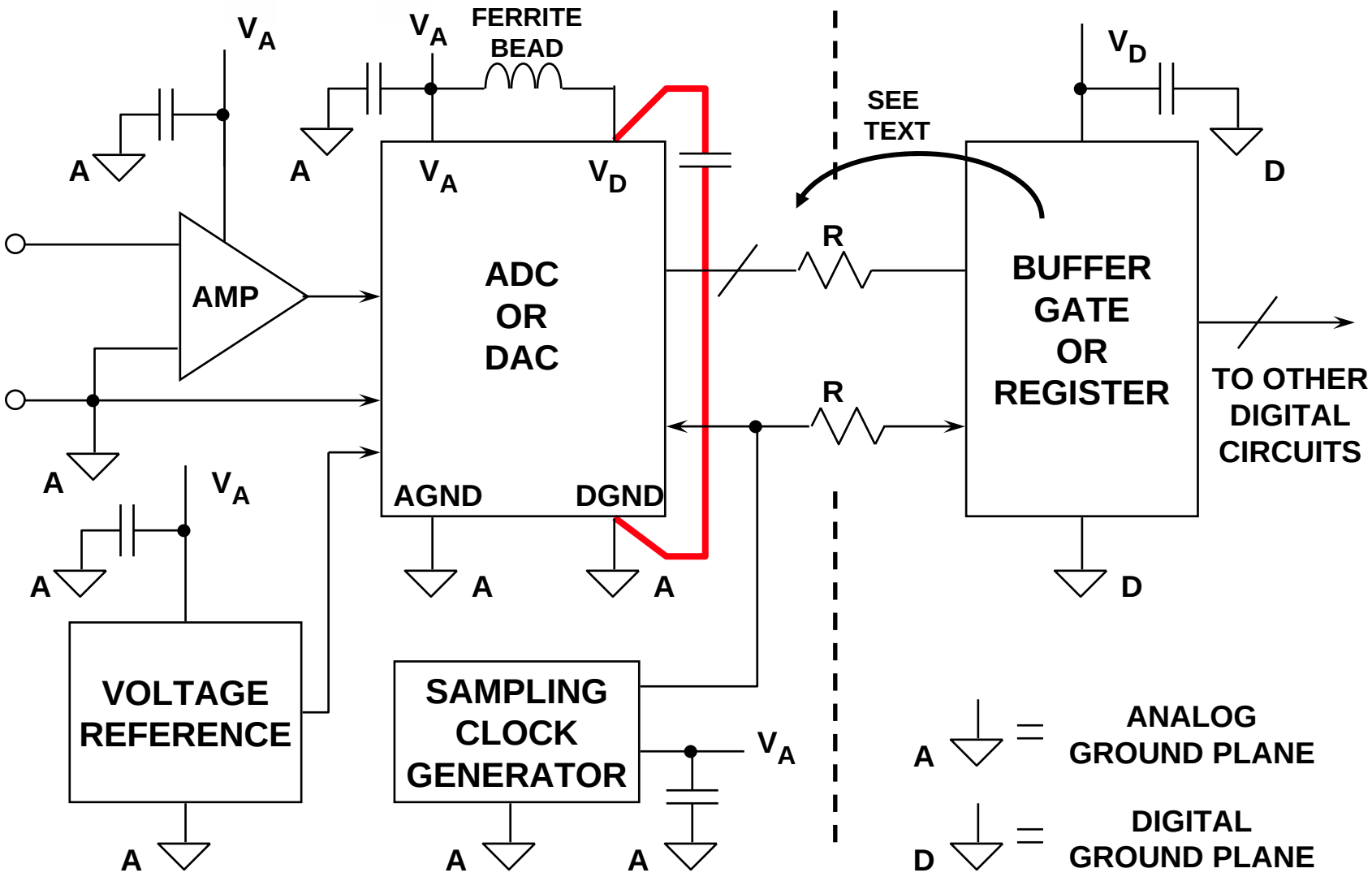
DC-DC power filter

Added the C-L-C filter to remove to switching noise generated from DC-DC.
Those components have to enclose the DC-DC Vin pin as possible.
C1, C2 need consider switch frequency (50k, 100k, 1.2M)

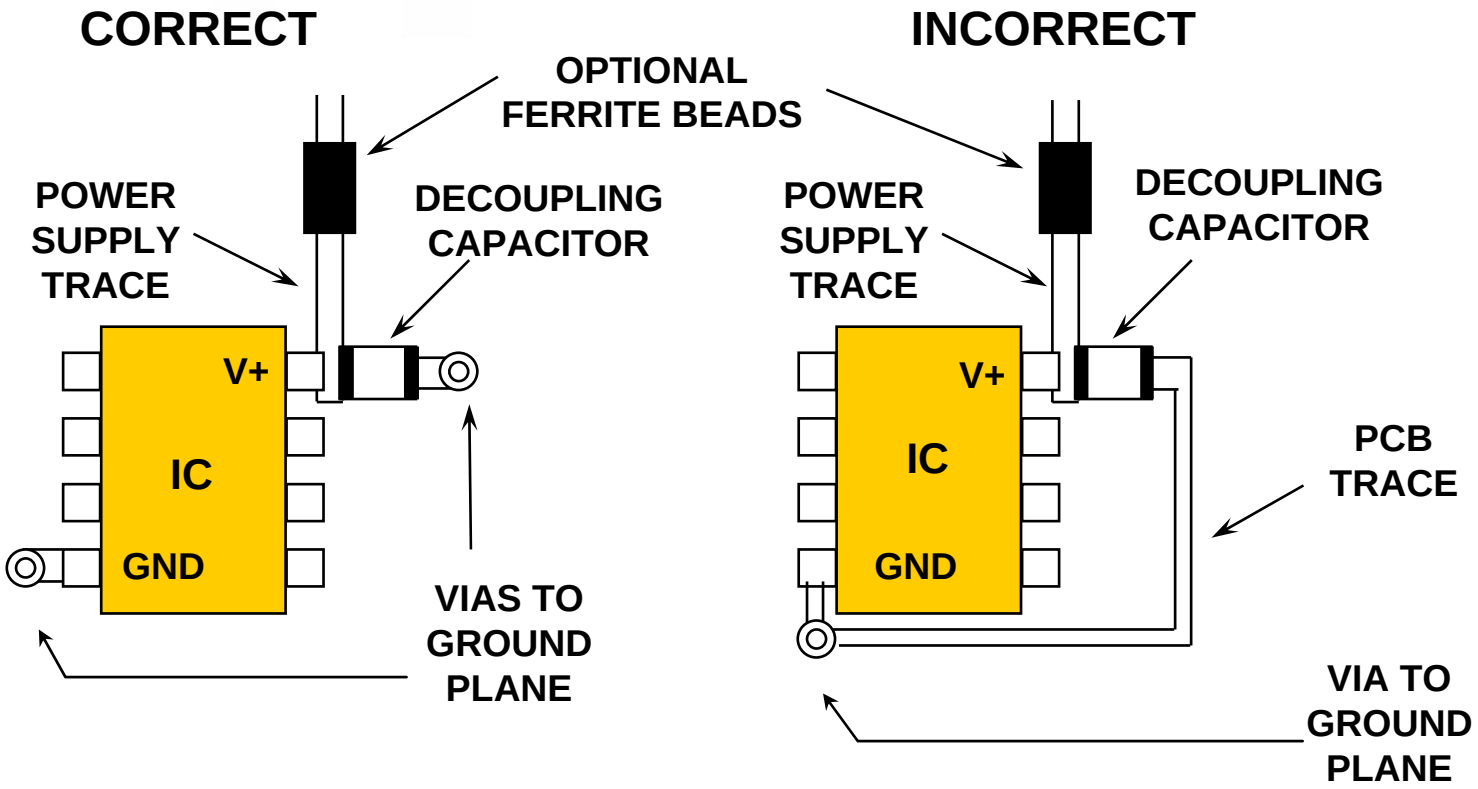


- **Switching regulators should be avoided if at all possible, but if not…**
  - **Apply noise control techniques**
  - **Use quality layout and grounding**
  - **Be aware of EMI**
  - **ADI do not suggest DC-DC power supply as analog power supply, at least add LDO**
- **DC-DC power supply can be used as digital power supply of ADC or MCV (ADuC702x)**
- **Let the DC-DC far away from ADC (or ADuC702x)**
- **The C-L-C filter near DC-DC.**
- **Still need 0.1uF on each power pin.**
- **Big 3.3V plane in Power layer helps a lot.**

Grounding and Decoupling Points



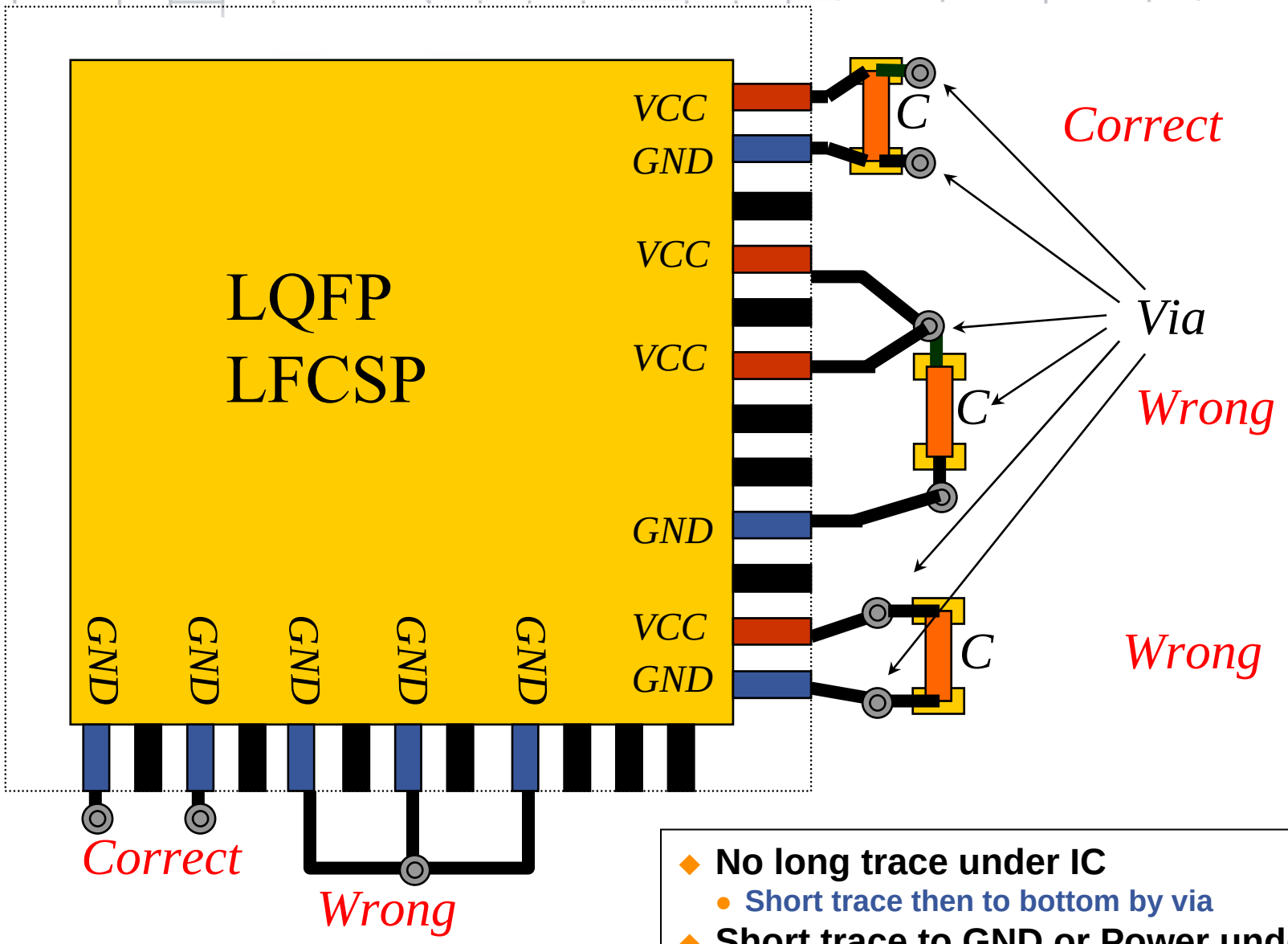
Decoupling on SOIC parts



RULE OF THUMB: VIA RESISTANCE ≈ 1mΩ, VIA INDUCTANCE ≈ 1nH

- **Localized high frequency supply filters provide optimum filtering and decoupling via short low inductance path (ground plane)**
- **Rule of Thumb:**
  - **Via resistance ≈ 1mΩ, Via inductance ≈ 1nH**

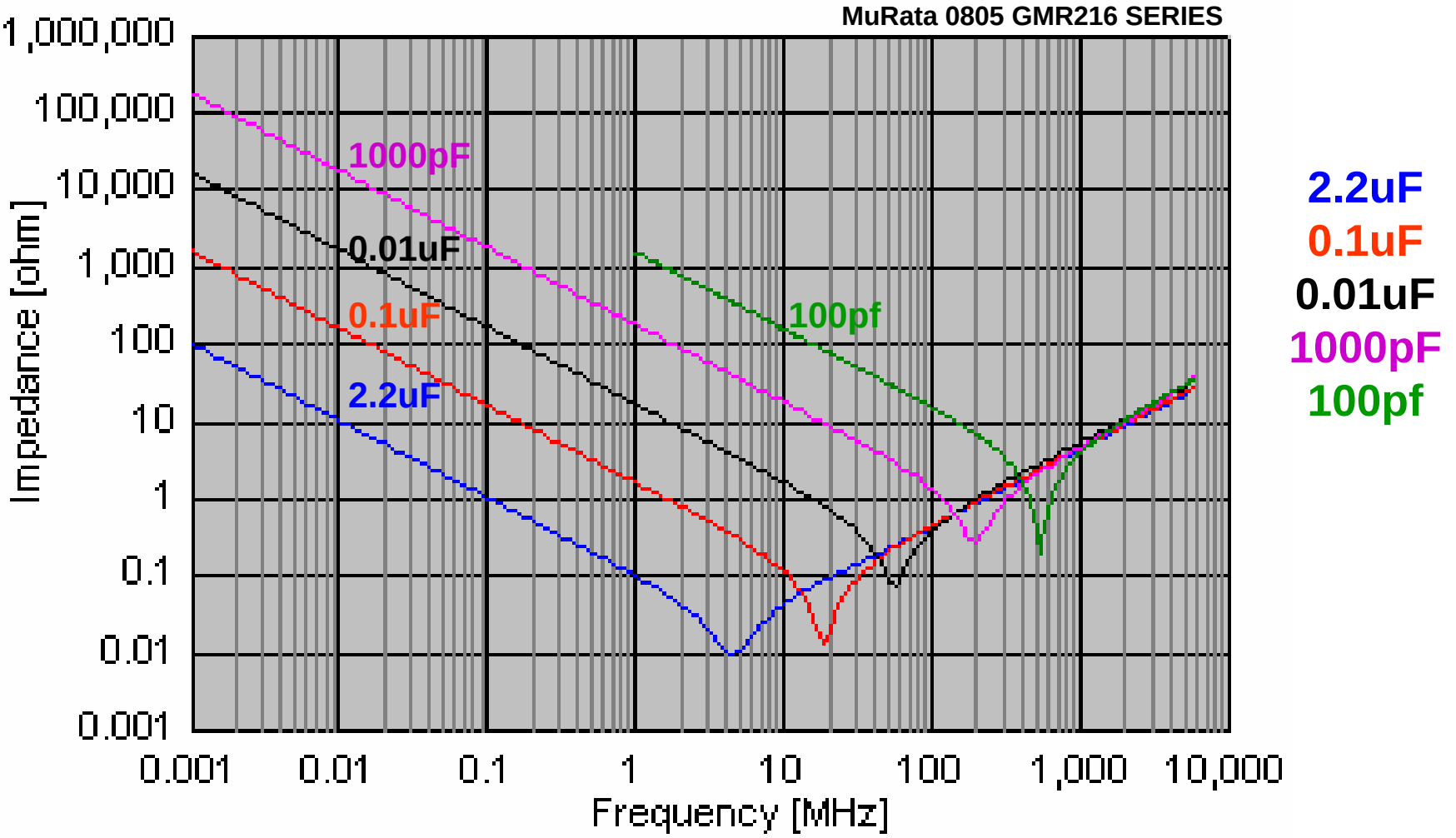
Decoupling on LQFP/LFCSP parts



Maybe your AD9779 Layout like this!

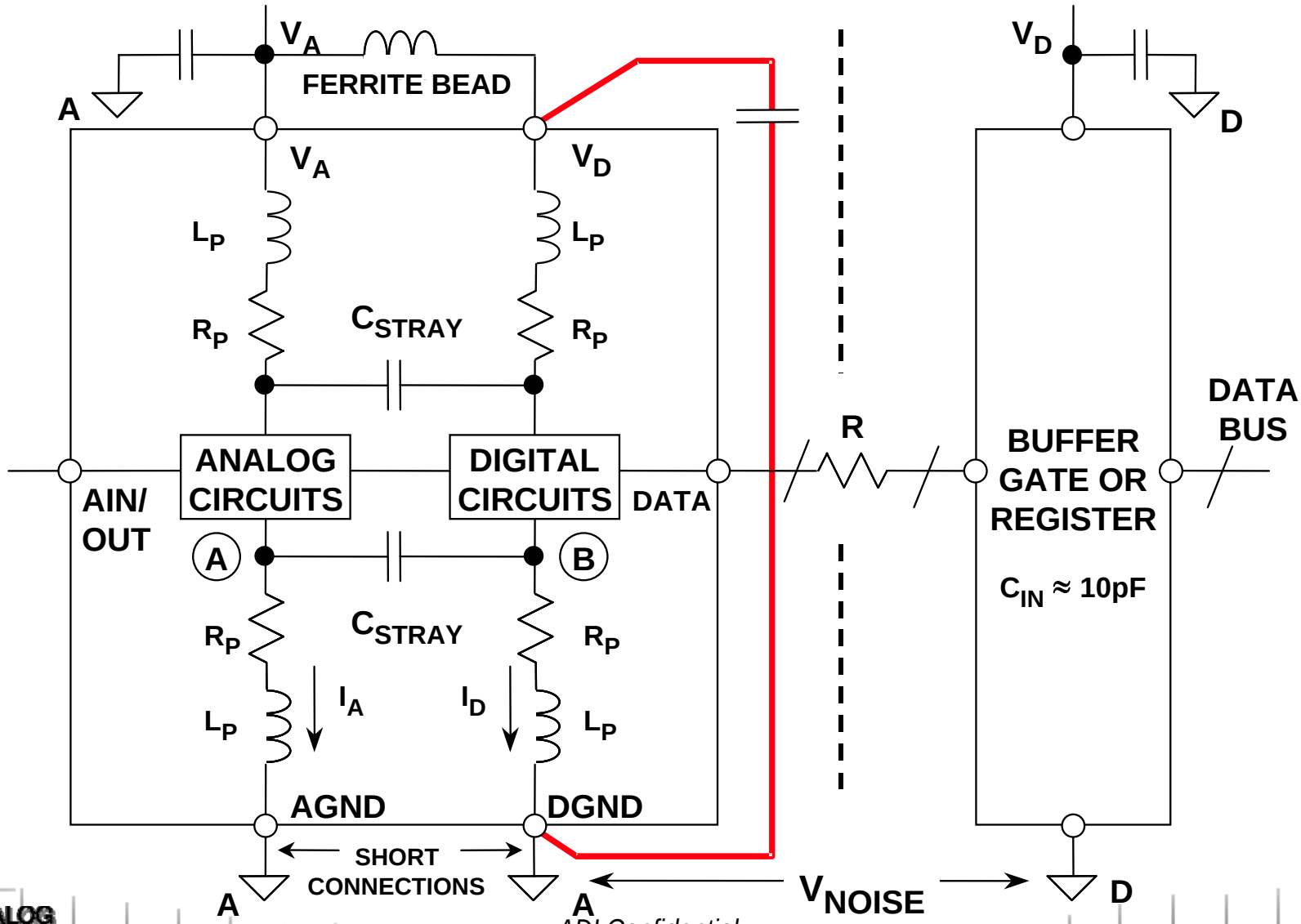
- No long trace under IC
  - Short trace then to bottom by via
- Short trace to GND or Power under IC.
- Short trace to decouple Capacitors

Different Capacitors' Impedance vs. Frequency



- **Paralleling caps reduces impedance over a wider frequency range.**
- **Put the smaller decoupling capcitor as near as possible to power pin.**

Why every power pin need decoupling Caps?

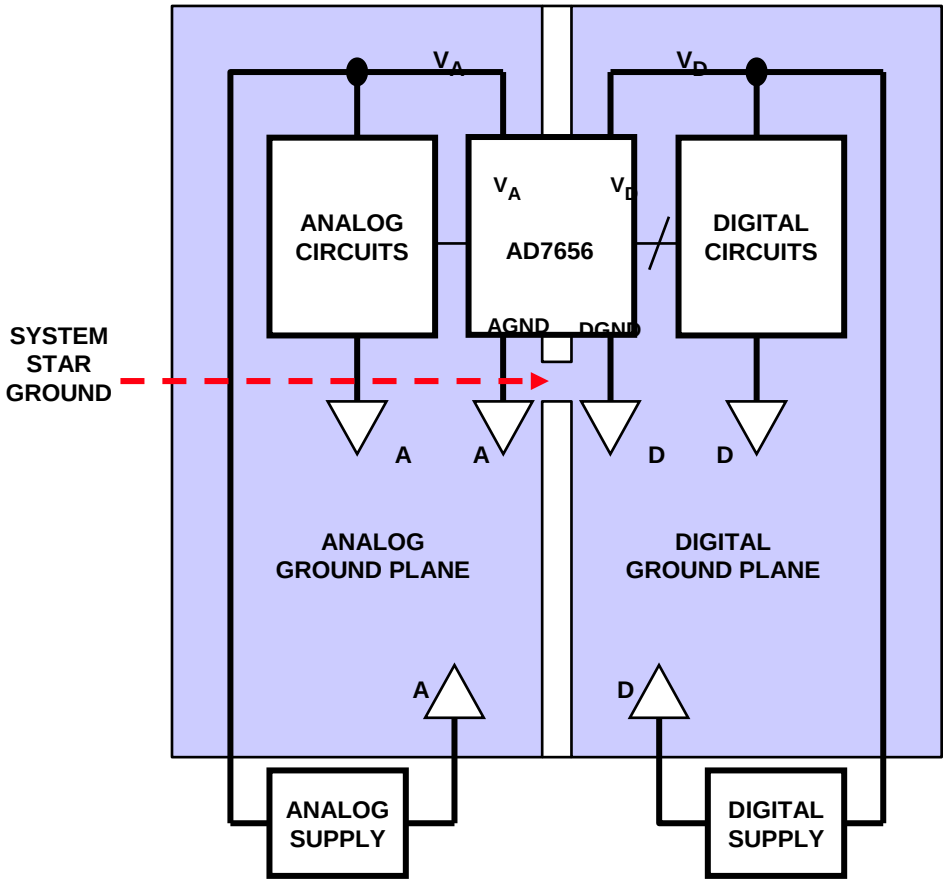


A = ANALOG GROUND PLANE

D = DIGITAL GROUND PLANE

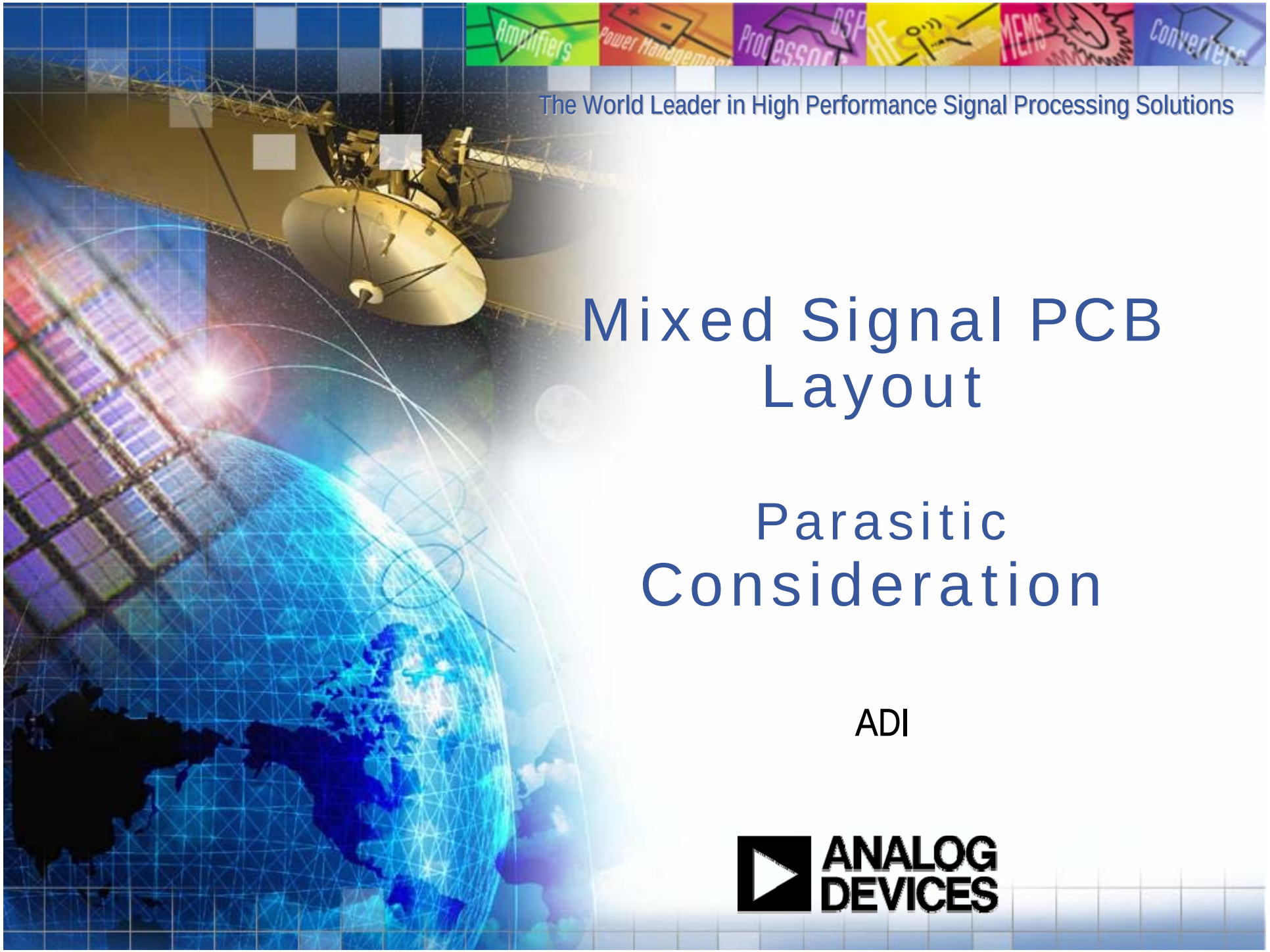
Low Speed High Resolution ADC layout Skills Example
AD7656 possible issue in Grounding and Decoupling

- **AD7656 Missing code (No codes between 0 ~ -32)**
  - Poor Grounding and poor power supply
    - **+5V AVCC must be very stable**
    - **Half AVCC power plan, half DVCC power plan. Use wide trace (>1mm) for +/-12V power supply on bottom layer, aviod +/-12V cut AVCC power layer to pieces**
    - **Single point connect AGND and DGND**
  - Insufficient decouple
    - **220uF Decoupling Cap for each AD7656**
    - **10uF + 0.1uF for each AVCC pin (8pins total)**
    - **Short but wide trace from Via to AVCC pin**
    - **Leadless capacitor layout**



Summary of Power Supply Bypassing & decoupling

- **Place bypass caps as close to the power supply pins as possible**
- **SMT ferrite beads are very effective in reducing ripple content**
- **High Frequency requires ground plane**
  - **Minimize parasitics**
- **Use stable, well behaved components**
  - **Low drift and low ESR**
- **Completely Analytical Approaches can be difficult**
  - **Prototyping is required for optimal results**
- **Use a combination of paralleled capacitors to achieve frequency rejection of unwanted noise across a wide bandwidth**



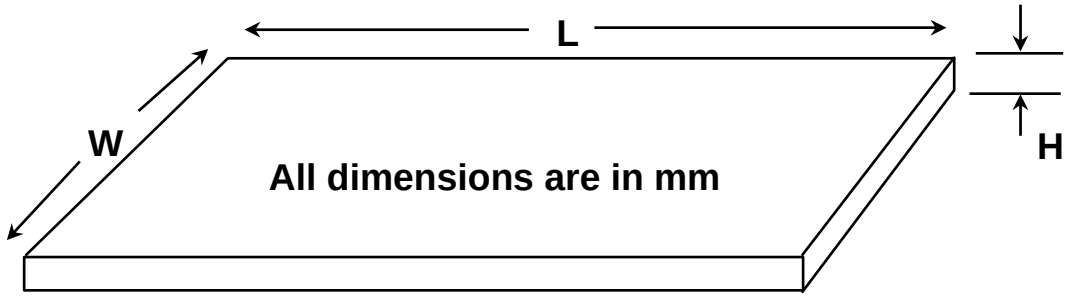
Mixed Signal PCB Layout

Parasitic Consideration

ADI

ANALOG DEVICES

Approximate Trace Inductance



$$\text{STRIP INDUCTANCE} = 0.0002L\left[\ln\left(\frac{2L}{W+H}\right) + 0.2235\left(\frac{W+H}{L}\right) + 0.5\right]\ \mu H$$

1cm of 0.25 mm PC track has an inductance of 9.59 nH

(H = 0.038mm, W = 0.25mm, L = 1cm)

Example

L= 2.54cm =25.4mm, W = 0.25mm

H = .035mm (1oz copper)

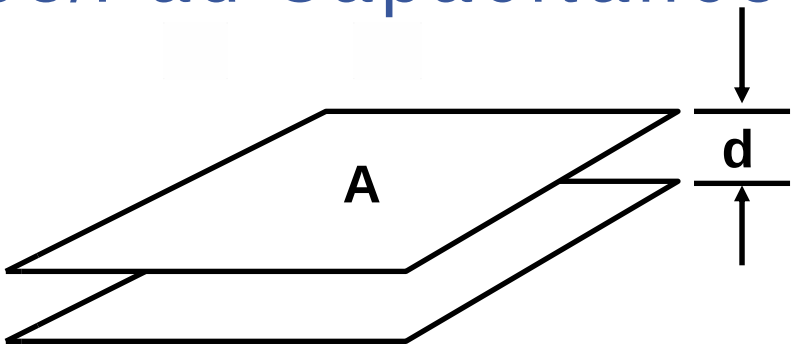
Strip Inductance = 28.8nH

At 10MHz Z_L = 1.86 Ω a 3.6% error in a 50Ω system

Minimize Inductance

1) Use Ground plane
2) Keep length short: Halving the length reduces inductance by 44%
3) Doubling width only reduces inductance by 11%

Trace/Pad Capacitance



$$C = \frac{0.00885\ E_r\ A}{d}\ \text{pF} \qquad C = \frac{kA}{11.3d}$$

A = plate area in mm^2

d = plate separation in mm

E_r = dielectric constant relative to air

K = relative dielectric constant

- Most common PCB type uses 1.5mm glass-fiber epoxy material with E = 4.7
- Capacity of PC track over ground plane is roughly 2.8pF/cm

Reduce Capacitance

1) Increase board thickness
2) Reduce trace/pad area
3) Remove ground plane

Example: Pad of SOIC

L = 0.2cm W = 0.063cm

K= 4.7

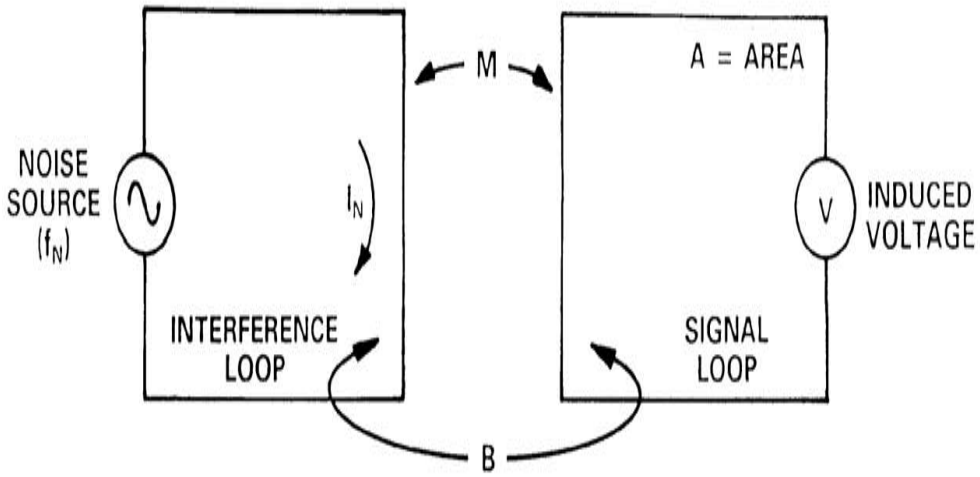
A = 0.126cm^2

d = 0.073cm

C = 0.072pF

BASIC PRINCIPLES OF COUPLING

INTERFERENCE CIRCUIT **SIGNAL CIRCUIT**

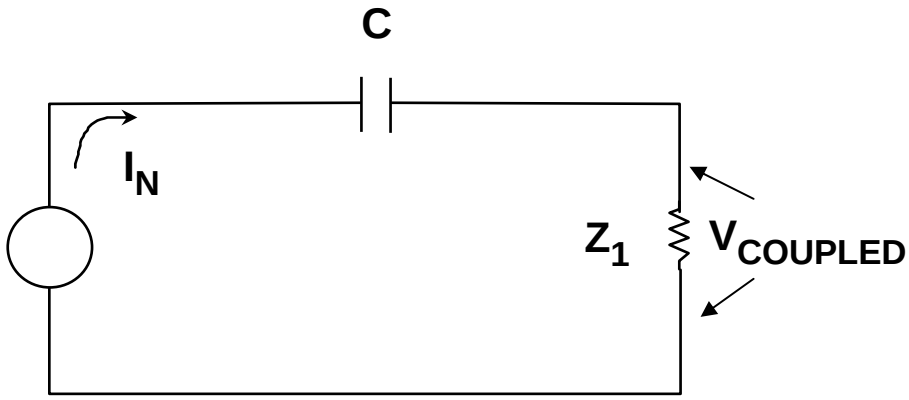


M = MUTUAL INDUCTANCE
B = MAGNETIC FLUX DENSITY
A = AREA OF SIGNAL LOOP
$\omega_N = 2\pi f_N$ = FREQUENCY OF NOISE SOURCE

V = INDUCED VOLTAGE = $\omega_N M I_N = \omega AB$

BASIC PRINCIPLES OF INDUCTIVE COUPLING

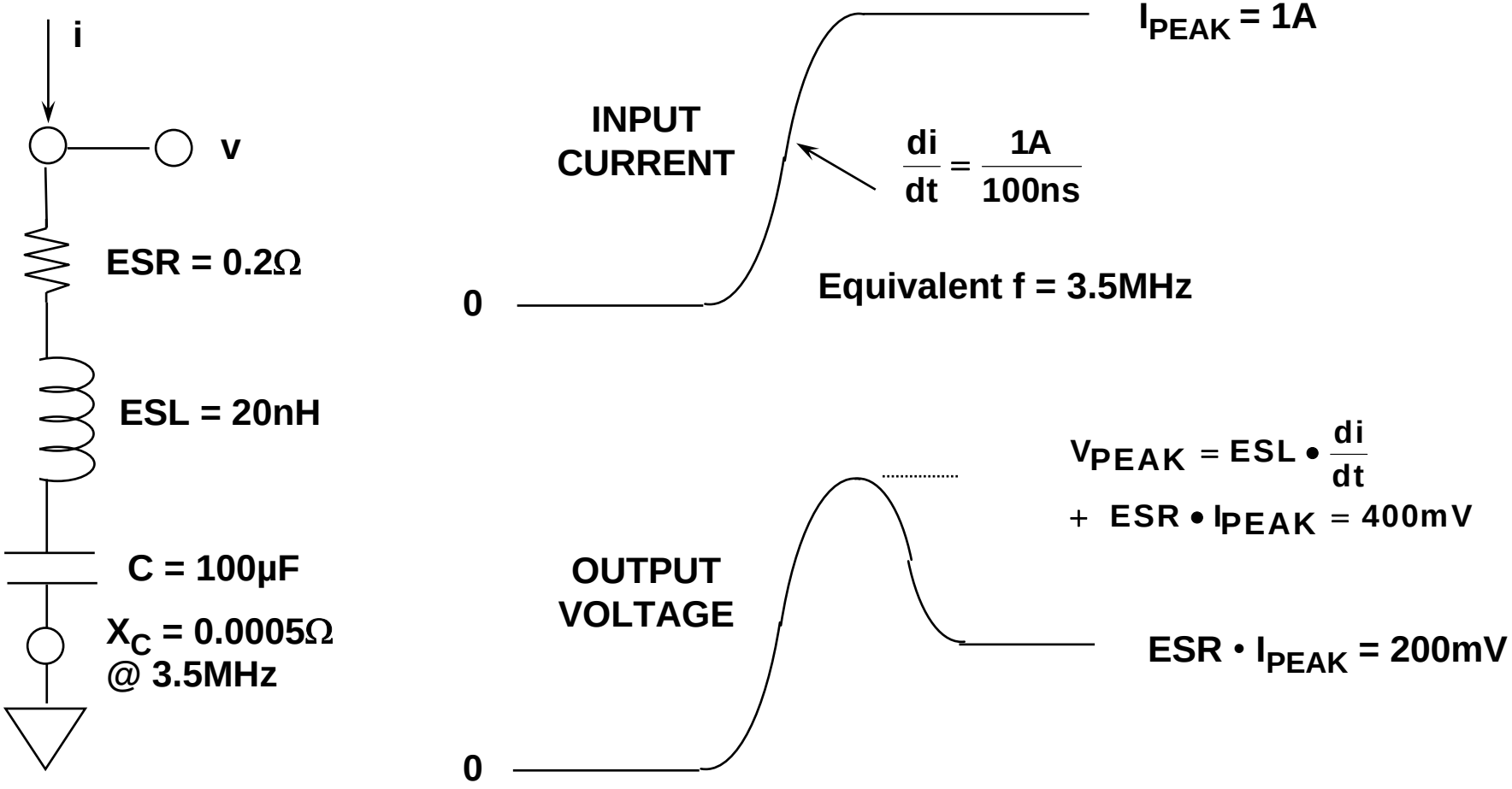
CAPACITIVE COUPLING EQUIVALENT CIRCUIT MODEL



Z_1 = CIRCUIT IMPEDANCE
Z2 = 1/jωC

$$V_{COUPLED} = V_N \left(\frac{Z_1}{Z_1 + Z_2} \right)$$

CAPACITOR EQUIVALENT CIRCUIT AND RESPONSE TO INPUT CURRENT PULSE



Via Parasitics

Via Inductance

$$L = 2h\left[\ln\left(\frac{4h}{d}\right)+1\right] \; nH$$

L = inductance of the via, nH

H = length of via, cm

D = diameter of via, cm

Consider a power supply pin of an op amp that goes through a via to the power plane of an 0.157 cm thick board, the diameter of the via is 0.041 cm

$$L = 2(0.157)\left[\ln\left(\frac{4(0.157)}{0.041}\right)+1\right]$$

L = 1.2nh

Via Capacitance

$$C = \frac{0.55\varepsilon_r TD_1}{D_2 - D_1}$$

D_2 = diameter of clearance hole in the ground plane, cm

D_1 = diameter of pad surrounding via, cm

T = thickness of printed circuit board, cm

ε_r = relative electric permeability of circuit board material

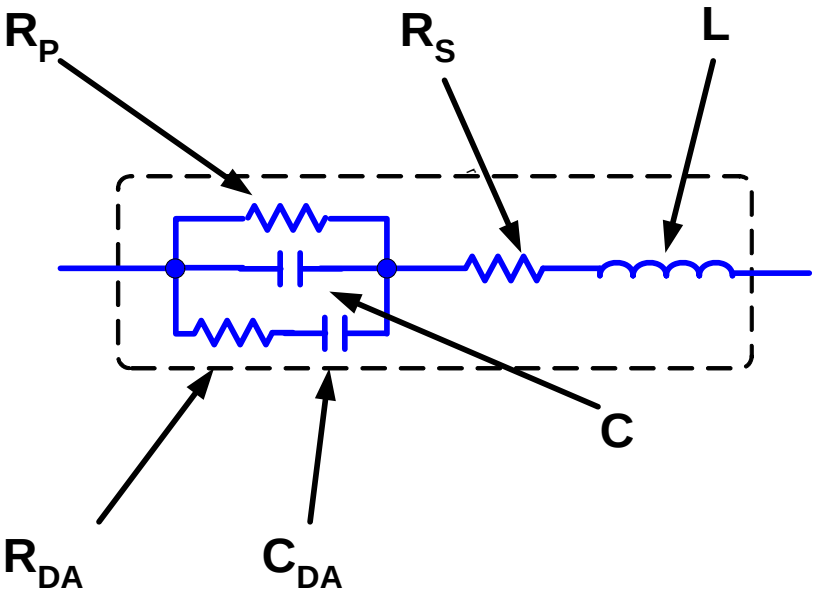
C = parasitic via capacitance, pF

Consider a signal coming from the back of the board to the top of the board through a via. Board thickness = 0.157cm, D_1=0.071cm D_2 = 0.127

C = 0.51pf

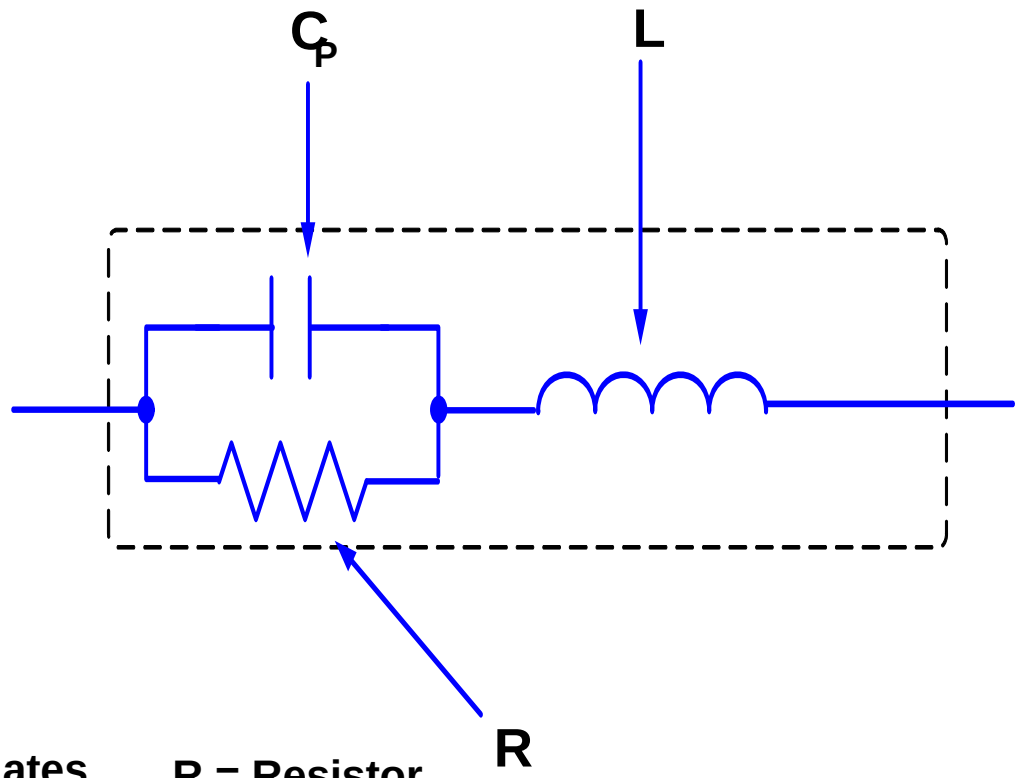
Parasitic Model

Capacitor Parasitic Model



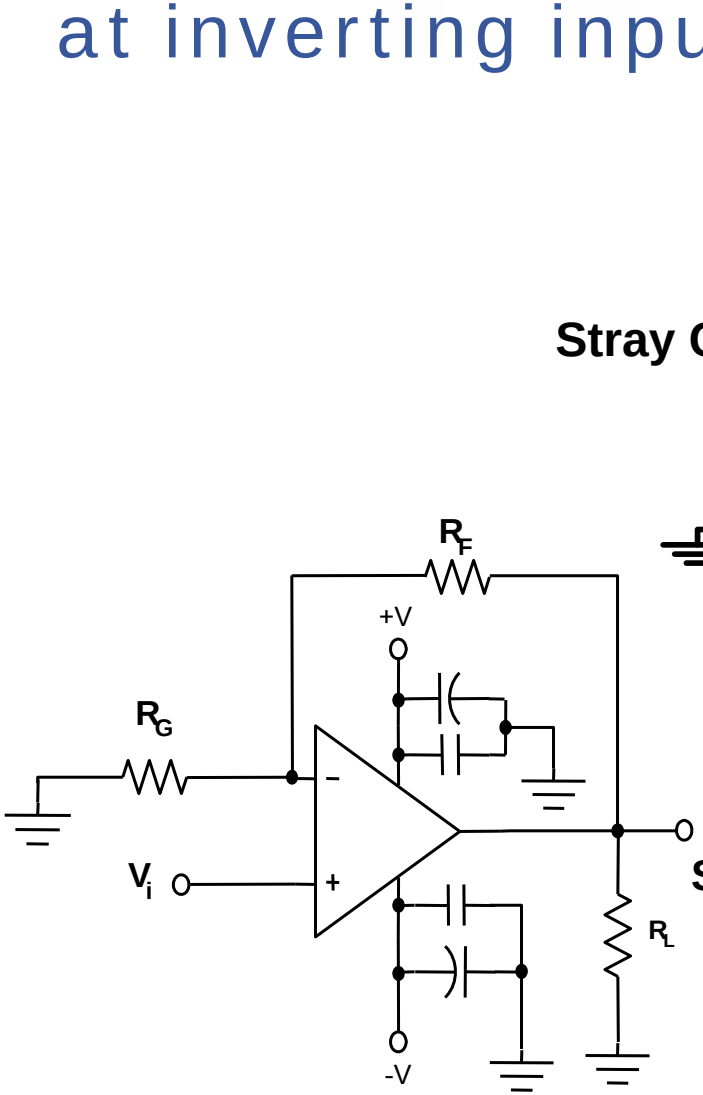
C = Capacitor
R_P = insulation resistance
R_S = equivalent series resistance (ESR)
L = series inductance of the leads and plates
R_{DA} = dielectric absorption
C_{DA} = dielectric absorption

Resistor Parasitic Model

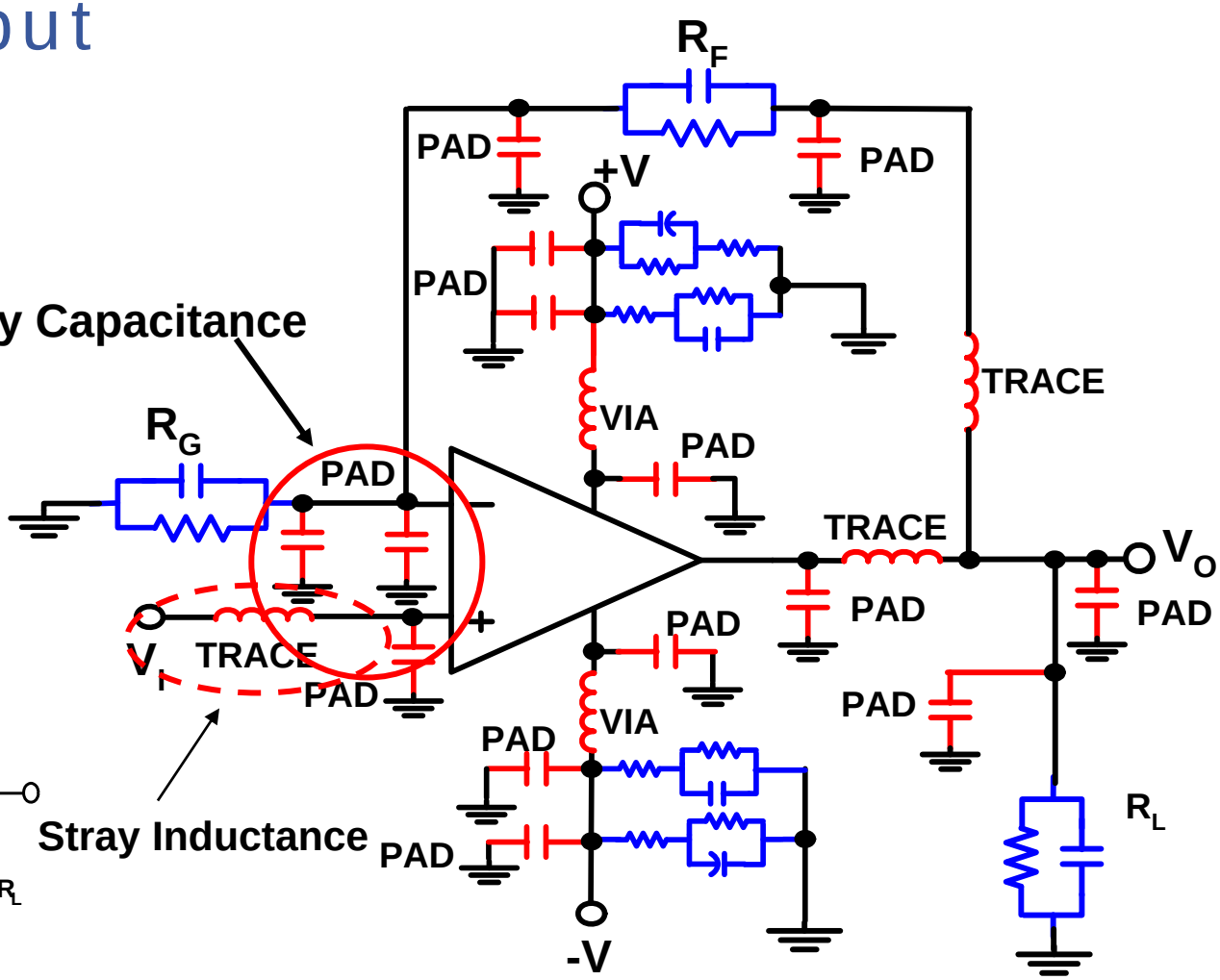


R = Resistor
C_P = Parallel capacitance
L= equivalent series inductance (ESL)

Stray Capacitance & Stray Inductance at inverting input

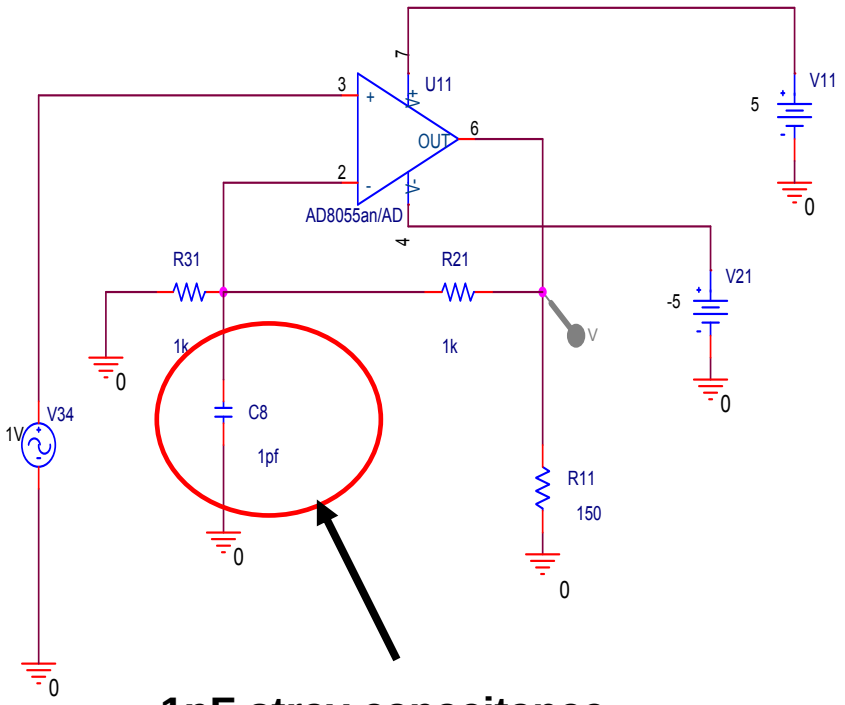


Low Frequency Op Amp Schematic

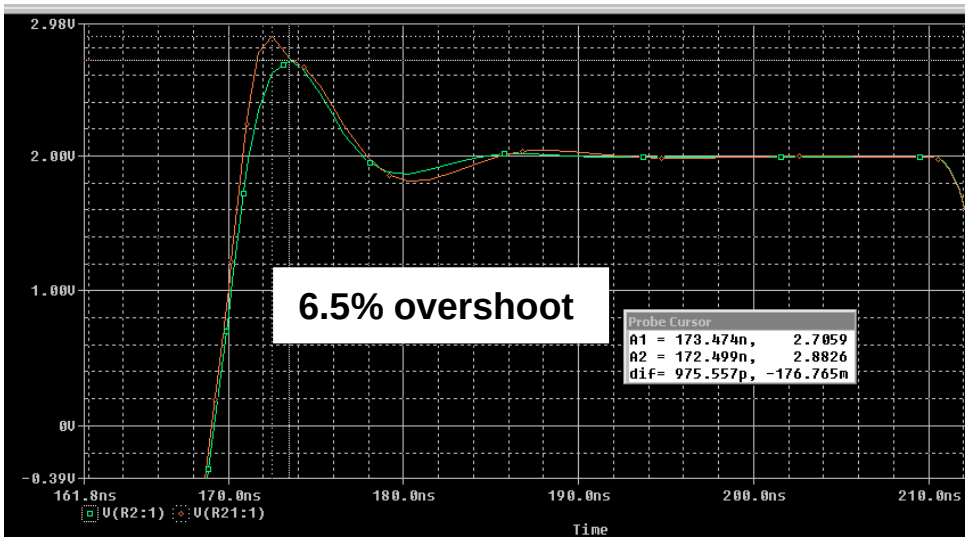


High Frequency Op Amp Model

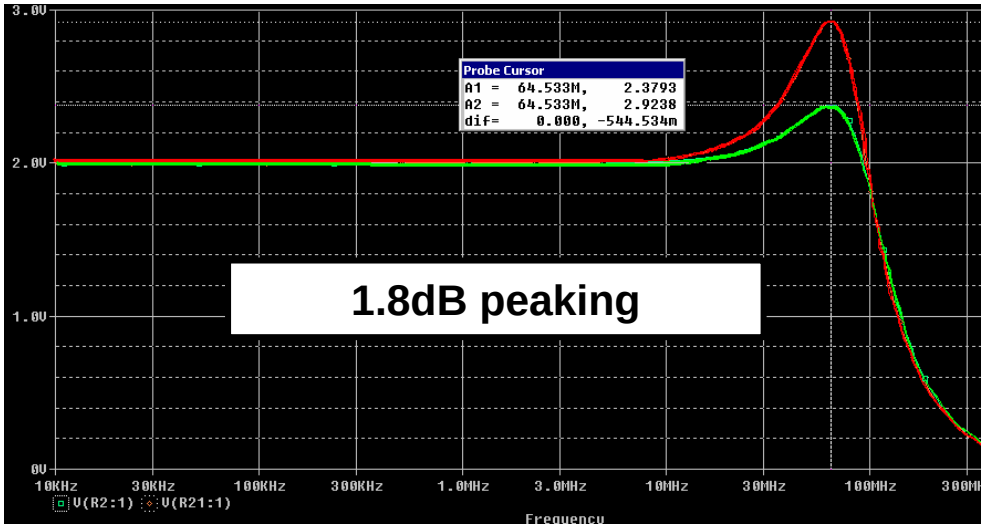
Stray Capacitance Simulation



1pF stray capacitance



Pulse Response with 1pF Stray Capacitance



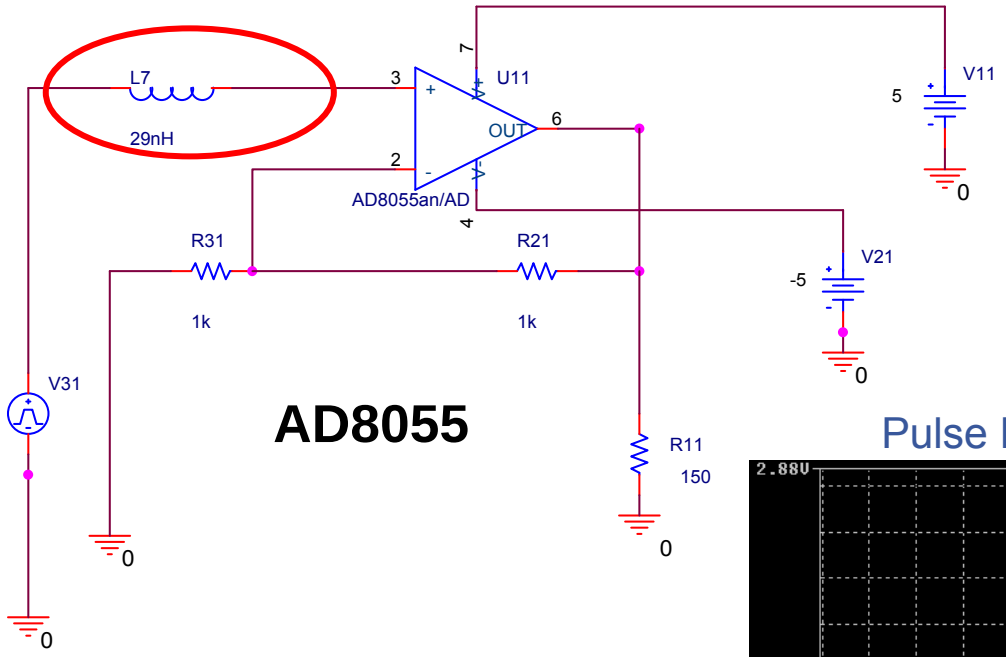
Frequency Response with 1pF Stray Capacitance

Reduce Overshoot

1) Increase board thickness
2) Reduce trace/pad area
3) Remove ground plane
4) Lower Resistance

Stray Inductance Simulation Schematic

1”x0.01” =29nH



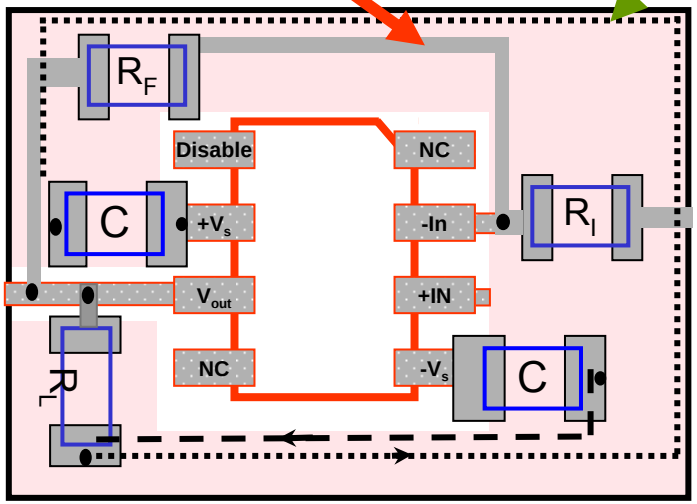
Pulse Response With and Without Ground Plane

Layouts – What to do and not do!

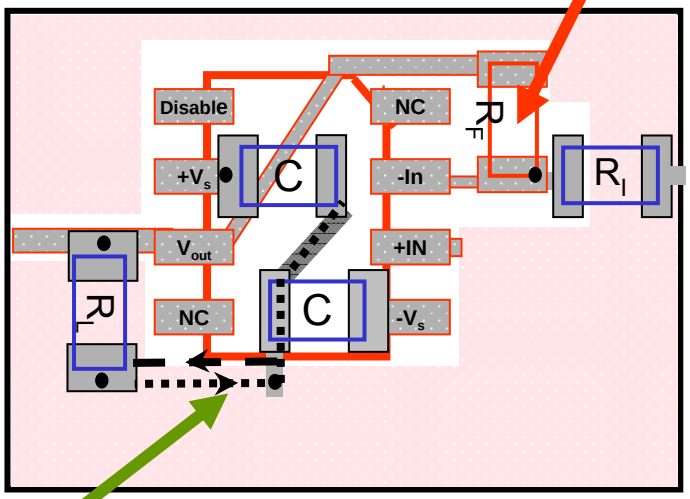
Even a few pF on summing junction can destabilize op amp

Vias and long return distance adds several nH

Remove ground plane under Negative input to reduce input capacitance



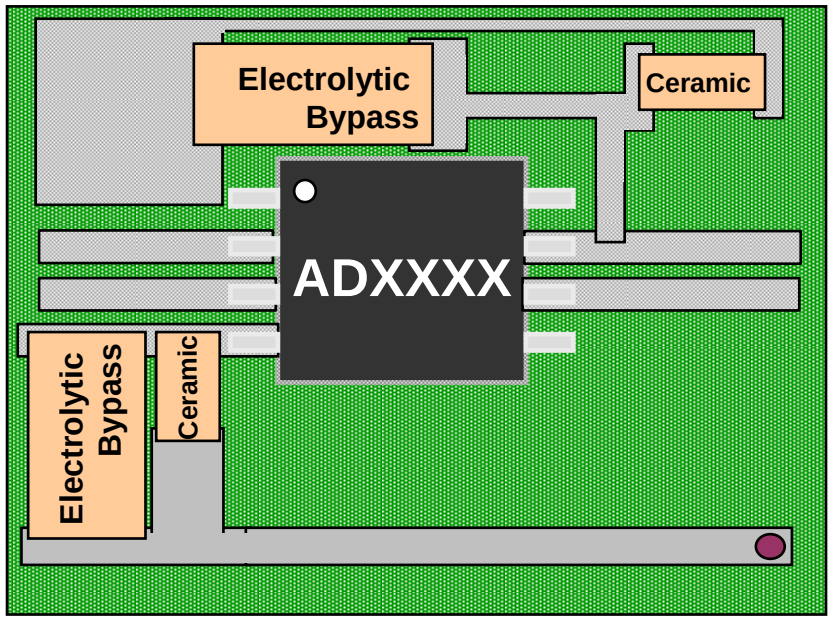
Bad PCB layout



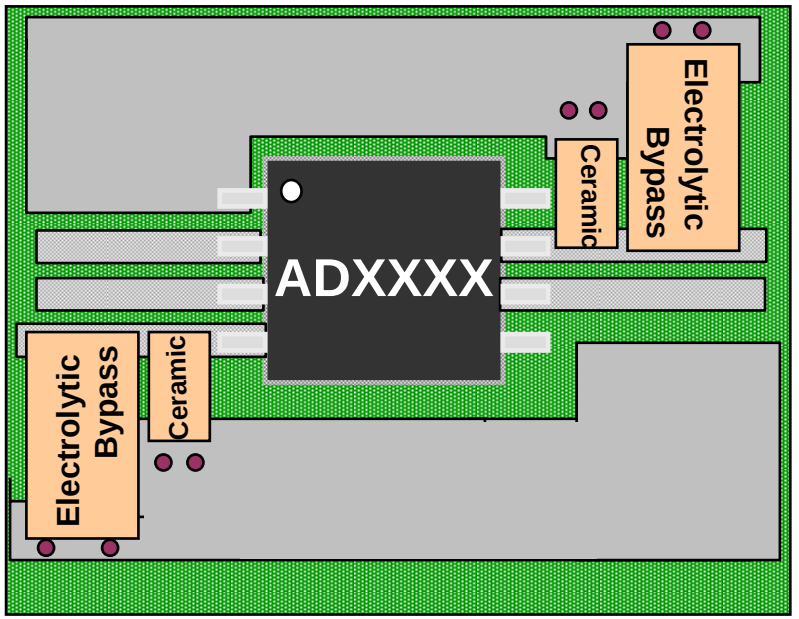
Good PCB layout

Reduce return path length to reduce Inductance

Power Supply Bypassing

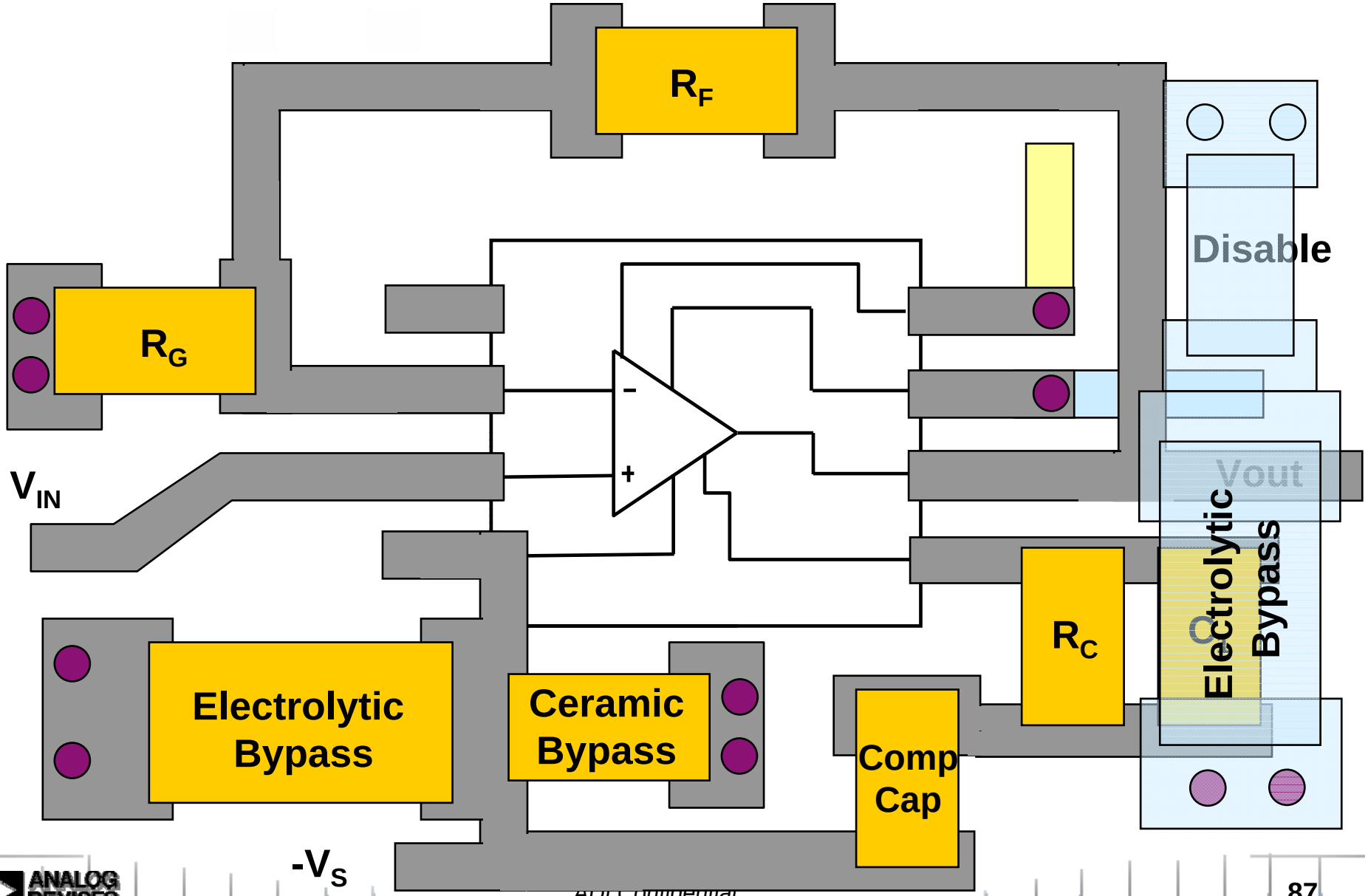


Incorrect

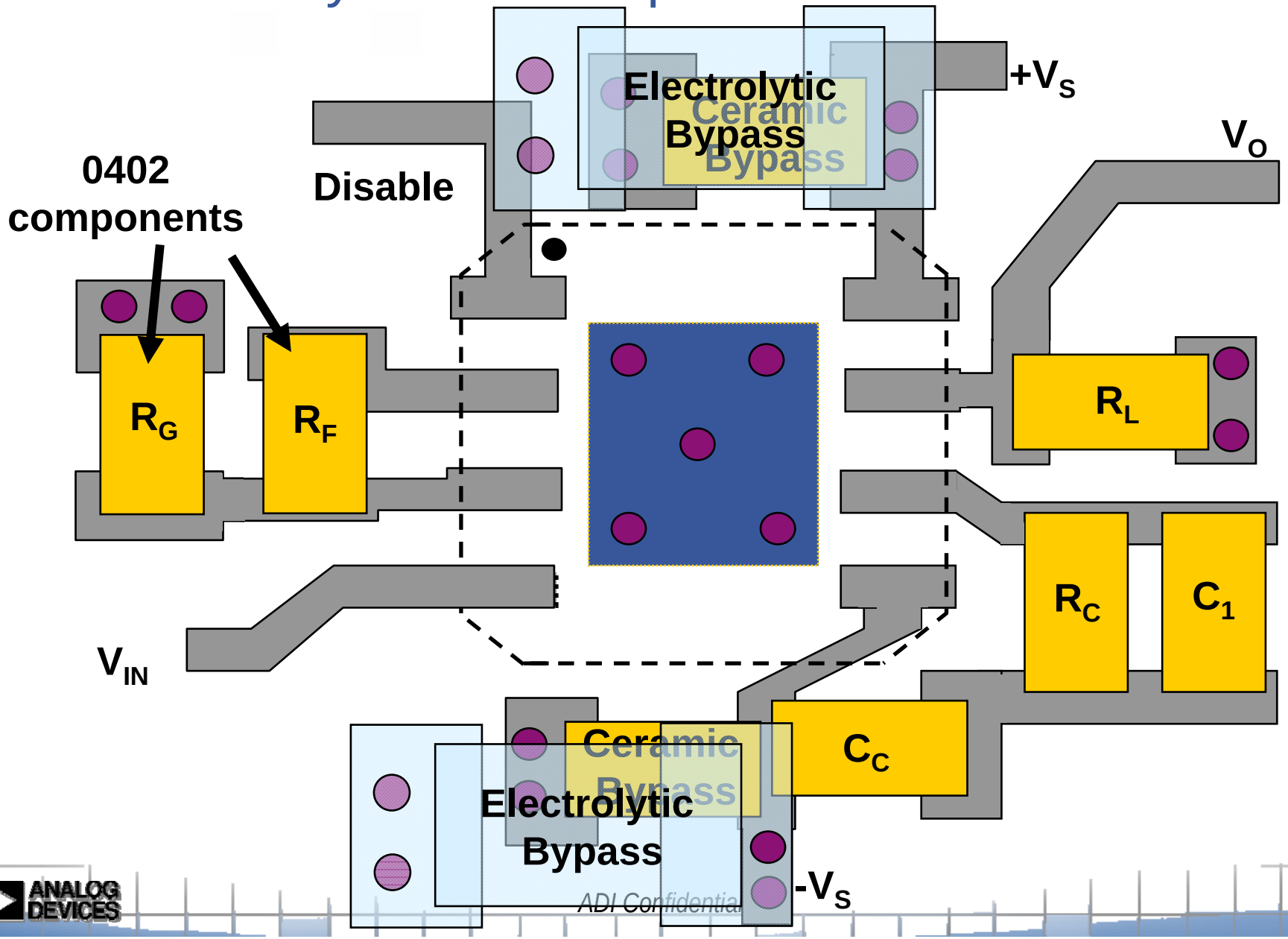


Correct

SOIC Layout Example



AD8099 Layout Example



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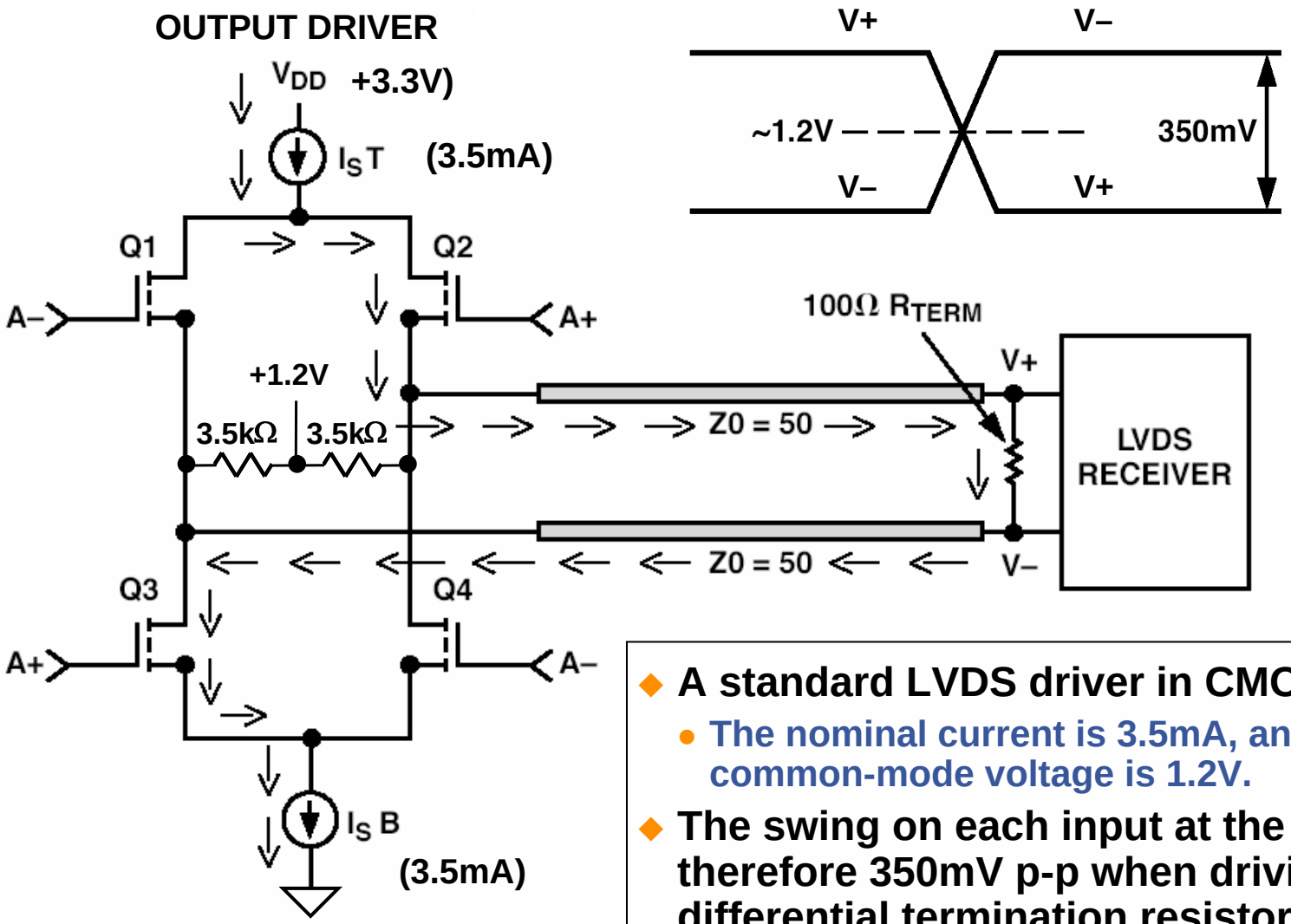
Mixed Signal PCB Layout

Control Differential Line Impedance

ADI

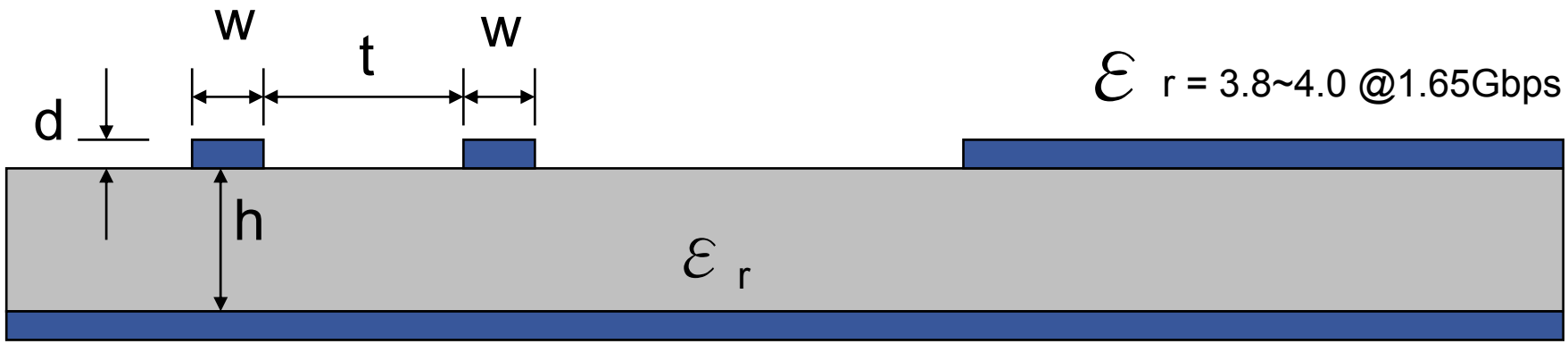
ANALOG DEVICES

Typical LVDS Driver in CMOS



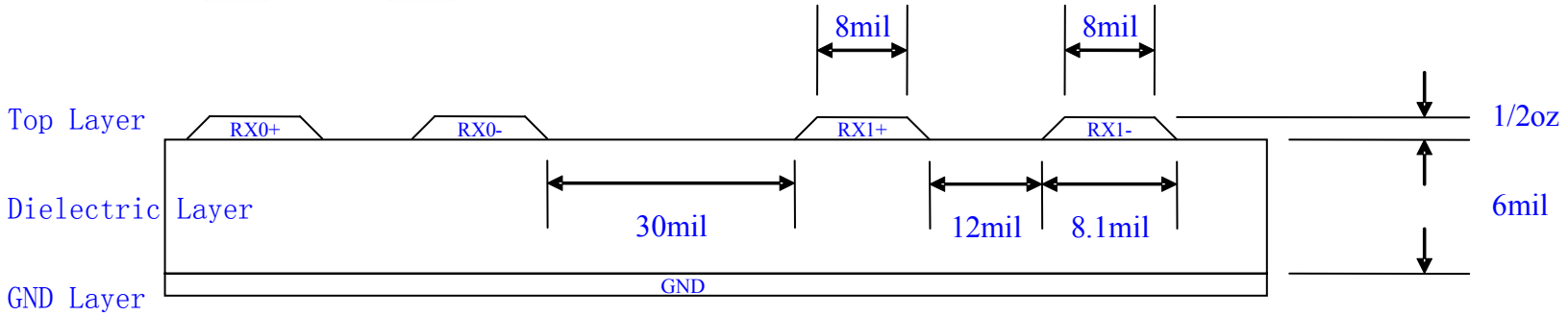
- **A standard LVDS driver in CMOS.**
  - **The nominal current is 3.5mA, and the common-mode voltage is 1.2V.**
- **The swing on each input at the receiver is therefore 350mV p-p when driving a 100Ω differential termination resistor.**
  - **This corresponds to a differential swing of 700mV p-p.**

Differential Line impedances



$$Zo_{diff}(\Omega) = \left[\frac{60}{\sqrt{0.475\varepsilon_r + 0.67}} * \ln\left[\frac{4h}{0.67(0.8w + d)}\right] * 2\right.$$

Control Differential Line Impendence



- **Control differential line impendence**
  - **Trace characteristic impedance will be around 54 Ohm single / 102 Ohm differential on ½ OZ copper (1.7mil) with dielectric of 4.7. After coating, it will change about 5-12 Ohm.**
  - **Distance between Differential line pair should be greater than 30mil to avoid interference of adjacent pairs.**
- **Lower down the length of differential lines**
  - **It's better to control >100MHz clock or RF signal trace length less than 2 inch.**
- **Routing differential signal pair together and minimize the total numbers of via on each trace as few as possible.**
- **Recommend software**
  - **Polar Si6000**

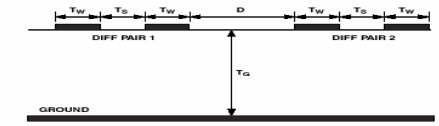
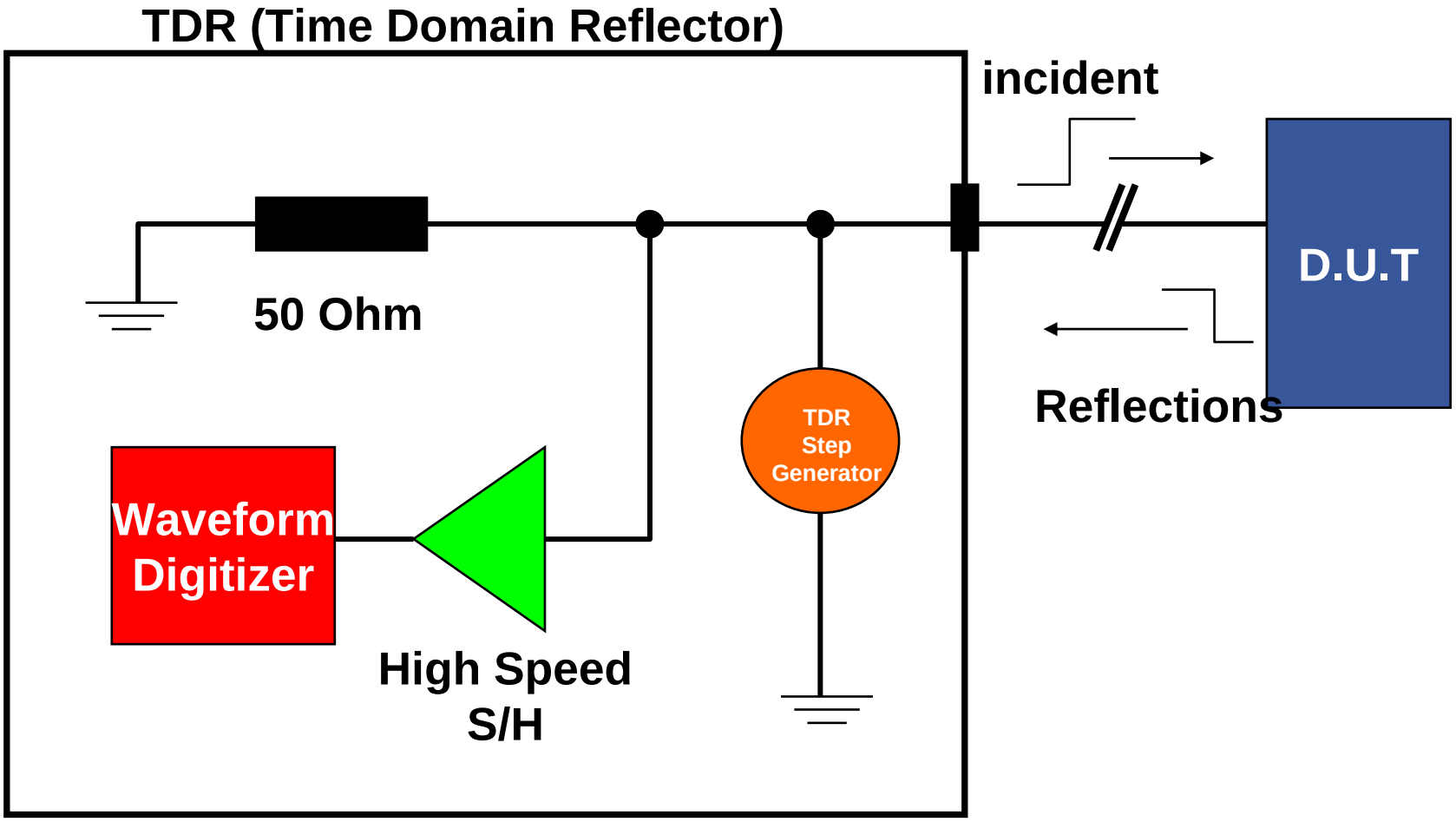


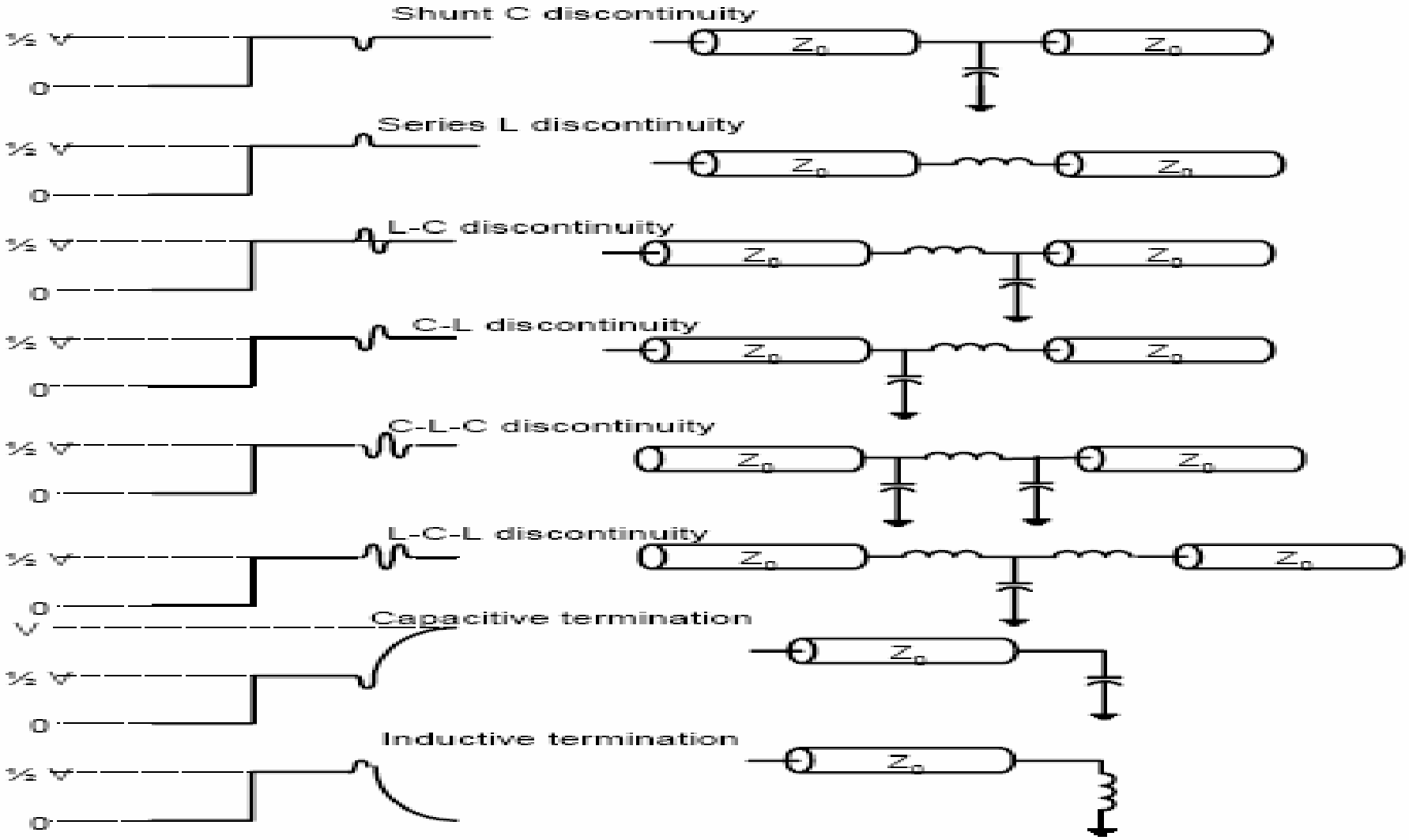
Figure 6. PCB Trace Spacing

Layout Guidelines
- Keep T_W, T_S, D constant over trace length
- Keep T_S ~ <2 T_W
- Avoid use of vias where possible
- Keep D >2 T_S
- Avoid 90 degree bends if possible
- Design T_W, T_G for ~50 Ω

Measuring the TMDS pair impedance



The Visual lumped interconnect analysis using TDR



Summary Mixed Signal Layout Techniques

- **Use ground plane**
  - **High speed applications require low impedance returns**
  - **Helps minimize parasitics**
- **Parasitics**
  - **Parasitic capacitance, inductance and resistance can ruin the best designed circuit**
  - **Layout is critical!**
- **Shielding Long Wire**
- **Control Differential Line Impendence**

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Small Signal PCB Layout

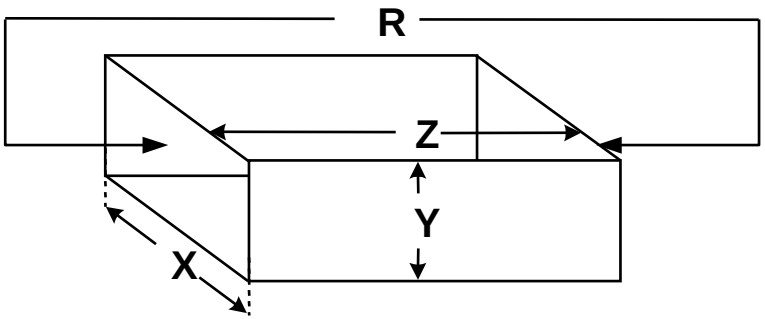
Consider loss on Track Resistor

ANALOG DEVICES

Calculation of Sheet resistance
(For Standard Copper PCB)

$$R = \frac{\rho Z}{X Y}$$

ρ = RESISTIVITY



SHEET RESISTANCE CALCULATION FOR 1 OZ. COPPER CONDUCTOR:

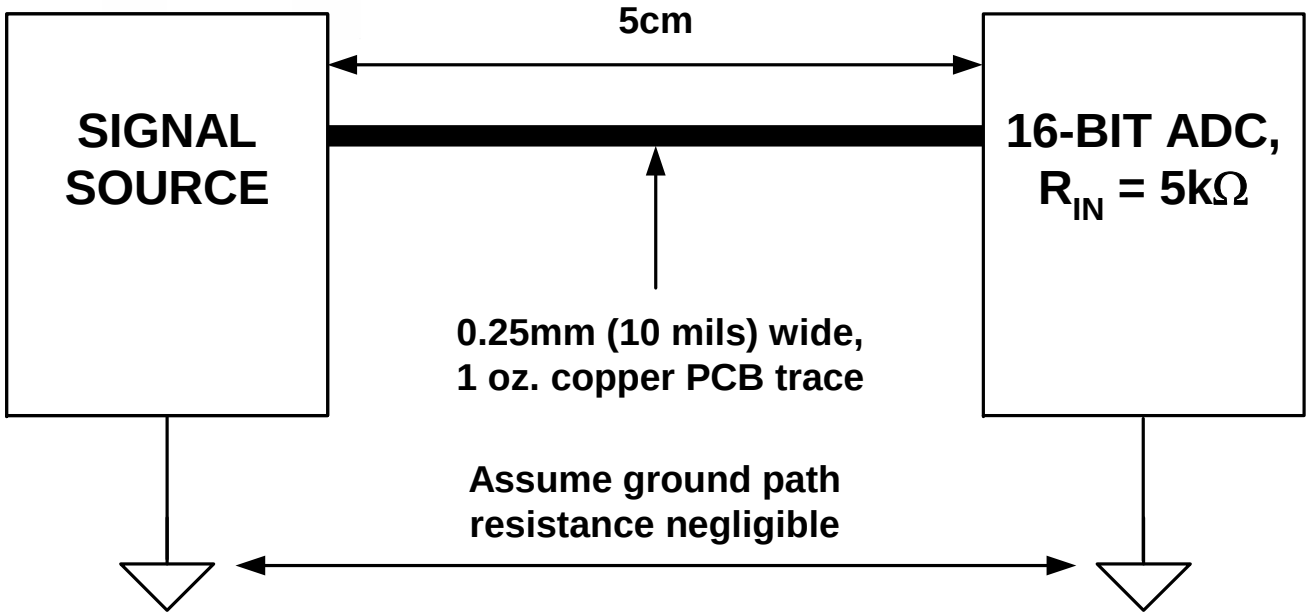
$\rho = 1.724 \times 10^{-6}\ \Omega cm$, Y = 0.0036cm

$$R = 0.48\frac{Z}{X}\ m\Omega$$

$\frac{Z}{X}$ = NUMBER OF SQUARES

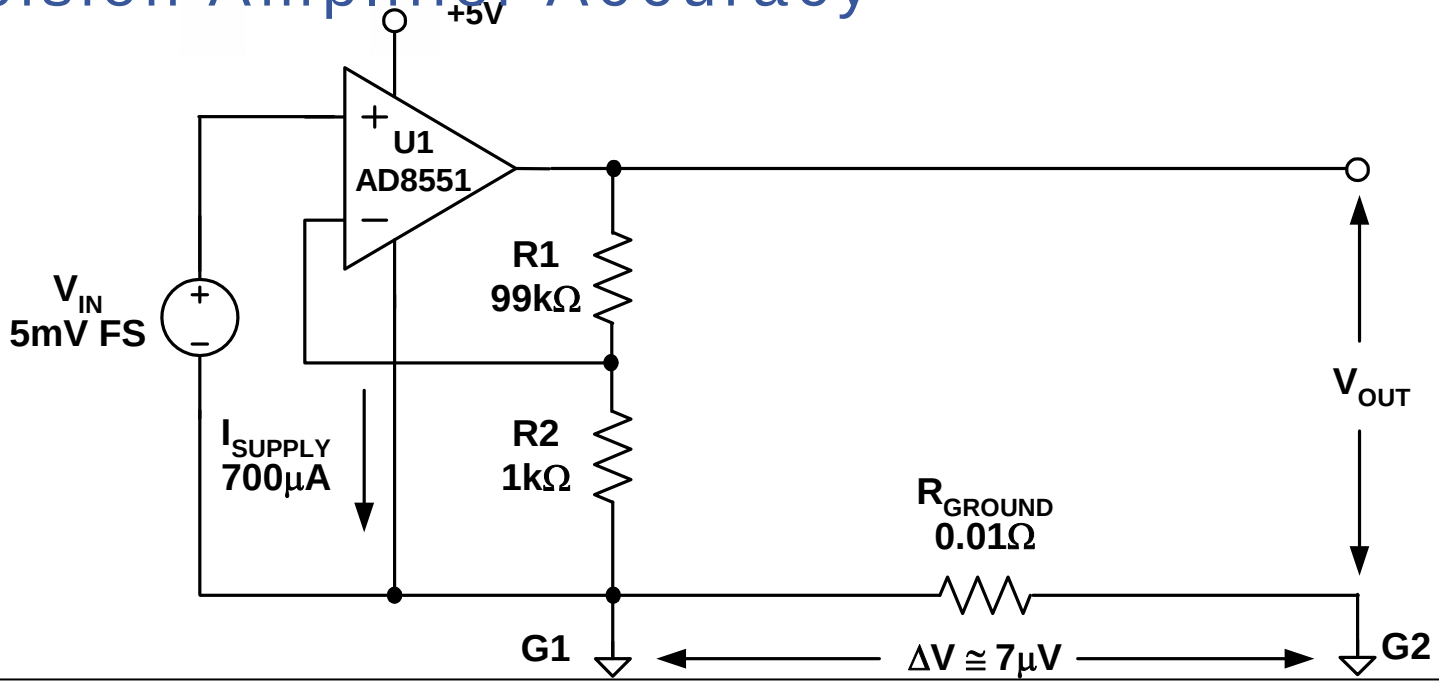
R = SHEET RESISTANCE OF 1 SQUARE (Z=X)
= 0.48mΩ/SQUARE

Long Track Resistance Impact on ADC



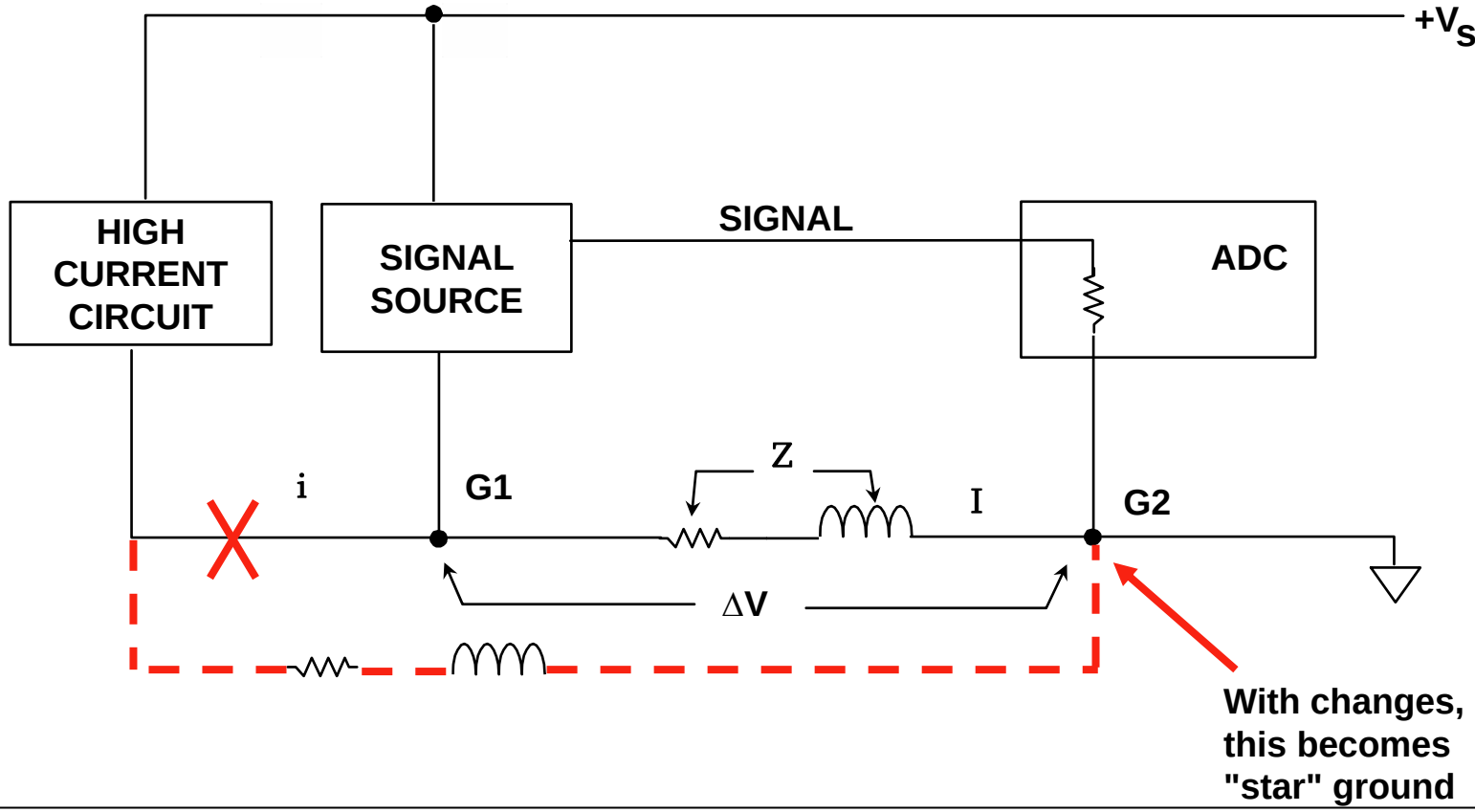
- **OHM's Law predicts >1 LSB of error due to drop in PCB conductor.**
  - Consider a 16-bit ADC with a 5kΩ input resistance,
  - PCB track is 5cm of 0.25mm wide 1 oz.
  - The track resistance of nearly 0.1Ω.
  - The resulting voltage drop is a gain error of 0.1/5k (~0.0019%),
  - Over 1LSB (0.0015% for 16 bits).

Small Common Ground Currents can degrade Precision Amplifier Accuracy



- **A low-level signal V_{IN} of 5mV FS, Design required to precisely gain of 100.**
  - **Using an AD8551 chopper-stabilized amplifier for best dc accuracy.**
  - Recall AD8551 Spec:
    - **Low offset voltage: 1 μV, offset drift: 0.005 μV/° C**
- **At the load end, the signal V_{OUT} is measured with respect to G2, the local ground.**
  - **Because of the small 700μA I_{SUPPLY} of the AD8551 flowing between G1 and G2, there is a 7μV ground error on 0.01Ohm Ground impedance.**
  - **About 7 times the typical input offset expected from the op amp!**

A More Realistic Model of a Ground System



- **Any current flow through a common ground impedance can cause errors**
- **$\Delta V = (I + i) * Z$**
  - **Z: The impedance between G1 and G2**
  - **I : Signal related currents.**
  - **i : The effect of any non-signal related currents.**

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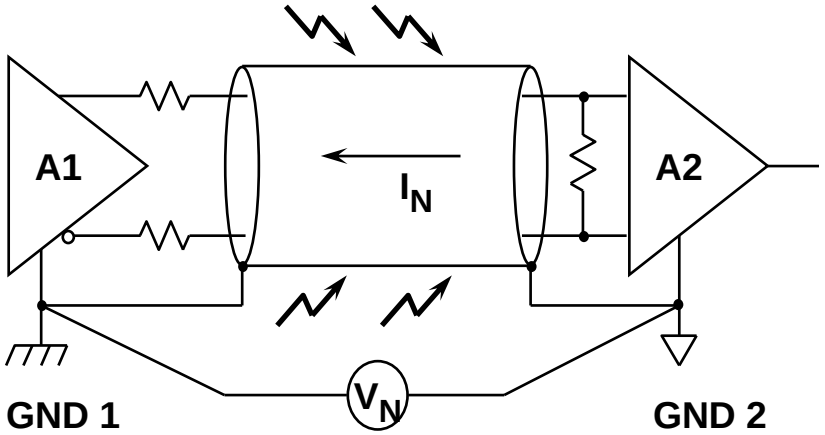
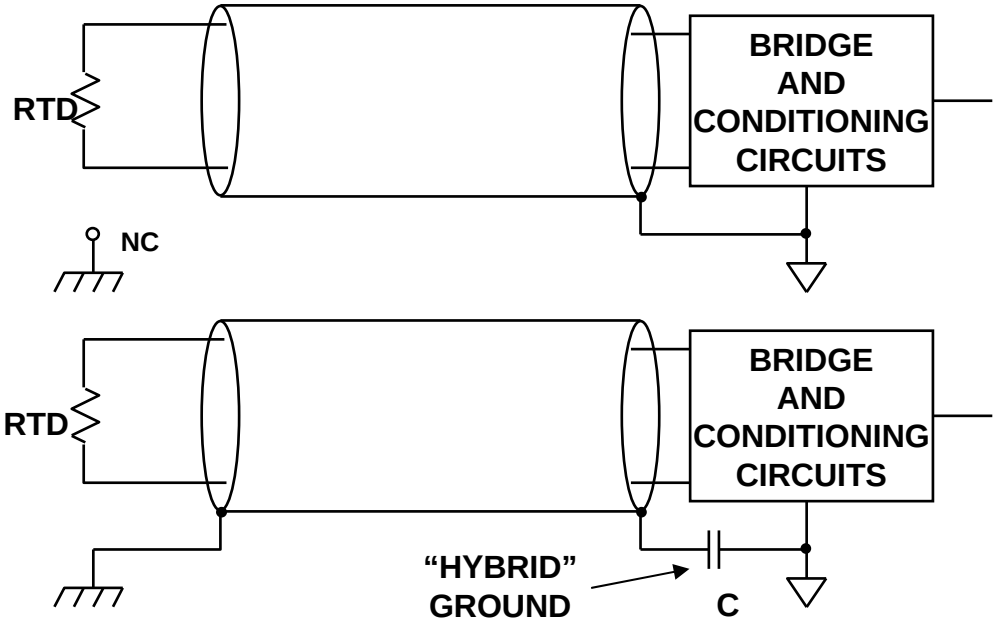
Small Signal PCB Layout

Proper Grounding Shielding Cable

ANALOG DEVICES

Ground loops in shield twisted pair cable

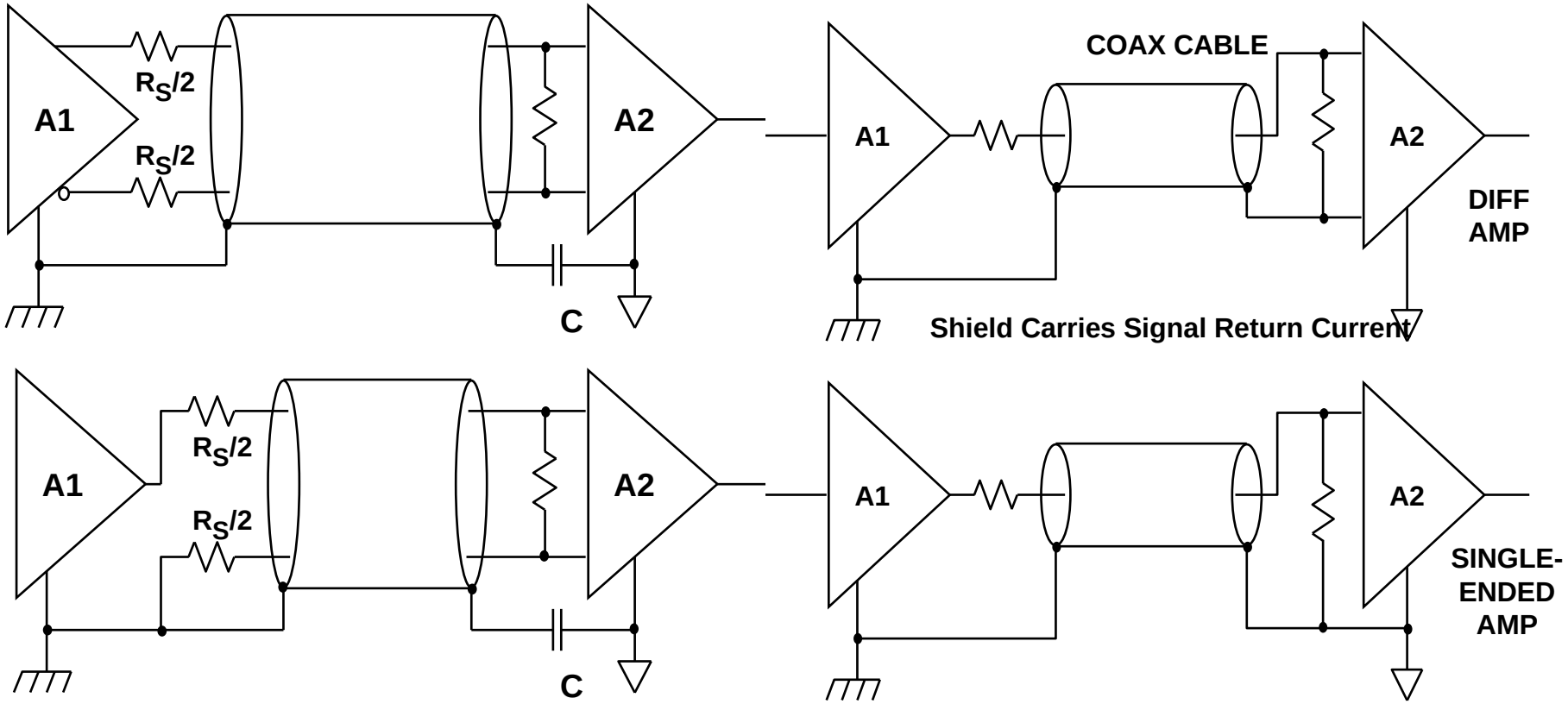




- **Ground loops in shield twisted pair cable can cause errors**
- **V_N Causes Current in Shield (Usually 50/60Hz)**
- **Differential Error Voltage is Produced at Input of A2 Unless:**
  - **A1 Output is Perfectly Balanced and**
  - **A2 Input is Perfectly Balanced and**
  - **Cable is Perfectly Balanced**

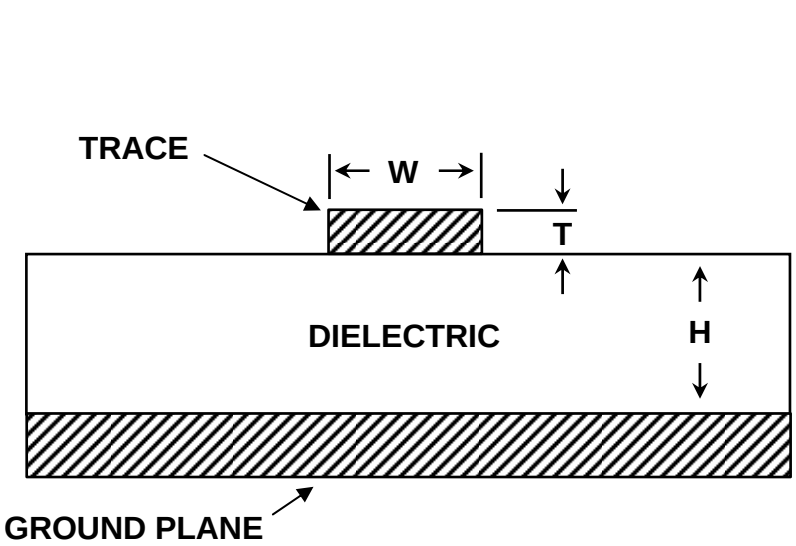
- **Hybrid grounding of shielded cable with passive sensor**

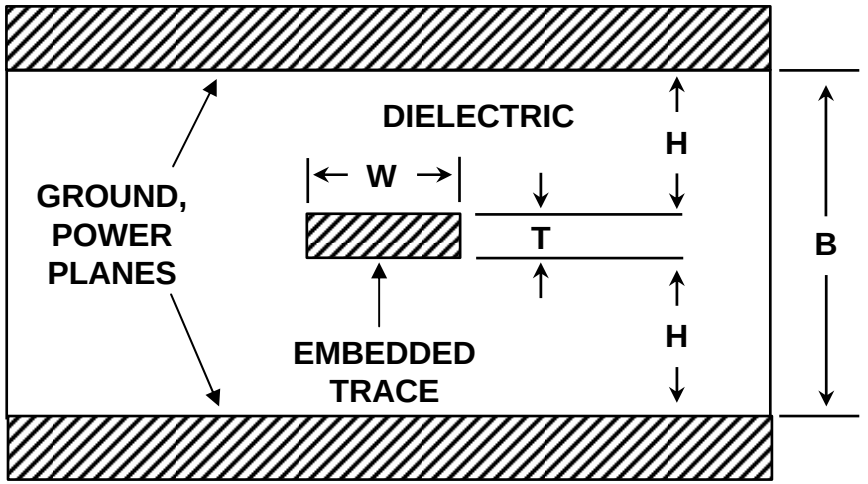
Impedance-balanced Driver of Balanced Drive of Balanced Shielded Cable & Coaxial Cables



- Impedance-balanced driver of balanced drive of balanced shielded cable aids noise-immunity with either balanced or single end source signals
- Coaxial cables can use either balanced or single-ender receivers

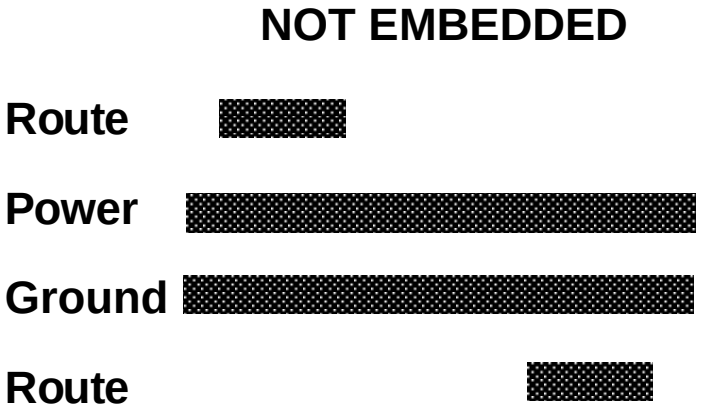
Transmitter low level IF/RF signal with Micro-Strip line

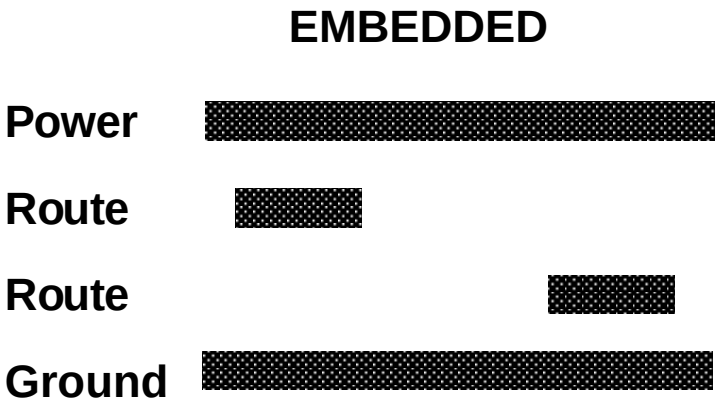




- A micro-strip transmission line with defined impedance is formed by a PCB trace of appropriated geometry, spaced from a ground plane.
- A Symmetric strip line transmission line with defined impedance is formed by a PCB trace of appropriate geometry embedded between equally spaced ground and/or power planes.

The pros and cons of not embedded vs the embedded signal trace in multi-layer PCB design





- **Fast switching signals (clocks etc) should be shielded**
  - Using digital ground to avoid radiating noise
  - Clock signals should never be run near analog inputs of the devices
  - Avoid cross over of digital and analog signals.
- **Advantages of embedded traces**
  - Signal traces shielded and protected
  - Lower impedance, thus lower emissions and crosstalk
  - Significant improvement > 50MHz
- **Disadvantages of embedded traces**
  - Difficult prototyping and troubleshooting
  - Decoupling may be more difficult
  - Impedance may be too low for easy matching

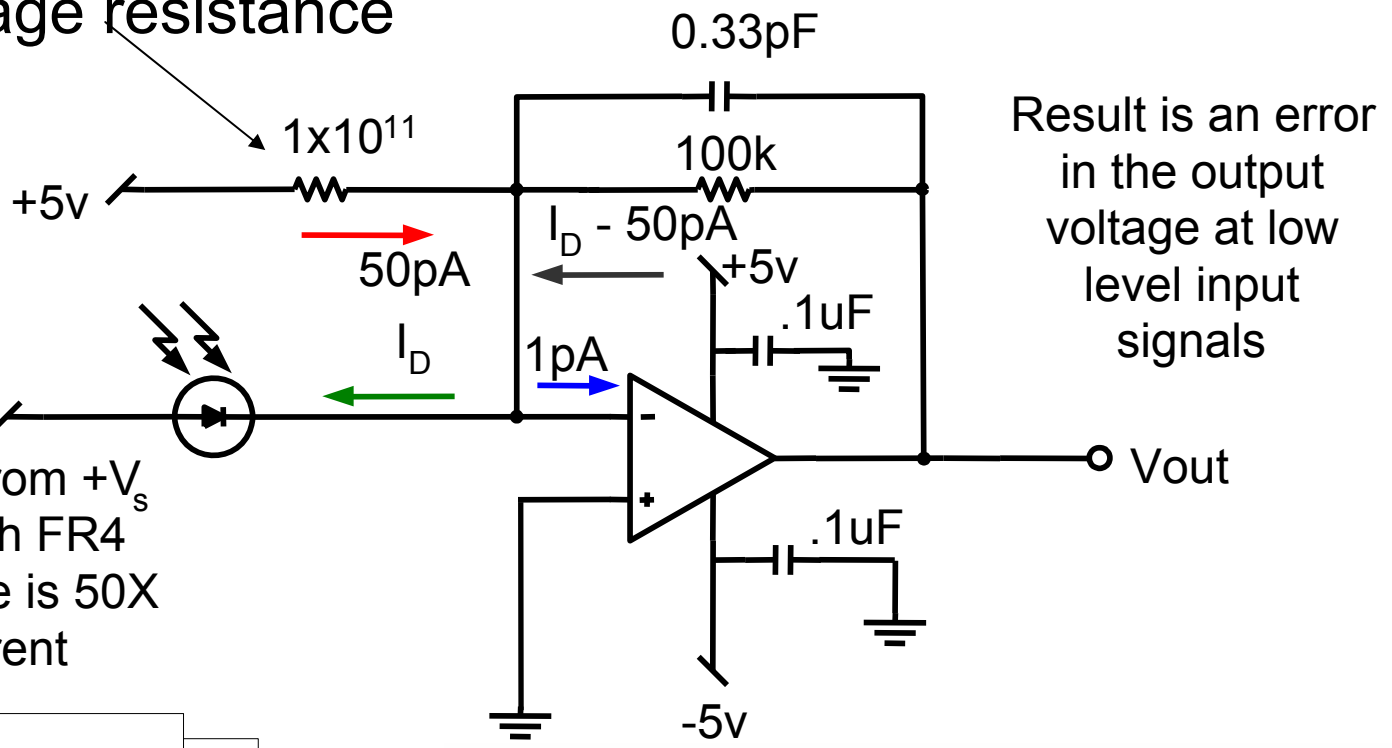
Small Signal PCB Layout

Minimize PCB Leakage by Guard Ring

ANALOG DEVICES

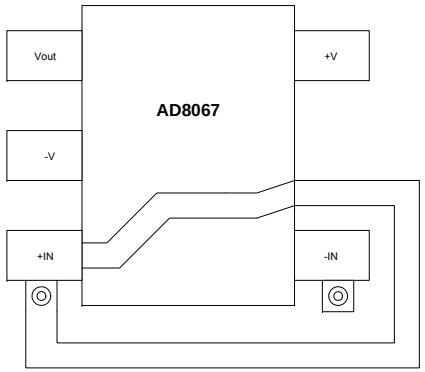
Using Guard-Rings Minimizes PCB Leakage Paths

Board leakage resistance

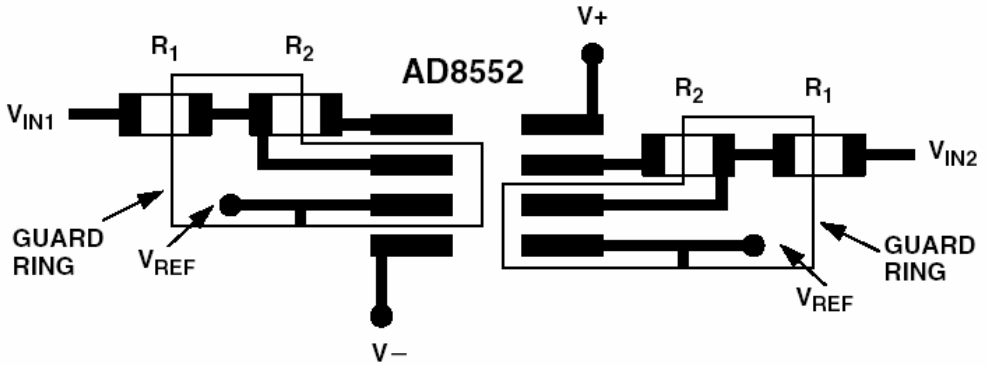


Result is an error in the output voltage at low level input signals

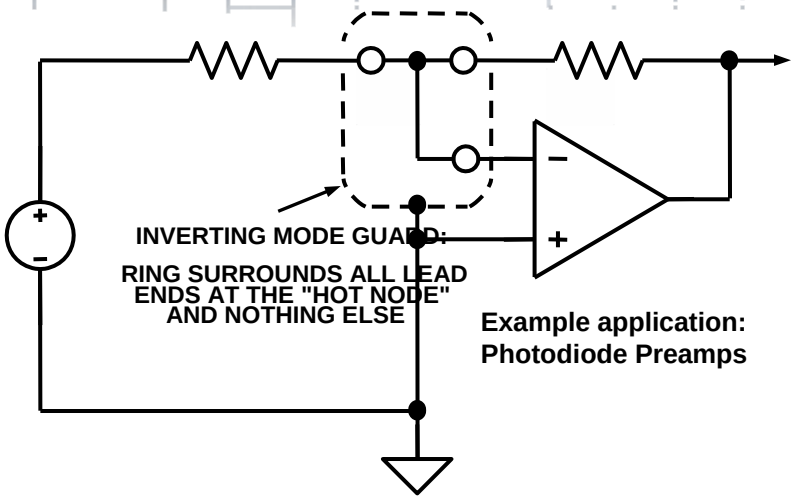
Leakage current from $+V_s$ pin to $-V_{in}$ through FR4 SOT23-5 package is 50X Input bias current

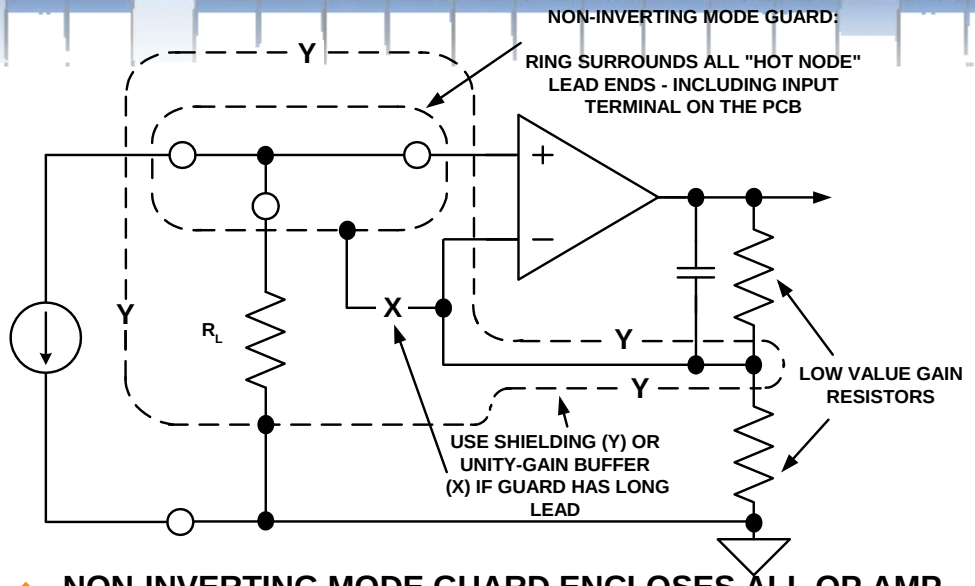


Inverting



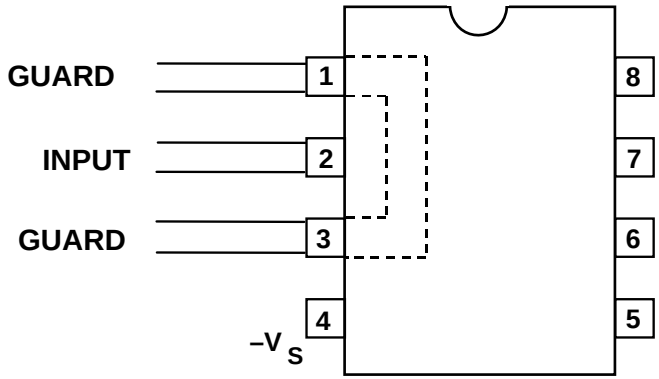
Guard Patterns



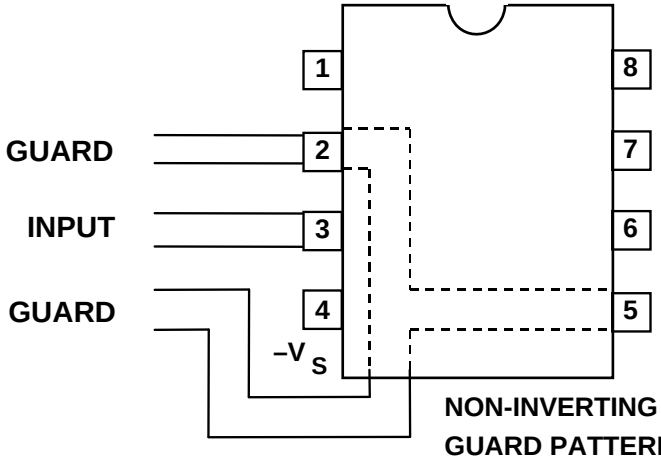


- INVERTING MODE GUARD ENCLOSES ALL OP AMP INVERTING INPUT CONNECTIONS WITHIN A GROUNDED GUARD RING
- NON-INVERTING MODE GUARD ENCLOSES ALL OP AMP NON-INVERTING INPUT CONNECTIONS WITHIN A LOW IMPEDANCE, DRIVEN GUARD RING

NOTE: PINS 1, 5, & 8 ARE OPEN ON MANY "R" PACKAGED DEVICES



INVERTING MODE GUARD PATTERN

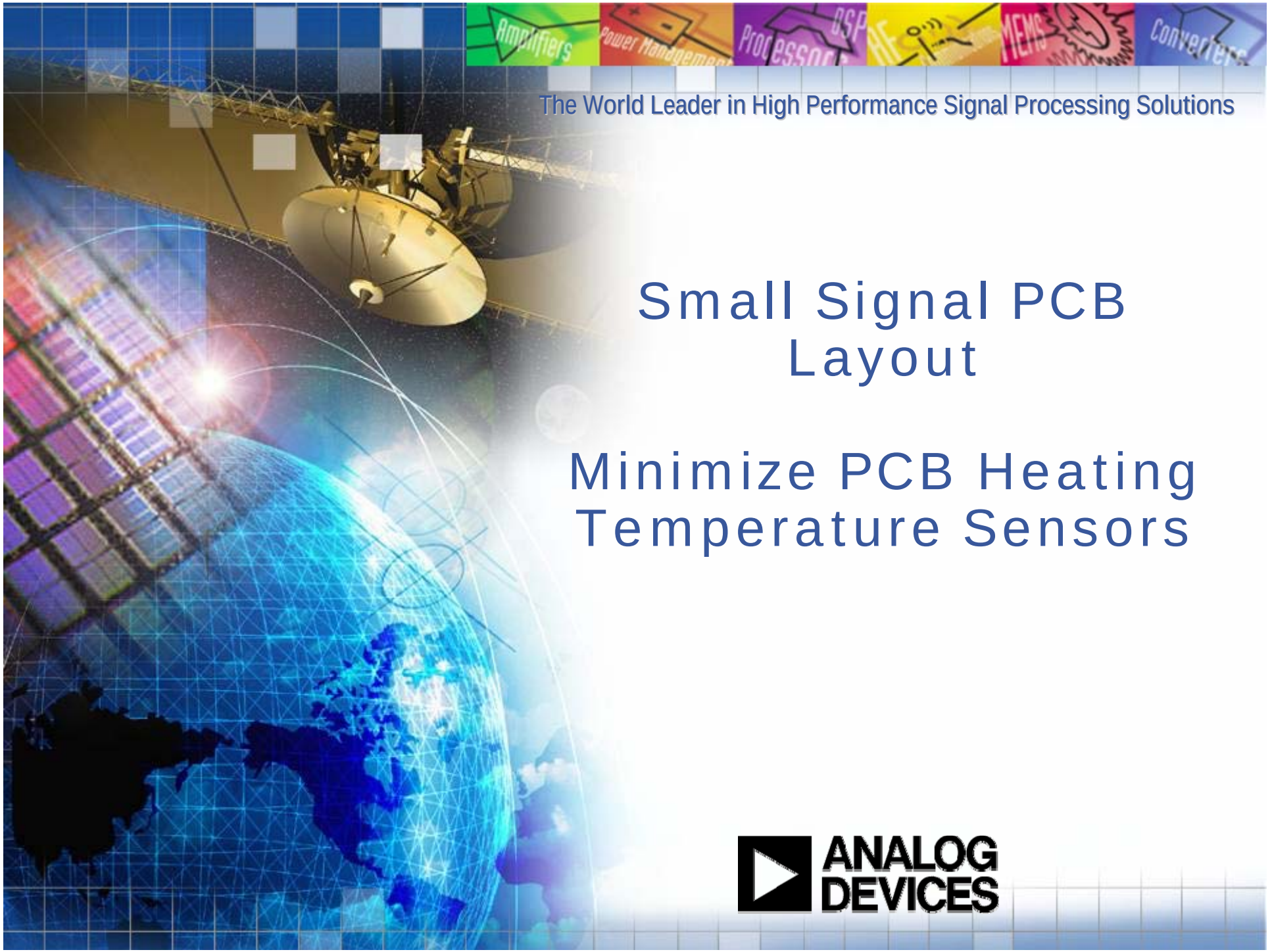


NON-INVERTING MODE GUARD PATTERN

- PCB GUARD PATTERNS FOR INVERTING AND NON-INVERTING MODE OP AMPS USING 8 PIN SOIC (R) PACKAGE

Summary of PCB Layout Skills For Low PCB Leakage Applications

- **Including photodiodes, pressure sensors, and other high source impedance inputs**
- **#1) Use a CMOS or JFET input amplifier**
- **#2) Minimize the PC-board leakage current**
  - **Keep trace lengths as short as possible**
  - **Use guard rings around the input pins**
- **#3) Keep the board CLEAN!!**
  - **Dirt and oil are a major cause of PC-board leakage current**



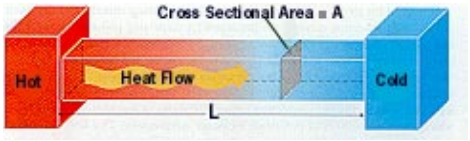
Small Signal PCB Layout

Minimize PCB Heating Temperature Sensors

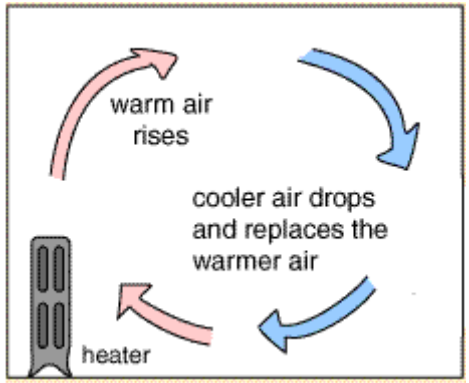
ANALOG DEVICES

Minimize PCB Heating Temperature Sensors Basics
Heat Transfer

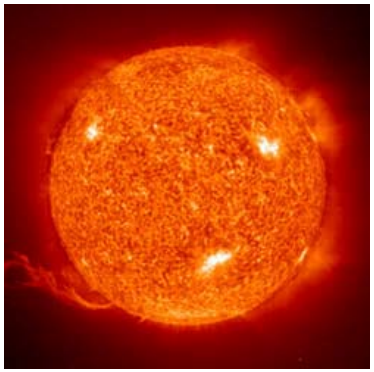
- **The transfer of heat is normally from a high temperature object to a lower temperature object.**
  - **Heat transfer from a cold region to a hot region can be done by forcing the system e.g. refrigerators, to perform the energy transfer.**
- **Heat transfer is accomplished by three basic methods –**
  - **Conduction**
  - **Convection**
  - **Radiation**



Conduction



Convection

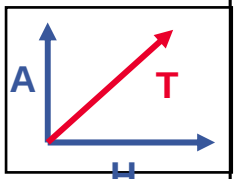


Radiation

Minimize PCB Heating Temperature Sensors Basics

Heat Transfer Theory - Conduction

- **Conduction is the most prevalent heat transfer method in pcbs**
  - **If one end of a PCB is at a higher temperature, then energy will be transferred down the PCB towards the colder end. The higher speed particles will collide with the slower ones with a net transfer of energy to the slower ones. The rate of conduction heat transfer is:**



$$H = (K \times A (T_{HOT} - T_{COLD}) / L$$

H = Energy conducted in time (joules/second)

K = Thermal conductivity of the copper (385 W/(m·K) @ room temp)

A = Area of copper on pcb

T = Temperature

L = Distance between hot and cold bodies

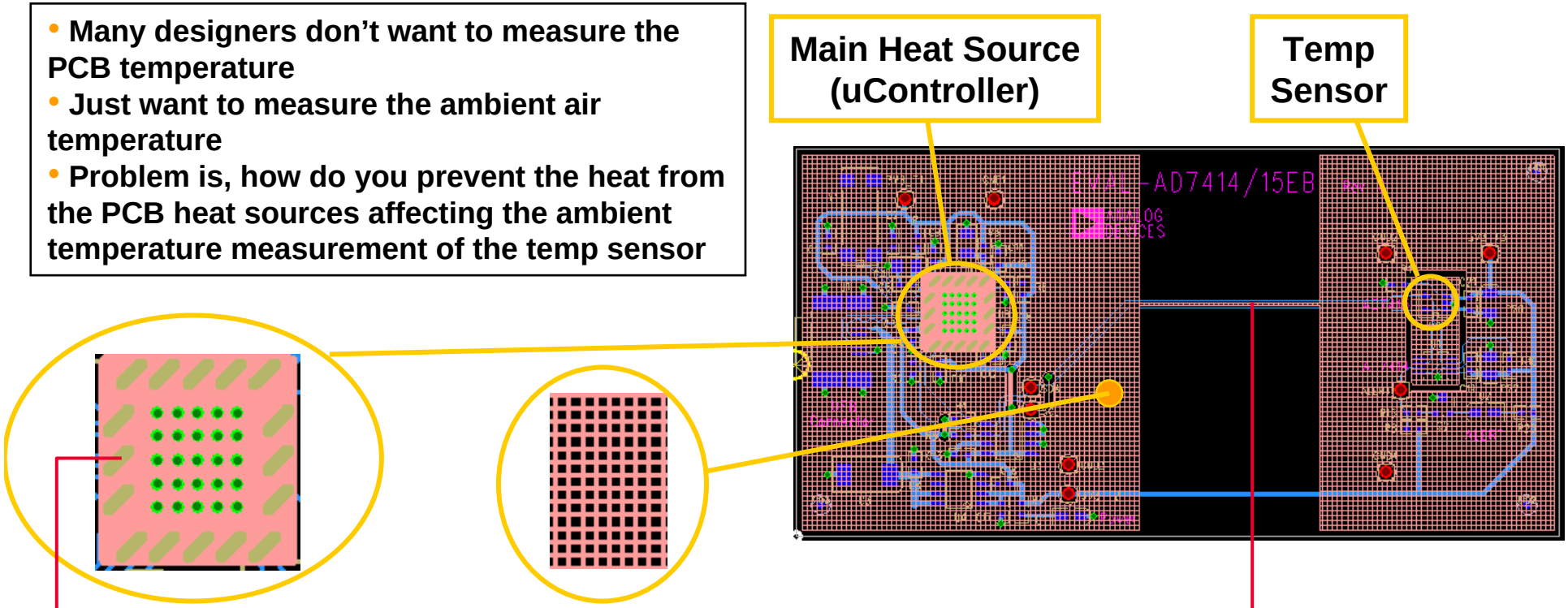
Excellent Temperature Conductive Material

Material	rmal conductivity W/m·K
Diamond	1000-2600
Silver	406
Copper	385
Gold	320
Aluminium	205
Brass	109
Platinum	70
Steel	50.2
Lead	34.7
Mercury	8.3
Quartz	8
Ice	1.6
Glass	0.8
Water	0.6
Wood	0.04-0.12
Wool	0.05
Fiberglass	0.04
Expanded polystyrene ("beadboard")	0.03
Air (300 K, 100 kPa)	0.026
Silica aerogel	0.017
Styrofoam	0.01

Minimize PCB Heating Temperature Sensors

Correct PCB layout for measuring ambient temperature

- Many designers don't want to measure the PCB temperature
- Just want to measure the ambient air temperature
- Problem is, how do you prevent the heat from the PCB heat sources affecting the ambient temperature measurement of the temp sensor



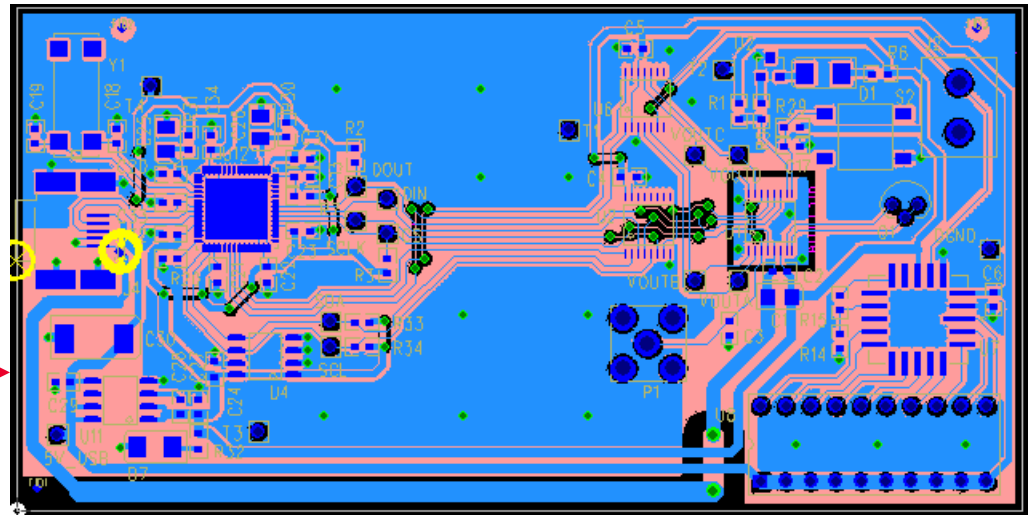
Tips for ambient temperature measurement

- Use a hatched GND plane. Reduce GND plane area therefore increasing thermal resistance.
- Keep the temp sensor as far away from heat sources as possible.
- Use a separate GND plane for the temp sensor and keep connections to main GND plane as low as possible.
- Use narrow GND connections as this will increase thermal resistance.
- Use solid GND plane under main heat source and expose green solder mask. This will give the min thermal resistance for the MHS to dissipate heat.

Minimize PCB Heating Temperature Sensors

Summary…

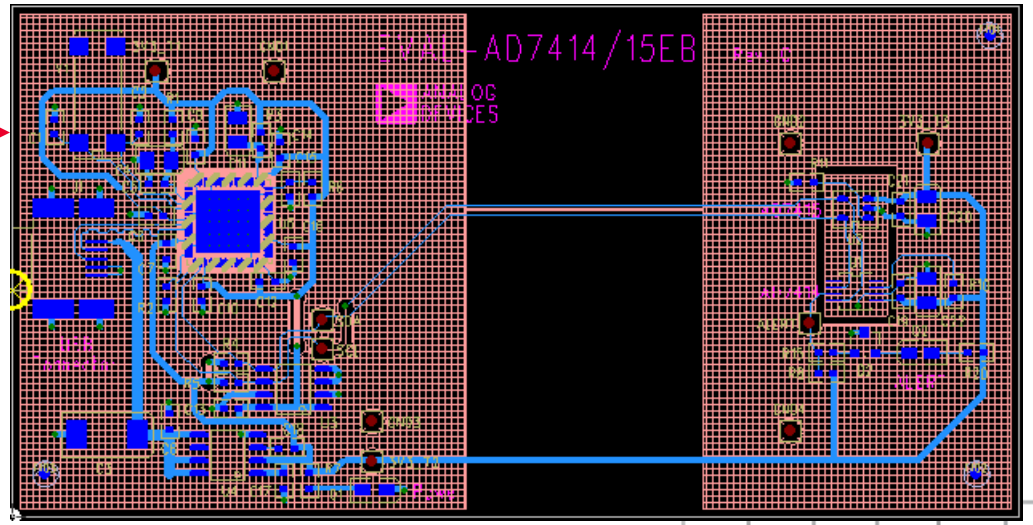
• Most customers will want to use IC Temp Sensors to measure the temperature of the PCB or a component.
•Therefore it is better to use this pcb layout technique.



$$H = (K \times A (T_{HOT} - T_{COLD}) / L$$

H = Energy conducted in time (joules/second)
K = Thermal conductivity of the copper (385 W/(m·K) @ room temp)
A = Area of GND plane
T = Temperature
L = Distance between hot and cold bodies

• There will be some customers that want to monitor air temperature and also use the accuracy, linearity, speedy response and convenience of an IC temp sensor.
• Therefore they should use this pcb layout technique.



Backup

Further References

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11. "*Low-Impedance Power Delivery Over Broad Frequencies*", J. Fang, J. Zhao, Printed Circuit Design & Manufacture, Sept, 2003.
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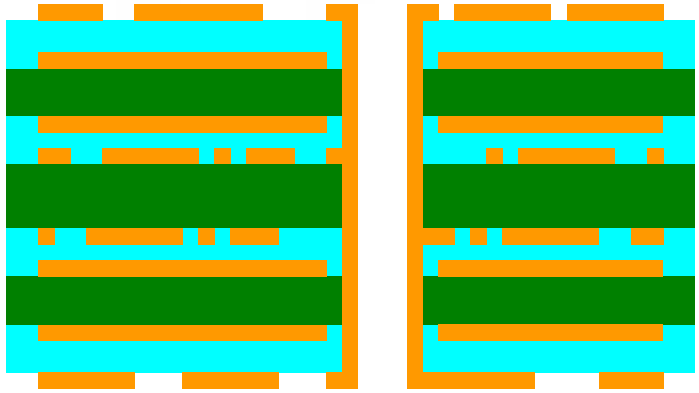
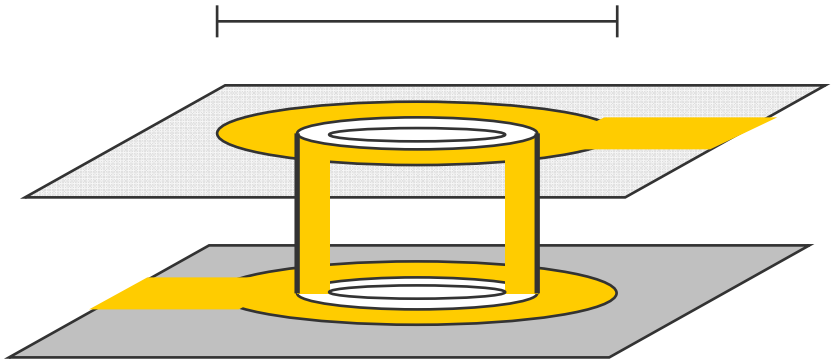
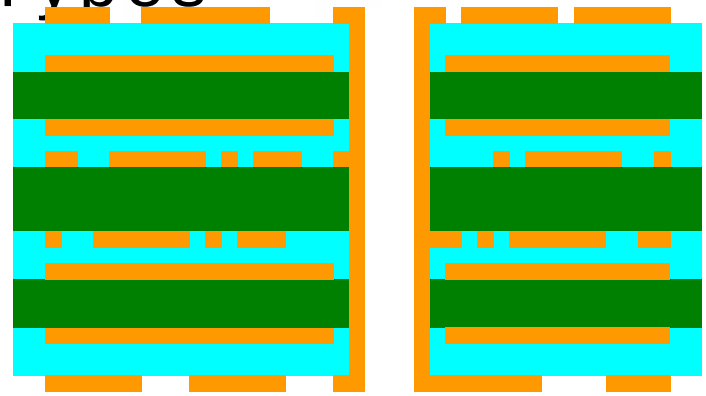
PCB Basics
Vias

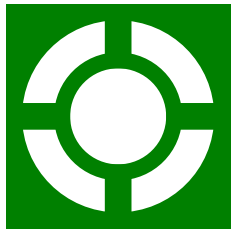




- **Vias (plated holes)**
  - **Used to connect layers**
  - **Formed by drilling or punching hole through PCB and plating the inside**
  - **Typically much larger than signal traces**
- **Blind**
- **Signal Integrity Tip: PCBs introduce capacitance and change the characteristic impedance of a trace.**

PCB Basics
Vias Types





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